

UFS Memory Device Data Sheet

Revision 1.10
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Toshiba Memory Corporation

256GB THGAF8T1T83BAIR

Table of Contents

| | |
|--|----|
| 1. INTRODUCTION | 3 |
| 2. FEATURES..... | 5 |
| 2.1. Toshiba UFS modules Interface | 5 |
| 2.2. Pin Assignment and Description..... | 5 |
| 2.3. Part Number | 7 |
| 2.4. Operating Temperature | 7 |
| 2.5. Storage Temperature..... | 7 |
| 2.6. Performance..... | 7 |
| 2.7. Power Supply..... | 8 |
| 2.8. Operating Current (RMS) | 8 |
| 2.9. Sleep Mode Current..... | 8 |
| 2.10. Product Architecture | 9 |
| 3. PRODUCT SPECIFICATIONS | 10 |
| 3.1. Package Dimensions..... | 10 |
| 3.2. Density Specifications | 11 |
| 3.3. M-PHY Attributes | 11 |
| 3.4. UniPro Attributes | 15 |
| 3.5. UPIU Transaction codes | 21 |
| 3.6. UFS Descriptors | 21 |
| 3.7. UFS Flags..... | 31 |
| 3.8. UFS Attributes..... | 32 |
| 3.9. UFS SCSI Commands | 33 |
| 3.10. Mode Pages..... | 34 |
| 3.11. Standard INQUIRY data | 36 |
| 3.12. Vital Product Data..... | 37 |
| 4. ELECTRICAL CHARACTERISTICS | 42 |
| 4.1. Absolute Maximum Ratings..... | 42 |
| 4.2. H/W Reset Operation..... | 42 |
| 4.3. Reference Clock | 43 |
| 4.4. Power Supply..... | 44 |
| 4.5. M-PHY Characteristics | 46 |
| 5. Reliability Guidance..... | 53 |
| 6. Reference | 54 |
| 7. Document Revision History | 54 |

1. INTRODUCTION

THGAF8T1T83BAIR is JEDEC UFS specification Ver.2.1 compliant NAND flash memory housed in 153 ball BGA package. This memory utilizes advanced TOSHIBA NAND flash memory and a controller chip assembled as Multi Chip Module.

Figure 1 shows the system model of TOSHIBA UFS Ver.2.1 memory. This memory supports HS-G1/G2/G3 A/B GEAR, and PWM-G1/G2/G3/G4 GEAR, and has differential input/output pins, some functional pins, power pins and ground pins. Data line specification is defined in M-PHY^R, and Reference clock and Reset signal specification is defined in UFS.

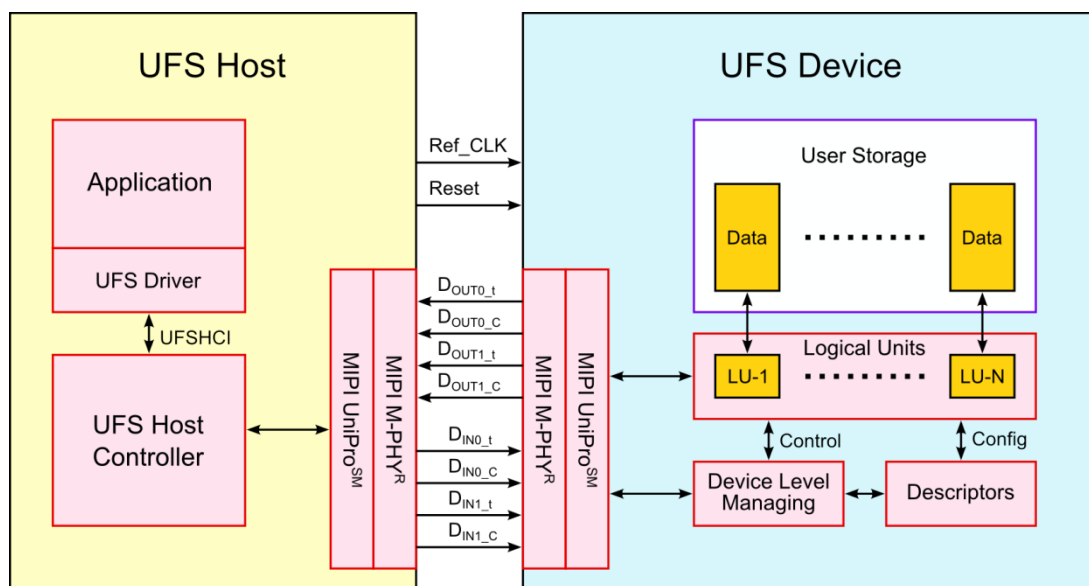


Figure 1 UFS System Model

Figure 2 shows UFS top level architecture. UFS adopts layered communication architecture based on a SCSI SAM architectural model. Lower layer specification than UTP is defined in MIPI UniProSM and M-PHY^R specification.

A UFS module can contain one or more Logical Units (LUs), and LUs can be accessed simultaneously. THGAF8T1T83BAIR supports maximum 32 LUs. All access to UFS storage should be through correspondent LUs with UFS SCSI command subset, thus users need to configure appropriate LUs on UFS Configuration Descriptor for their own application. Device Descriptors, which includes device configuration variables, can be accessed through UFS Device Manager.

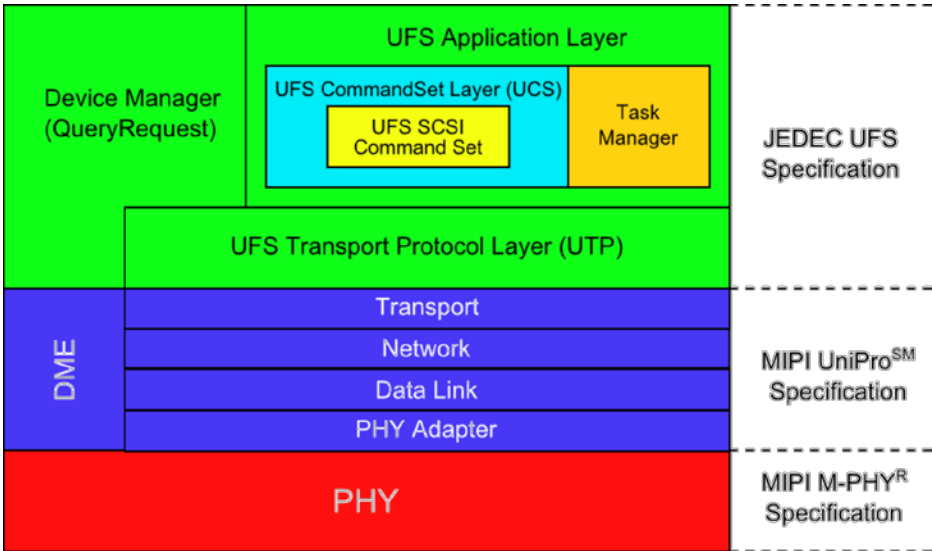


Figure 2 UFS Top Level Architecture

2. FEATURES

2.1. Toshiba UFS modules Interface

Toshiba UFS modules have downstream data lanes and upstream data lanes which are specified by M-PHY^R, Reference Clock and Reset Signal which are specified by UFS.

2.2. Pin Assignment and Description

P-VFBGA153-1113-0.50 (11.5mm x 13mm, H1.0mm max. package)

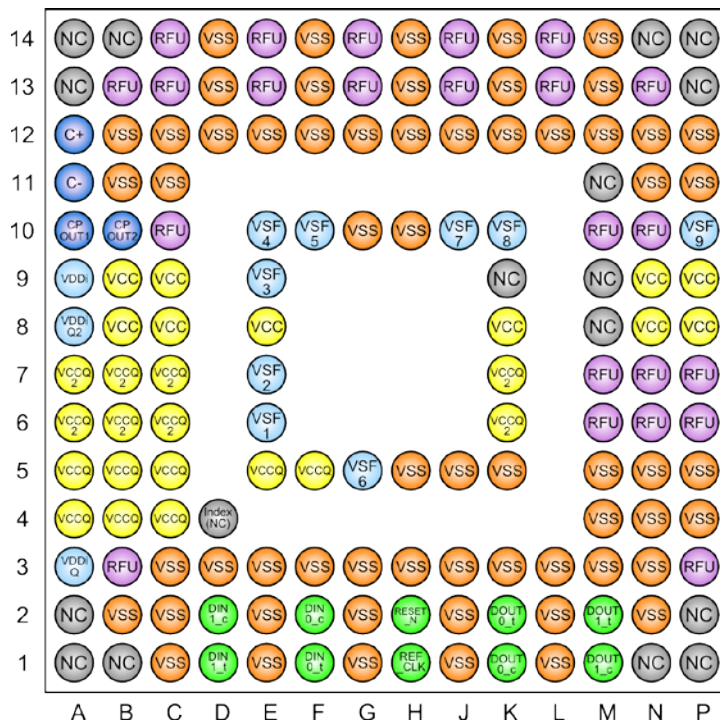


Figure 3 Pin Assignment (top view)

Table 1 Pin Description

| Name | Type | Pin Number | Description |
|-----------------------------|--------|--|--|
| VCC | Supply | B8-9, C8-9, E8, K8, N8-9, P8-9 | Supply voltage for NAND chips |
| VCCQ | Supply | A4-5, B4-5, C4-5, E5, F5, | Not used. Shall be connected to ground or left floating. |
| VCCQ2 | Supply | A6-7, B6-7, C6-7, K6-7 | Supply voltage for a memory controller, NAND I/O interface and the M-PHY interface |
| VDDi | - | A9 | Not used. Shall be left floating. If the capacitor is connected, it is necessary for the value to be 2.2uF or less. |
| VDDiQ | - | A3 | Not used. Shall be left floating. If the capacitor is connected, it is necessary for the value to be 2.2uF or less. |
| VDDiQ2 | Input | A8 | Input terminal to provide bypass capacitor for VCCQ2 internal regulator |
| VSS | Supply | B2, B11-12, C1-3, C11-12, D3, D12-14, E1-3, E12, F3, F12-14, G1-3, G10, G12, H3, H5, H10, H12-14, J1-3, J5, J12, K3, K5, K12-14, L1-3, L12, M3-5, M12-14, N2-5, N11-12, P4-5, P11-12 | Ground |
| RESET_N ^(Note 1) | Input | H2 | Input hardware reset signal |
| REF_CLK ^(Note 1) | Input | H1 | Input reference clock. When not active, this signal should be pull-down or driven low by the host SoC. |
| DIN0_t | Input | F1 | Downstream data lane 0 |
| DIN0_c | Input | F2 | Downstream data lane 0 |
| DIN1_t | Input | D1 | Downstream data lane 1 |
| DIN1_c | Input | D2 | Downstream data lane 1 |
| DOU0_t | Output | K2 | Upstream data lane 0 |
| DOU0_c | Output | K1 | Upstream data lane 0 |
| DOU1_t | Output | M2 | Upstream data lane 1 |
| DOU1_c | Output | M1 | Upstream data lane 1 |
| CPOUT1 | - | A10 | Not used. Shall be connected to ground or left floating. |
| CPOUT2 | - | B10 | Not used. Shall be connected to ground or left floating. |
| C+ | - | A12 | Not used. Shall be connected to ground or left floating. |
| C- | - | A11 | Not used. Shall be connected to ground or left floating. |
| VSFn | - | E6-7, E9-10, F10, G5, J10, K10, P10 | Shall be left floating |
| NC | - | A1, A2, A13, A14, B1, B14, D4, K9, M8, M9, M11, N1, N14, P1, P2, P13, P14 | Shall be connected to ground or left floating |
| RFU | - | B3, B13, C10, C13, C14, E13, E14, G13, G14, J13, J14, L13, L14, M6, M7, M10, N6, N7, N10, N13, P3, P6, P7 | Shall be left floating for future use |

Note:

- 1) Users need to input VCCQ (1.1 to 1.3V) based signals to RESET_N and REF_CLK to meet the electrical characteristics defined by UFS specification.

2.3. Part Number

Table 2 Product Part Number

| TOSHIBA Part Number | Density | NAND Flash Type | Package Size | Weight |
|---------------------|---------|------------------------------|------------------------------|--------------|
| THGAF8T1T83BAIR | 256GB | 8 x 256Gbit BiCS FLASH Gen.3 | 11.5mm x 13mm x 1.0mm (max.) | 0.26g (typ.) |

2.4. Operating Temperature

Table 3 Operating Temperature

| Characteristics | Min | Max | Unit |
|--|-------------------------|-------------------------|------|
| Operating Temperature(Tc) ^(Note 1, 4) | -25 ^(Note 2) | +85 ^(Note 3) | °C |

Note:

- 1) Operating Temperature is the package case surface temperature of the UFS device when UFS device is operating.
- 2) The minimum temperature should be based on the lowest temperature over the entire case surface.
- 3) The maximum temperature should be based on the highest temperature over the entire case surface.
- 4) Avoid locations where UFS devices may be exposed to water (wet, rain, dew condensation, etc).

2.5. Storage Temperature

Table 4 Storage Temperature

| Characteristics | Min | Max | Unit |
|--|-------------------------|-------------------------|------|
| Storage Temperature(Tc) ^(Note 1, 4) | -40 ^(Note 2) | +85 ^(Note 3) | °C |

Note:

- 1) Storage Temperature is the package case surface temperature of the UFS device when power is not supplied.
- 2) The minimum temperature should be based on the lowest temperature over the entire case surface.
- 3) The maximum temperature should be based on the highest temperature over the entire case surface.
- 4) Avoid locations where UFS devices may be exposed to water (wet, rain, dew condensation, etc).

2.6. Performance

HS-Gear with Rate B, Sequential Access (512KB access size)

Table 5 Performance

| TOSHIBA Part Number | Density | NAND Flash Type | HS-Gear | No. of Lane | Typ. Performance [MB/sec] | |
|---------------------|---------|------------------------------|---------|-------------|---------------------------|-------|
| | | | | | Read | Write |
| THGAF8T1T83BAIR | 256GB | 8 x 256Gbit BiCS FLASH Gen.3 | HS-G3 | 1 | 525 | 230 |
| | | | | 2 | 900 | 230 |

2.7. Power Supply

THGAF8T1T83BAIR supports 2 power supply of VCC and VCCQ2 and does not use VCCQ as power supply.

VCC = 2.7V to 3.6V

VCCQ2 = 1.7V to 1.95V

2.8. Operating Current (RMS)

Table 6 Maximum Operating Current

| TOSHIBA Part Number | Density | NAND Flash Type | HS-Gear | No. of Lane | Symbol | Max. Operating Current [mA] |
|---------------------|---------|------------------------------|---------|-------------|--------|-----------------------------|
| THGAF8T1T83BAIR | 256GB | 8 x 256Gbit BiCS FLASH Gen.3 | HS-G3 | 1 | Icc | 195 |
| | | | | | Iccq2 | 345 |
| | | | | 2 | Icc | 200 |
| | | | | | Iccq2 | 475 |

Note:

- 1) The measurement for max RMS current is done as average RMS current consumption over a period of 100ms
- 2) The conditions of maximum values are 85°C, VCC = 3.6V, VCCQ2 = 1.95V.

2.9. Sleep Mode Current

Table 7 Sleep Mode Current

| TOSHIBA Part Number | Density | NAND Flash Type | Symbol | Current [μA] | |
|---------------------|---------|------------------------------|-------------|---------------|---------------|
| | | | | Typ. (Note 1) | Max. (Note 2) |
| THGAF8T1T83BAIR | 256GB | 8 x 256Gbit BiCS FLASH Gen.3 | Iccqs2 | 270 | 2305 |
| | | | Iccs+Iccqs2 | 350 | 3505 |

Note:

- 1) The conditions of typical values are 25°C, VCC = 3.3V, VCCQ2 = 1.8V, UFS Sleep/M-PHY Hibern8.
- 2) The conditions of maximum values are 85°C, VCC = 3.6V, VCCQ2 = 1.95V, UFS Sleep/M-PHY Hibern8.

2.10. Product Architecture

Figure 4 illustrates the main functional blocks of the UFS module, and Table 8 shows the recommended capacitor values for power supplies.

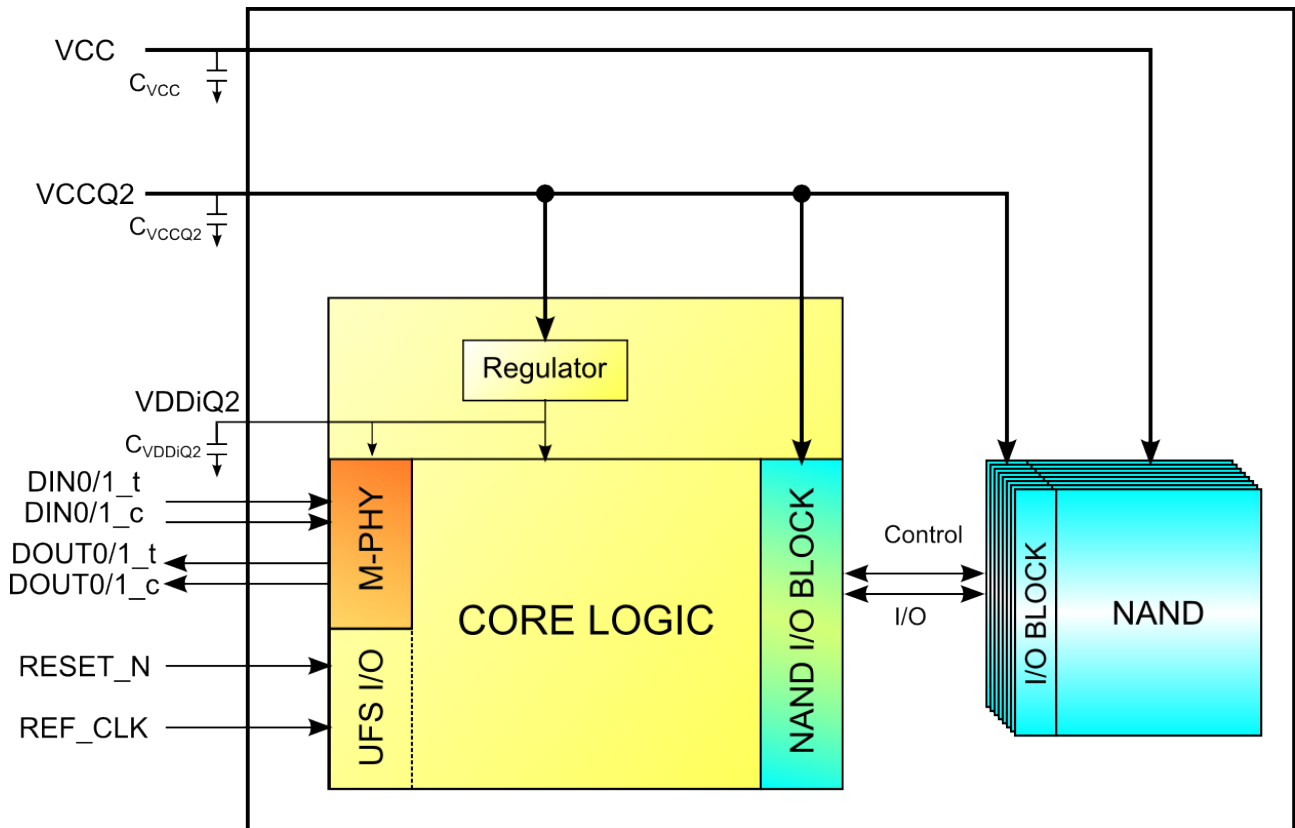


Figure 4 UFS module Block Diagram

Table 8 Recommended Capacitor Value for Power Supply

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|------------------|--------------|------|-----------|------|---------------|
| VDDiQ2 capacitor | C_{VDDiQ2} | 0.7 | 1 | 2.4 | μF |
| VCC capacitor | C_{VCC} | - | 2.2 + 0.1 | - | μF |
| VCCQ2 capacitor | C_{VCCQ2} | - | 2.2 + 0.1 | - | μF |

3. PRODUCT SPECIFICATIONS

3.1. Package Dimensions

P-VFBGA153-1113-0.50 (11.5mm x 13mm, H1.0mm max. package)

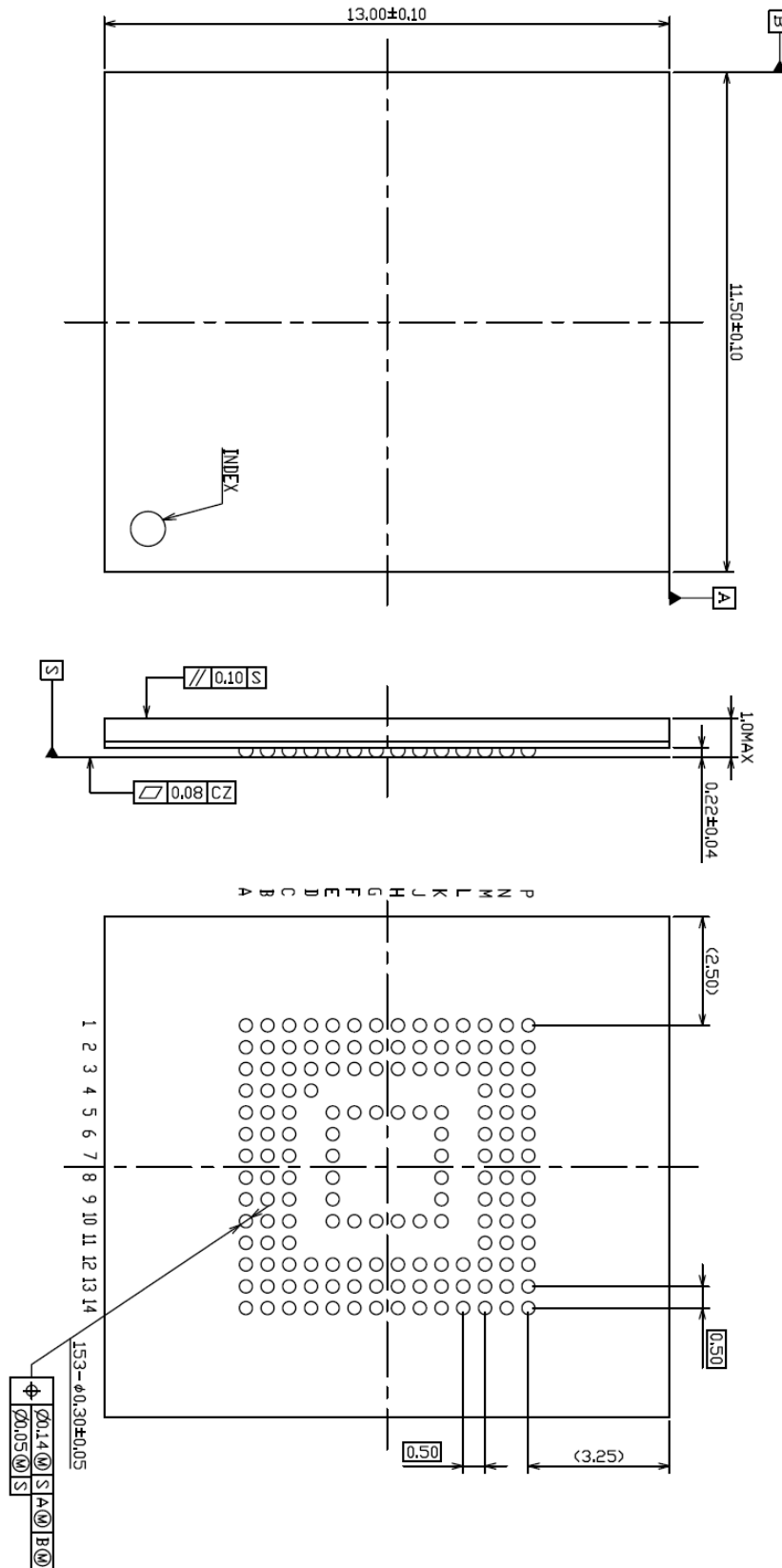


Figure 5 Package Dimensions (Unit: mm)

3.2. Density Specifications

Table 9 User Area Density

| TOSHIBA Part Number | Density | User Area Density [Bytes] |
|---------------------|---------|---------------------------|
| THGAF8T1T83BAIR | 256GB | 255,944,818,688 Byte |

Note:

- 1) User area density is reduced if enhanced user data area is defined.

3.3. M-PHY Attributes

THGAF8T1T83BAIR supports 2 lanes. All M-PHY Attributes of each lane are identified by Selector number and Attribute ID.

Table 10 Lane Number and Selector Number

| TX / RX | Selector |
|-----------|----------|
| Lane 0 TX | 0x0 |
| Lane 1 TX | 0x1 |
| Lane 0 RX | 0x4 |
| Lane 1 RX | 0x5 |

3.3.1. M-TX Capability Attributes

Table 11 M-TX Capability Attributes

| Attribute Name | Access | Attribute ID | Reset Value <small>(Note 1)</small> | Notes |
|--|--------|--------------|-------------------------------------|--|
| TX_HSMODE_Capability | R | 0x01 | 0x01 | Supports HS_MODE |
| TX_HSGEAR_Capability | R | 0x02 | 0x03 | Supports HS_G1 to HS_G3 (A/B) |
| TX_PWMG0_Capability | R | 0x03 | 0x00 | PWM_G0 is NOT supported |
| TX_PWMGEAR_Capability | R | 0x04 | 0x04 | Supports PWM_G1 to PWM_G4 |
| TX_Amplitude_Capability | R | 0x05 | 0x03 | Supports Small and Large Amplitude |
| TX_ExternalSYNC_Capability | R | 0x06 | 0x01 | Supports external SYNC pattern |
| TX_HS_Unterminated_LINE_Drive_Capability | R | 0x07 | 0x01 <small>(Note 2)</small> | Supports un-terminated line in HS-MODE |
| TX_LS_Terminated_LINE_Drive_Capability | R | 0x08 | 0x01 | Supports terminated line in LS-MODE |
| TX_Min_SLEEP_NoConfig_Time_Capability | R | 0x09 | 0x04 | Minimum time in SLEEP state is 4 SI |
| TX_Min_STALL_NoConfig_Time_Capability | R | 0x0A | 0x20 | Minimum time is STALL state is 32 SI |
| TX_Min_SAVE_Config_Time_Capability | R | 0x0B | 0xFA | Minimum reconfiguration time is 10 μs |
| TX_REF_CLOCK_SHARED_Capability | R | 0x0C | 0x01 | 1: YES |
| TX_PHY_MajorMinor_Release_Capability | R | 0x0D | 0x30 | Supports M-PHY ^R version 3.0 |
| TX_PHY_Editorial_Release_Capability | R | 0x0E | 0x03 | |
| TX_Hibern8Time_Capability | R | 0x0F | 0x01 | Minimum time in Hibern8 state is 100 μs |
| TX_Advanced_Granularity_Capability | R | 0x10 | 0x05 | Supports fine granularity with the step size of 16μs |
| TX_Advanced_Hibern8Time_Capability | R | 0x11 | 0x02 | |

| | | | | |
|------------------------------------|---|------|------|---------------------------------------|
| TX_HS_Equalizer_Setting_Capability | R | 0x12 | 0x03 | Supports de-emphasis of 3.5dB and 6dB |
|------------------------------------|---|------|------|---------------------------------------|

Note:

- 1) Reset value means the value after Link-up.
- 2) Terminated line in HS-MODE is recommended.

3.3.2. M-TX Configuration Attributes

Table 12 M-TX Configuration Attributes

| Attribute Name | Access ^(Note 1) | Attribute ID | Reset Value ^(Note 2) | Notes |
|--|----------------------------|--------------|---------------------------------|--|
| TX_MODE | R ^(Note 3) | 0x21 | 0x01 | 0x1: LS_MODE, 0x2: HS_MODE |
| TX_HSRATE_Series | R ^(Note 3) | 0x22 | 0x01 | 0x1: Rate A Series, 0x2: Rate B Series |
| TX_HSGEAR | R ^(Note 3) | 0x23 | 0x01 | 0x1: HS_G1, 0x2: HS_G2, 0x3: HS_G3 |
| TX_PWMGEAR | R ^(Note 3) | 0x24 | 0x01 | 0x1: PWM_G1, 0x2: PWM_G2, 0x3: PWM_G3, 0x4: PWM_G4 |
| TX_Amplitude | R/W | 0x25 | 0x02 | 0x1: Small Amplitude, 0x2: Large Amplitude |
| TX_HS_SlewRate | R/W | 0x26 | 0x00 | Slew Rate control is NOT supported |
| TX_SYNC_Source | R/W | 0x27 | 0x00 | 0: INTERNAL_SYNC, 1: EXTERNAL_SYNC |
| TX_HS_SYNC_LENGTH ^(Note 4) | R/W | 0x28 | - | Bit[7:6]: 0x0: FINE, 0x1: COARSE |
| | | | | Bit[5:0]: Valid range: 0x00 - 0x0F This value is 0x4F before Link-up, and is updated during Link-up depending on the capability of host and device. |
| TX_HS_PREPARE_LENGTH ^(Note 4) | R/W | 0x29 | - | Valid range: 0x6 - 0xF This value is 0x0F before Link-up, and is updated during Link-up depending on the capability of host and device. |
| TX_LS_PREPARE_LENGTH ^(Note 4) | R/W | 0x2A | - | Valid range: 0x9 - 0xF This value is 0x0A before Link-up, and is updated during Link-up depending on the capability of host and device. |
| TX_HIBERN8_Control | R ^(Note 3) | 0x2B | 0x00 | 0: EXIT, 1: ENTER This value is 1 before Link-up. |
| TX_LCC_Enable | R/W | 0x2C | 0x01 | 0: NO, 1: YES |
| TX_PWM_BURST_Closure_Extension | R/W | 0x2D | - | Valid range: 0x00 - 0xFF This value is 0x20 before Link-up, and is updated during Link-up depending on the capability of host and device |
| TX_BYPASS_8B10B_Enable | R/W | 0x2E | 0x00 | 0: FALSE, 1: TRUE |
| TX_DRIVER_POLARITY | R/W | 0x2F | 0x00 | 0: NORMAL, 1: INVERTED |
| TX_HS_Unterminated_LINE_Drive_Enable | R ^(Note 3) | 0x30 | 0x00 ^(Note 5) | 0: HS Terminated, 1: HS Un-terminated |
| TX_LS_Terminated_LINE_Drive_Enable | R ^(Note 3) | 0x31 | 0x00 | 0: LS Un-terminated, 1: LS Terminated |

| | | | | |
|---------------------------------|------------|------|------|---|
| TX_LCC_Sequencer | R (Note 3) | 0x32 | 0x00 | Bit[7]: LCC WRITE ATTRIBUTE 0: Not requested, 1: Requested |
| | | | | Bit[6:3]: 0x0 |
| | | | | Bit[2]: LCC READ-VEND-INFO 0: Not requested, 1: Requested |
| | | | | Bit[1]: LCC READ-MFG-INFO 0: Not requested, 1: Requested |
| | | | | Bit[0]: LCC READ-CAPABILITY 0: Not requested, 1: Requested |
| TX_Min_ActivateTime | R/W | 0x33 | 0x0F | Valid range: 0x00 - 0x0F |
| TX_Advanced_Granularity_Setting | R | 0x35 | 0x00 | Bit[2:1] step size b00: 4 µs, b01: 8 µs, b10: 16 µs, b11: 32 µs |
| | | | | Bit[0] Supports advanced granularity 0: No, 1: Yes |
| TX_Advanced_Granularity | R | 0x36 | 0x0F | Valid range: 0x1 - x0F |
| TX_HS_Equalizer_Setting | R/W | 0x37 | 0x00 | b000: No de-emphasis selected, b001: De-emphasis of 3.5 dB selected, b010: De-emphasis of 6 dB selected, b011 to b111: Reserved |

Note:

- 1) All writable Attributes are reset by power failure, H/W reset, Endpoint reset, or Link lost
- 2) Reset value means the value after Link-up
- 3) The attributes are write-protected by UniPro layer 1.5
- 4) The value has to be set equal or bigger than the value of RX side capability
- 5) Terminated line in HS-MODE is recommended.

3.3.3. M-RX Capability Attributes

Table 13 M-RX Capability Attributes

| Attribute Name | Access | Attribute ID | Reset Value (Note 1) | Notes |
|--|--------|--------------|----------------------|---|
| RX_HSMODE_Capability | R | 0x81 | 0x01 | Supports HS mode |
| RX_HSGEAR_Capability | R | 0x82 | 0x03 | Supports HS_G1 to HS_G3 (A/B) |
| RX_PWMG0_Capability | R | 0x83 | 0x00 | PWM-G0 is NOT supported |
| RX_PWMGEAR_Capability | R | 0x84 | 0x04 | Supports PWM_G1 to PWM_G4 |
| RX_HS_Unterminated_Capability | R | 0x85 | 0x01 (Note 2) | Supports un-terminated line in HS-MODE |
| RX_LS_Terminated_Capability | R | 0x86 | 0x01 | Supports terminated line in LS-MODE |
| RX_Min_SLEEP_NoConfig_Time_Capability | R | 0x87 | 0x0F | Minimum time in SLEEP state is 15 SI |
| RX_Min_STALL_NoConfig_Time_Capability | R | 0x88 | 0xBE | Minimum time is STALL state is 190 SI |
| RX_Min_SAVE_Config_Time_Capability | R | 0x89 | 0xFA | Minimum reconfiguration time is 10 µs |
| RX_REF_CLOCK_SHARED_Capability | R | 0x8A | 0x01 | 1: YES |
| RX_HS_G1_SYNC_LENGTH_Capability | R | 0x8B | 0x48 | SYNC_range: COARSE, SYNC_length: 8 |
| RX_HS_G1_PREPARE_LENGTH_Capability | R | 0x8C | 0x0F | HS-G1 PREPARE length is 15 |
| RX_LS_PREPARE_LENGTH_Capability | R | 0x8D | 0x0D | PWM-BURST PREPARE length is 13 Reset value of 10 at a host side is receivable before capability exchange. |
| RX_PWM_Burst_Closure_Length_Capability | R | 0x8E | 0x1F | Minimum burst closure time is 31 SI |

| | | | | |
|---|---|------|------|--|
| RX_Min_ActivateTime_Capability | R | 0x8F | 0x02 | Minimum activate time is 200 μ s |
| RX_PHY_MajorMinor_Release_Capability | R | 0x90 | 0x30 | Supported M-PHY ^R version 3.0 |
| RX_PHY_Editorial_Release_Capability | R | 0x91 | 0x03 | |
| RX_Hibern8Time_Capability | R | 0x92 | 0x01 | Minimum time in HIBERN8 state is 100 μ s |
| RX_HS_G2_SYNC_LENGTH_Capability | R | 0x94 | 0x49 | SYNC_range: COARSE, SYNC_length: 9 |
| RX_HS_G3_SYNC_LENGTH_Capability | R | 0x95 | 0x4A | SYNC_range: COARSE, SYNC_length: 10 |
| RX_HS_G2_PREPARE_LENGTH_Capability | R | 0x96 | 0x0F | HS-G2 PREPARE length is 15 |
| RX_HS_G3_PREPARE_LENGTH_Capability | R | 0x97 | 0x0F | HS-G3 PREPARE length is 15 |
| RX_Advanced_Granularity_Capability | R | 0x98 | 0x04 | |
| RX_Advanced_Hibern8Time_Capability | R | 0x99 | 0x01 | |
| RX_Advanced_Min_ActivateTime_Capability | R | 0x9A | 0x0A | |

Note:

- 1) Reset value means the value after Link-up.
- 2) Terminated line in HS-MODE is recommended.

3.3.4. M-RX Configuration Attributes

Table 14 M-RX Configuration Attributes

| Attribute Name | Access ^(Note 1) | Attribute ID | Reset Value ^(Note 2) | Notes |
|-----------------------------|----------------------------|--------------|---------------------------------|--|
| RX_MODE | R ^(Note 3) | 0xA1 | 0x01 | 0x01: LS_MODE, 0x02: HS_MODE |
| RX_HSRATE_Series | R ^(Note 3) | 0xA2 | 0x01 | 0x01: Rate A Series, 0x02: Rate B Series |
| RX_HSGEAR | R ^(Note 3) | 0xA3 | 0x01 | 0x01: HS_G1, 0x02: HS_G2, 0x03: HS_G3 |
| RX_PWMGEAR | R ^(Note 3) | 0xA4 | 0x01 | 0x01: PWM_G1, 0x02: PWM_G2, 0x03: PWM_G3, 0x04: PWM_G4 |
| RX_LS_Terminated_Enable | R ^(Note 3) | 0xA5 | 0x00 | 0: LS Un-terminated 1: LS Terminated |
| RX_HS_Unterminated_Enable | R ^(Note 3) | 0xA6 | 0x00 ^(Note 4) | 0: HS Terminated, 1: HS Un-terminated |
| RX_Enter_HIBERN8 | R ^(Note 3) | 0xA7 | 0x00 | 0: NO, 1: YES This value is 1 before Link-up. |
| RX_BYPASS_8B10B_Enable | R/W | 0xA8 | 0x00 | 0: Disabled, 1: Enabled |
| RX_Termination_Force_Enable | R/W | 0xA9 | 0x00 | 0: NO, 1: YES |

Note:

- 1) All writable Attributes are reset by power failure, H/W reset, Endpoint reset, or Link lost
- 2) Reset value means the value after Link-up.
- 3) The attributes are write-protected by UniPro layer 1.5
- 4) Terminated line in HS-MODE is recommended.

3.3.5. M-TX & M-RX Status Attributes

Table 15 M-TX & M-RX Status Attributes

| Attribute Name | Access | Attribute ID | Reset Value ^(Note 1) | Notes |
|----------------|--------|--------------|---------------------------------|---|
| TX_FSM_State | R | 0x41 | - | 0x0: DISABLED, 0x1: HIBERN8 0x2: SLEEP, 0x3: STALL 0x4: LS-BURST, 0x5: HS-BURST 0x6: LINE-CFG, 0x7: LINE-RESET |
| RX_FSM_State | R | 0xC1 | - | |

Note:

- 1) Reset value means the value after Link-up.

3.4. UniPro Attributes

3.4.1. UniPro L1.5 Attributes

Table 16 UniPro L1.5 Attributes

| Attribute Name | Access ^(Note 1) | Attribute ID | Reset Value ^(Note 2) | Notes |
|------------------------|----------------------------|--------------|---------------------------------|--|
| PA_PHY_Type | R | 0x1500 | 1 | M-PHY |
| PA_AvailTxDataLanes | R | 0x1520 | 0x2 | Available TX Data Lane is 2 |
| PA_AvailRxDataLanes | R | 0x1540 | 0x2 | Available RX Data Lane is 2 |
| PA_MinRxTrailingClocks | R | 0x1543 | 0x4D | The host should set own PA_TxTrailingClocks to bigger value than this value. |
| PA_TxHsG1SyncLength | R/W | 0x1552 | - | This value is 0x4F before Link-up, and is updated during Link-up depending on the capability of host and device. |
| PA_TxHsG1PrepareLength | R/W | 0x1553 | - | This value is 0x0F before Link-up, and is updated during Link-up depending on the capability of host and device. |
| PA_TxHsG2SyncLength | R/W | 0x1554 | - | This value is 0x4F before Link-up, and is updated during Link-up depending on the capability of host and device. |
| PA_TxHsG2PrepareLength | R/W | 0x1555 | - | This value is 0x0F before Link-up, and is updated during Link-up depending on the capability of host and device. |
| PA_TxHsG3SyncLength | R/W | 0x1556 | - | This value is 0x4F before Link-up, and is updated during Link-up depending on the capability of host and device. |
| PA_TxHsG3PrepareLength | R/W | 0x1557 | - | This value is 0x0F before Link-up, and is updated during Link-up depending on the capability of host and device. |
| PA_TxMk2Extension | R/W | 0x155A | - | This value is 0x00 before Link-up, and is updated during Link-up depending on the capability of host and device. |
| PA_PeerScrambling | R/W | 0x155B | - | This value is 0x00 before Link-up, and is updated during Link-up depending on the capability of host and device. |

| | | | | |
|---------------------------------|-----|--------|------|--|
| PA_TxSkip | R/W | 0x155C | - | This value is 0x00 before Link-up, and is updated during Link-up depending on the capability of host and device. |
| PA_TxSkipPeriod | R/W | 0x155D | 0xFA | |
| PA_Local_TX_LCC_Enable | R/W | 0x155E | 0x1 | |
| PA_Peer_TX_LCC_Enable | R/W | 0x155F | - | This value is 0x01 before Link-up, and is updated during Link-up depending on the capability of host and device. |
| PA_ActiveTxDataLanes | R/W | 0x1560 | 0x1 | Valid Range: 0x1 - 0x2 |
| PA_ConnectedTxDataLanes | R/W | 0x1561 | - | Valid Range: 0x0 - 0x2 This value is 0x02 before Link-up, and is updated during Link-up depending on the capability of host and device. |
| PA_TxTrailingClocks | R/W | 0x1564 | - | Valid Range: 0x00 - 0xFF (255 clocks) This value is 0x0FF before Link-up, and is updated during Link-up depending on the capability of host and device. |
| PA_TxPWRStatus | R | 0x1567 | - | 0x0: OFF_STATE 0x1: FAST_STATE 0x2: SLOW_STATE 0x3: HIBERNATE_STATE 0x4: SLEEP_STATE |
| PA_TxGear | R/W | 0x1568 | 0x1 | 0x1: PWM_G1, 0x2: PWM_G2 0x3: PWM_G3 0x4: PWM_G4 |
| PA_TxTermination | R/W | 0x1569 | 0 | 0: Un-terminated, 1: Terminated |
| PA_HSSeries ^(Note 3) | R/W | 0x156A | 0x1 | 0x1: Rate A Series, 0x2: Rate B Series |
| PA_PWRMode | R/W | 0x1571 | 0x55 | Bit[6:4] RX Power Mode 0x1: Fast_Mode 0x2: Slow_Mode 0x4: FastAuto_Mode 0x5: SlowAuto_Mode 0x7: UNCHANGED |
| | | | | Bit[4:0] TX Power Mode 0x1: Fast_Mode 0x2: Slow_Mode 0x4: FastAuto_Mode 0x5: SlowAuto_Mode 0x7: UNCHANGED |
| PA_ActiveRxDataLanes | R/W | 0x1580 | 0x1 | Valid Range: 0x1 - 0x2 |
| PA_ConnectedRxDataLanes | R/W | 0x1581 | - | Valid Range: 0x0 - 0x2 This value is 0x00 before Link-up, and is updated during Link-up depending on the capability of host and device. |
| PA_RxPWRStatus | R | 0x1582 | - | 0x0: OFF_STATE 0x1: FAST_STATE 0x2: SLOW_STATE 0x3: HIBERNATE_STATE 0x4: SLEEP_STATE |
| PA_RxGear | R/W | 0x1583 | 0x1 | 0x1: PWM_G1 0x2: PWM_G2 0x3: PWM_G3 0x4: PWM_G4 |
| PA_RxTermination | R/W | 0x1584 | 0 | 0: Un-terminated, 1: Terminated |
| PA_Scrambling | R/W | 0x1585 | 0 | |
| PA_MaxRxPWMGear | R | 0x1586 | - | This value is 0x01 before Link-up, and is updated during Link-up depending on the capability of host and device. |
| PA_MaxRxHSGear | R | 0x1587 | - | This value is 0x00 before Link-up, and is updated during Link-up depending on the capability of host and device. |
| PA_PACPRReqTimeout | R/W | 0x1590 | 0x3F | Valid range: 1 - 63 [ms] |

| | | | | |
|--------------------------------|-----|------------------|------------|--|
| PA_PACPRReqEoBTimeout | R/W | 0x1591 | 0xF | Valid range: 1 - 15 [ms] |
| PA_RemoteVerInfo | R | 0x15A0 | - | Undefined before link startup, after link startup depends on peer version information. |
| PA_LogicalLaneMap | R/W | 0x15A1 | - | Logical lane 0 is mapped to physical lane 0 (TX/RX) |
| PA_SleepNoConfigTime | R/W | 0x15A2 | - | Valid range: 0x1 (1 SI) - 0xF (15 SI) This value is 0x0F before Link-up, and is updated during Link-up depending on the capability of host and device. |
| PA_StallNoConfigTime | R/W | 0x15A3 | - | Valid range: 0x01 (1 SI) - 0xFF (255 SI) This value is 0xFF before Link-up, and is updated during Link-up depending on the capability of host and device. |
| PA_SaveConfigTime | R/W | 0x15A4 | - | Valid range: 0x01 (40 ns) - 0xFA (10 μ s) This value is 0xFA before Link-up, and is updated during Link-up depending on the capability of host and device. |
| PA_RxHSUnterminationCapability | R/W | 0x15A5 | - | 0: FALSE, 1: TRUE This value is 0x0 before Link-up, and is updated during Link-up depending on the capability of host and device. |
| PA_RxLSTerminationCapability | R/W | 0x15A6 | - | 0: FALSE, 1: TRUE This value is 0x0 before Link-up, and is updated during Link-up depending on the capability of host and device. |
| PA_Hibern8Time | R/W | 0x15A7 | - | Valid range: 0 - 10000 This value is 0x80 before Link-up, and is updated during Link-up depending on the capability of host and device. |
| PA_Tactivate | R/W | 0x15A8 | - | Valid range: 10 - 10000 This value is 0x10 before Link-up, and is updated during Link-up depending on the capability of host and device. |
| PA_LocalVerInfo | R/W | 0x15A9 | 0x0004 | Local version info This value is 0x0000 before Link-up, and is updated during Link-up depending on the capability of host and device. |
| PA_Granularity | R/W | 0x15AA | - | 0x1: 1 μ s, 0x2: 4 μ s, 0x3: 8 μ s, 0x4: 16 μ s, 0x5: 32 μ s, 0x6: 100 μ s This value is 0x06 before Link-up, and is updated during Link-up depending on the capability of host and device. |
| PA_MK2ExtensionGuardBand | R/W | 0x15AB | 0x0 | Valid range: 0 to 10000 |
| PA_PWRModeUserData[0 to11] | R/W | 0x15B0 to 0x15BB | All 0x0000 | Data to be sent within PACP_PWR_req and delivered to the remote DME. Valid range: 0x0000 - 0xFFFF |
| PA_PACPFramCount | R/W | 0x15C0 | - | Valid range: 0x00000000- 0xFFFFFFFF This counter value is incremented each time valid PACP frame is received. |
| PA_PACPErrorCount | R/W | 0x15C1 | 0x00000000 | Valid range: 0x00000000- 0xFFFFFFFF This counter value is incremented each time erroneous PACP frame is received. |
| PA_PHYTestControl | R/W | 0x15C2 | 0x00 | PHY Test Feature control register |
| | | | | Bit[4] TestPatternSelect Valid range: 0 - 1 |
| | | | | Bit[3] TestPatternTransmit Valid range: 0 - 1 |
| | | | | Bit[2] LineReset Valid range: 0 - 1 |
| | | | | Bit[1] CfgReady Valid range: 0 - 1 |
| | | | | Bit[0] ContBurst Valid range: 0 - 1 |

Note:

- 1) All writable Attributes are reset by power failure or H/W reset. All writable Attributes except for PA_PACPFramCount and PA_PACPErrorCount are reset by Endpoint reset or Link lost
- 2) Reset value means the value after Link-up
- 3) PA_HSSeries can be changed only when PA_PWRMode is Slow_Mode or SlowAuto_Mode

3.4.2. UniPro L2 Attributes

Table 17 UniPro L2 Attributes

| Attribute Name | Access ^(Note 1) | Attribute ID | Reset Value ^(Note 2) | Notes |
|---|----------------------------|--------------|---------------------------------|---|
| DL_TxPreemptionCap | R | 0x2000 | 1 | Supports preemption |
| DL_TC0TxMaxSDUSize | R | 0x2001 | 0x90 | TC0 Tx maximum SDU size is 144 symbols |
| DL_TC0RxInitCreditVal | R | 0x2002 | - | |
| DL_TC1TxMaxSDUSize | R | 0x2003 | 0x90 | TC1 Tx maximum SDU size is 144 symbols |
| DL_TC1RxInitCreditVal | R | 0x2004 | - | |
| DL_TC0TxBufferSize | R | 0x2005 | - | |
| DL_TC1TxBufferSize | R | 0x2006 | - | |
| DL_TC0TXFCThreshold | R/W | 0x2040 | 0x09 | Threshold is 9 * 32 Bytes Valid range: 0x01 - (DL_PeerTC0RxInitCreditVal - 1) |
| DL_FC0ProtectionTimeOutVal | R/W | 0x2041 | 0x1FFF | Valid range: 0x0000 - 0xFFFF (65535 μs) |
| DL_TC0ReplayTimeOutVal | R/W | 0x2042 | 0xFFFF | Valid range: 0x0000 - 0xFFFF (65535 μs) |
| DL_AFC0ReqTimeOutVal | R/W | 0x2043 | 0x7FFF | Valid range: 0x0000 - 0xFFFF (65535 μs) |
| DL_AFC0CreditThreshold | R/W | 0x2044 | 0x00 | Valid range: 0x00 - 0x1F |
| DL_TC0OutAckThreshold | R/W | 0x2045 | 0 | Valid range: 0x0 - 0xF (15 Frames) |
| DL_PeerTC0Present ^(Note 3) | R | 0x2046 | - | |
| DL_PeerTC0RxInitCreditVal ^(Note 3) | R | 0x2047 | - | |
| DL_TC1TXFCThreshold | R/W | 0x2060 | 0x09 | TC1 is not supported |
| DL_FC1ProtectionTimeOutVal | R/W | 0x2061 | 0x1FFF | Valid range: 0x0000 - 0xFFFF (65535 μs) |
| DL_TC1ReplayTimeOutVal | R/W | 0x2062 | 0xFFFF | Valid range: 0x0000 - 0xFFFF (65535 μs) |
| DL_AFC1ReqTimeOutVal | R/W | 0x2063 | 0x7FFF | Valid range: 0x0000 - 0xFFFF (65535 μs) |
| DL_AFC1CreditThreshold | R/W | 0x2064 | 0x00 | TC1 is not supported |
| DL_TC1OutAckThreshold | R/W | 0x2065 | 0 | Valid range: 0x0 - 0xF (15 Frames) |
| DL_PeerTC1Present ^(Note 3) | R | 0x2066 | - | |
| DL_PeerTC1RxInitCreditVal ^(Note 3) | R | 0x2067 | - | |

Note:

- 1) All writable Attributes are reset by power failure, H/W reset, Endpoint reset, or Link lost
- 2) Reset value means the value after Link-up
- 3) The value depends on host capability

3.4.3. UniPro L3 Attributes

Table 18 UniPro L3 Attributes

| Attribute Name | Access ^(Note 1) | Attribute ID | Reset Value ^(Note 2) | Notes |
|-------------------|----------------------------|--------------|---------------------------------|---------------------------|
| N_DeviceID | R/W | 0x3000 | 0x01 | Local Device ID is 0x01 |
| N_DeviceID_valid | R/W | 0x3001 | 0x01 | 1: TRUE |
| N_TC0TxMaxSDUSize | R | 0x3020 | 0x0111 | Maximum size is 273 Bytes |
| N_TC1TxMaxSDUSize | R | 0x3021 | 0x0111 | Maximum size is 273 Bytes |

Note:

- 1) All writable Attributes are reset by power failure, H/W reset, Endpoint reset, or Link lost
- 2) Reset value means the value after Link-up

3.4.4. UniPro L4 Attributes

Table 19 UniPro L4 Attributes

| Attribute Name | Access ^(Note 1) | Attribute ID | Reset Value ^(Note 2) | Notes |
|--|----------------------------|--------------|---------------------------------|---|
| T_NumCPorts | R | 0x4000 | 0x0001 | 1 CPort |
| T_NumTestFeatures | R | 0x4001 | 0x0001 | 1 Test Feature |
| T_ConnectionState | R/W | 0x4020 | 1 | 1: Connected |
| T_PeerDeviceID | R/W | 0x4021 | 0x00 | DeviceID of the peer device (host) is 0 |
| T_PeerCPortID | R/W | 0x4022 | 0x000 | CPortID of the peer CPort is 0 |
| T_TrafficClass | R/W | 0x4023 | 0 | Traffic class is 0 |
| T_ProtocolID | R/W | 0x4024 | 0x0000 | Reserved for future use |
| T_CPortFlags | R/W | 0x4025 | 0x6 | Valid range: 0x6 |
| T_TxTokenValue ^(Note 3) | R/W | 0x4026 | 0x20 | Value of a E2E FC Token transmitted is 32 Bytes Valid range: 0x20 - 0x1000000 (powers of 2 only) |
| T_RxTokenValue ^(Note 3) | R/W | 0x4027 | 0x20 | Value of a E2E FC Token received is 32 Bytes Valid range: 0x20 - 0x1000000 (powers of 2 only) |
| T_LocalBufferSpace ^(Note 3) | R/W | 0x4028 | 0x00000000 | |
| T_PeerBufferSpace ^(Note 3) | R/W | 0x4029 | 0x00000000 | |
| T_CreditsToSend ^(Note 3) | R/W | 0x402A | 0x00000000 | |
| T_CPortMode | R/W | 0x402B | 0x1 | 0x1:CPORT_APPLICATION 0x2:CPORT_UNDER_TEST |
| T_TC0TxMaxSDUSize | R | 0x4060 | 0x110 | Maximum transmit payload (SDU) size per Segment for TC0 is 272 Bytes |
| T_TC1TxMaxSDUSize | R | 0x4061 | 0x110 | Maximum transmit payload (SDU) size per Segment for TC1 is 272 Bytes |

Note:

- 1) All writable Attributes are reset by power failure, H/W reset, Endpoint reset, or Link lost
- 2) Reset value means the value after Link-up
- 3) These values are invalid because UFS specifaion doesn't support End-to-End flow control. Don't change these values.

3.4.5. UniPro DME DDB L1 Attributes

Table 20 UniPro DME DDB L1 Attributes

| Attribute Name | Access | Attribute ID | Reset Value ^(Note 1) | Notes |
|--------------------------|--------|--------------|---------------------------------|---|
| DME_DDBL1_Revision | R | 0x5000 | 0x10 | DDB v1.0 |
| DME_DDBL1_Level | R | 0x5001 | 0x01 | DDB L2 is not supported |
| DME_DDBL1_DeviceClass | R | 0x5002 | 0x0002 | The Device Class ID of the DME User |
| DME_DDBL1_ManufacturerID | R | 0x5003 | 0x0126 | Manufacturer ID of the DME User |
| DME_DDBL1_ProductID | R | 0x5004 | 0x0001 | The Manufacturer's internal product ID of the DME User is 0 |
| DME_DDBL1_Length | R | 0x5005 | 0x0000 | The length of any DDB Level 2 data is 0 |

Note:

- 1) Reset value means the value after Link-up

3.4.6. UniPro TstSrc/TstDst Attributes

Table 21 UniPro TstSrc/TstDst Attributes

| Attribute Name | Access ^(Note 1) | Attribute ID | Reset Value ^(Note 2) | Notes |
|---|----------------------------|--------------|---------------------------------|---|
| T_TstCPortID | R/W | 0x4080 | 0x00 | The ID of the CPort-under-test is 0 |
| T_TstSrcOn | R/W | 0x4081 | 0x00 | 0: FALSE, 1: TRUE |
| T_TstSrcPattern | R/W | 0x4082 | 0x00 | 0: Saw tooth |
| T_TstSrcIncrement | R/W | 0x4083 | 0x01 | Increment value is 1 Valid range: 0x00 - 0xFF |
| T_TstSrcMessageSize | R/W | 0x4084 | 0x0100 | The size of each generated Message Valid range: 0x0001 - 0xFFFF (65535 Bytes) |
| T_TstSrcMessageCount | R/W | 0x4085 | 0x0100 | The number of Messages generated Valid range: 0x0000 - 0xFFFF (65535 Messages) |
| T_TstSrcInterMessageGap | R/W | 0x4086 | 0x0000 | If non-zero, the gap time between two Messages. Valid range: 0x0000 - 0xFFFF (65535 μ s) |
| T_TstDstOn | R/W | 0x40A1 | 0x00 | 0: FALSE, 1: TRUE |
| T_TstDstErrorDetectionEnable | R/W | 0x40A2 | 0x00 | 0: FALSE, 1: TRUE |
| T_TstDstPattern | R/W | 0x40A3 | 0x00 | 0: Saw tooth |
| T_TstDstIncrement | R/W | 0x40A4 | 0x01 | Increment value is 1 Valid range: 0x00 - 0xFF |
| T_TstDstMessageCount | R/W | 0x40A5 | 0x0000 | Number of received Messages Valid range: 0x0000 - 0xFFFF (65535 Messages) |
| T_TstDstMessageOffset | R/W | 0x40A6 | 0x0000 | Offset of error from start of Message Valid range: 0x0000 - 0xFFFF (65535 Bytes) |
| T_TstDstMessageSize | R/W | 0x40A7 | 0x0100 | The expected size of incoming Message Valid range: 0x0000 - 0xFFFF (65535 Bytes) |
| T_TstDstFCCredits ^(Note 3) | R/W | 0x40A8 | 0x0000 | Valid range: 0x1 - 0xFFFFFFFF (4294967295 Bytes) |
| T_TstDstInterFCTokenGap ^(Note 3) | R/W | 0x40A9 | 0x0000 | Valid range: 0x0000 - 0xFFFF (65535 μ s) |

| | | | | |
|--|-----|--------|--------|---|
| T_TstDstInitialFCCredits ^(Note 3) | R/W | 0x40AA | 0x0000 | Valid range: 0x1 - 0xFFFFFFFF (4294967295 Bytes) |
| T_TstDstErrorCode | R/W | 0x40AB | 0x00 | 0x0: NO_ERROR 0x1: FRAGMENT_CORRUPT 0x2: INVALID_MSG_SIZE 0x3: UNEXPECTED_BYTE_VALUE |

Note:

- 1) All writable Attributes are reset by power failure, H/W reset, Endpoint reset, or Link lost
- 2) Reset value means the value after Link-up
- 3) These values are invalid because UFS specifaion doesn't support End-to-End flow control. Don't change these values.

3.5. UPIU Transaction codes

THGAF8T1T83BAIR supports following UPIU transaction codes. Each command is used with corresponding UPIU. It is not allowed to use undefined codes. Refer to UFS specification for more detail information.

Table 22 UPIU Transaction Codes

| Initiator To Target | T+Opcode | Target to Initiator | T+Opcode |
|-------------------------|----------|--------------------------|----------|
| NOP Out | 0x00 | NOP In | 0x20 |
| Command | 0x01 | Response | 0x21 |
| Data Out | 0x02 | Data In | 0x22 |
| Task Management Request | 0x04 | Task Management Response | 0x24 |
| Reserved | 0x11 | Ready To Transfer | 0x31 |
| Query Request | 0x16 | Query Response | 0x36 |
| Reserved | 0x1F | Reject UPIU | 0x3F |

3.6. UFS Descriptors

The UFS modules support following UFS descriptors defined in UFS specification. Please refer to UFS specification for more detail information.

Table 23 UFS Descriptor TYPE and IDN

| DESCRIPTOR TYPE | DESCRIPTOR IDN | DESCRIPTOR TYPE | DESCRIPTOR IDN |
|-----------------|----------------|-----------------|----------------|
| DEVICE | 0x00 | STRING | 0x05 |
| CONFIGURATION | 0x01 | RFU | 0x06 |
| UNIT | 0x02 | GEOMETRY | 0x07 |
| RFU | 0x03 | POWER | 0x08 |
| INTERCONNECT | 0x04 | DEVICE HEALTH | 0x09 |

3.6.1. Device Descriptor

Table 24 Device Descriptor

| OFFSET | SIZE | NAME | VALUE | DESCRIPTION |
|--------|------|-----------------------|------------|--|
| 0x00 | 1 | bLength | 0x40 | Size of this descriptor |
| 0x01 | 1 | bDescriptorIDN | 0x00 | Device Descriptor Type Identifier |
| 0x02 | 1 | bDevice | 0x00 | 0x00: Device |
| 0x03 | 1 | bDeviceClass | 0x00 | 0x00: Mass Storage |
| 0x04 | 1 | bDeviceSubClass | 0x00 | 0x00: Embedded Bootable |
| 0x05 | 1 | bProtocol | 0x00 | 0x00: SCSI |
| 0x06 | 1 | bNumberLU | User Conf. | Valid range: 0x00 - 0x1F (Default value: 0x00) |
| 0x07 | 1 | bNumberWLU | 0x04 | 0x04: 4 Well known logical Units exist |
| 0x08 | 1 | bBootEnable | User Conf. | 0x00: Boot feature disabled (Default) 0x01: Bootable feature enabled |
| 0x09 | 1 | bDescrAccessEn | User Conf. | 0x00: Device Descriptor access disabled (Default) 0x01: Device Descriptor access enabled |
| 0x0A | 1 | bInitPowerMode | User Conf. | 0x00: UFS-Sleep Mode 0x01: Active Mode (Default) |
| 0x0B | 1 | bHighPriorityLUN | User Conf. | 0x00 - 0x07: Configured LUN has high priority 0x7F: All logical units have the same priority (Default) |
| 0x0C | 1 | bSecureRemovalType | User Conf. | Secure Removal Type Valid range: 0x00, 0x03 |
| 0x0D | 1 | bSecurityLU | 0x01 | 0x01: RPMB |
| 0x0E | 1 | bBackgroundOpsTermLat | 0x0F | 0x0F: 150ms |
| 0x0F | 1 | bInitActiveICCLLevel | User Conf. | bInitActiveICCLLevel defines the bActiveICCLLevel value after power on or reset. Valid range: 0x00 to 0x0F. (Default value: 0x00) |
| 0x10 | 2 | wSpecVersion | 0x0210 | Specification version |
| 0x12 | 2 | wManufactureDate | - | Manufacturing Date |
| 0x14 | 1 | iManufacturerName | 0x01 | Manufacturer Name |
| 0x15 | 1 | iProductName | 0x02 | Product Name |
| 0x16 | 1 | iSerialNumber | 0x03 | Serial Number |
| 0x17 | 1 | iOemID | 0x04 | OEM ID |
| 0x18 | 2 | wManufacturerID | 0x0198 | Manufacturer ID |
| 0x1A | 1 | bUD0BaseOffset | 0x10 | Unit Descriptor 0 Base Offset |
| 0x1B | 1 | bUDConfigPLength | 0x10 | Unit Descr. Config. Param. Length Total size of the configurable Unit Descriptor parameters. |
| 0x1C | 1 | bDeviceRTTCap | 0x02 | RTT Capability of device |
| 0x1D | 2 | wPeriodicRTCUpdate | User Conf. | Frequency and method of Real-Time Clock update. (Default value: 0x0000) |
| 0x1F | 1 | bUFSFeaturesSupport | 0x03 | |
| 0x20 | 1 | bFFUTimeout | 0x01 | |
| 0x21 | 1 | bQueueDepth | 0x40 | Shared Queue Depth = 64 |
| 0x22 | 2 | wDeviceVersion | 0x0000 | |
| 0x24 | 1 | bNumSecureWPArea | 0x20 | |
| 0x25 | 4 | dPSAMaxDataSize | 0x00100000 | |
| 0x29 | 1 | bPSAStateTimeout | 0x0D | 819.2 ms |
| 0x2A | 1 | iProductRevisionLevel | 0x05 | |
| 0x2B | 21 | Reserved | - | |

3.6.2. UFS Geometry Descriptor

Table 25 UFS Geometry Descriptor

| OFFSET | SIZE | NAME | VALUE | DESCRIPTION |
|--------|------|--------------------------------|---------------------|---|
| 0x00 | 1 | bLength | 0x48 | Byte of device geometry information |
| 0x01 | 1 | bDescriptorIDN | 0x07 | Geometry Descriptor Type Identifier |
| 0x02 | 1 | bMediaTechnology | 0x00 | Reserved |
| 0x03 | 1 | Reserved | - | |
| 0x04 | 8 | qTotalRawDeviceCapacity | 0x00000000_1DCBC000 | Device capacity |
| 0x0C | 1 | bMaxNumberLU | 0x01 | 32 Logical Units |
| 0x0D | 4 | dSegmentSize | 0x00002000 | 4M Bytes |
| 0x11 | 1 | bAllocationUnitSize | 0x01 | Value expressed in number of Segments |
| 0x12 | 1 | bMinAddrBlockSize | 0x08 | 4K Bytes |
| 0x13 | 1 | bOptimalReadBlockSize | 0x80 | 64K Bytes |
| 0x14 | 1 | bOptimalWriteBlockSize | 0x80 | 64K Bytes |
| 0x15 | 1 | bMaxInBufferSize | 0x08 | 4K Bytes |
| 0x16 | 1 | bMaxOutBufferSize | 0x08 | 4K Bytes |
| 0x17 | 1 | bRPMB_ReadWriteSize | 0x40 | Maximum 64 of RPMB frames allowed in Security Protocol In/Out |
| 0x18 | 1 | bDynamicCapacityResourcePolicy | 0x01 | |
| 0x19 | 1 | bDataOrdering | 0x00 | 0x00: out-of-order data transfer is not supported by the device |
| 0x1A | 1 | bMaxContextIDNumber | 0x05 | Maximum 5 contexts are available |
| 0x1B | 1 | bSysDataTagUnitSize | 0x00 | Tag Unit Size is 4K Bytes |
| 0x1C | 1 | bSysDataTagResSize | 0x00 | System Data Tag Resource Size is 0.1 % |
| 0x1D | 1 | bSupportedSecRTypes | 0x09 | Supported Secure Removal Types |
| 0x1E | 2 | wSupportedMemoryTypes | 0x801F | Supported Memory Types Normal memory type System code memory type Non-Persistent memory type Enhanced memory type 1 Enhanced memory type 2 RPMB memory type |
| 0x20 | 4 | dSystemCodeMaxNAllocU | 0x0000EE5E | Max Number of Allocation Units for the System Code memory type |
| 0x24 | 2 | wSystemCodeCapAdjFac | 0x0300 | Capacity Adjustment Factor for the System Code memory type |
| 0x26 | 4 | dNonPersistMaxNAllocU | 0x0000EE5E | Max Number of Allocation Units for the Non-Persistent memory type |
| 0x2A | 2 | wNonPersistCapAdjFac | 0x0300 | Capacity Adjustment Factor for the Non-Persistent memory type |
| 0x2C | 4 | dEnhanced1MaxNAllocU | 0x0000EE5E | Max Number of Allocation Units for the Enhanced memory type 1 |
| 0x30 | 2 | wEnhanced1CapAdjFac | 0x0300 | Capacity Adjustment Factor for the Enhanced memory type 1 |
| 0x32 | 4 | dEnhanced2MaxNAllocU | 0x00000060 | Max Number of Allocation Units for the Enhanced memory type 2 |
| 0x36 | 2 | wEnhanced2CapAdjFac | 0x0300 | Capacity Adjustment Factor for the Enhanced memory type 2 |
| 0x38 | 4 | dEnhanced3MaxNAllocU | 0x00000000 | Enhanced memory type 3 is not supported |
| 0x3C | 2 | wEnhanced3CapAdjFac | 0x0000 | |
| 0x3E | 4 | dEnhanced4MaxNAllocU | 0x00000000 | Enhanced memory type 4 is not supported |

| | | | | |
|------|---|--------------------------|--------|----------|
| 0x42 | 2 | wEnhanced4CapAdjFac | 0x0000 | |
| 0x44 | 4 | dOptimalLogicalBlockSize | 0x00 | 4K Bytes |

3.6.3. Unit Descriptor

THGAF8T1T83BAIR has 32 Unit Descriptors. All default values except for bUnitIndex are the same.

Table 26 Unit Descriptor

| OFFSET | SIZE | NAME | VALUE | DESCRIPTION |
|-----------|------|--------------------------|--------------|--|
| 0x00 | 1 | bLength | 0x23 | Size of this descriptor |
| 0x01 | 1 | bDescriptorIDN | 0x02 | Unit Descriptor Type Identifier |
| 0x02 | 1 | bUnitIndex | 0x00 to 0x1F | Unit Index |
| 0x03 | 1 | bLUEnable | User Conf. | 0x00: Logical Unit disabled (Default) 0x01: Logical Unit enabled |
| 0x04 | 1 | bBootLunID | User Conf. | 0x00: Not bootable (Default) 0x01: Boot LU A 0x02: Boot LU B |
| 0x05 | 1 | bLUWriteProtect | User Conf. | 0x00: LU not write protected (Default) 0x01: LU write protected when fPowerOnWPEn =1 0x02: LU permanently write protected when fPermanentWPEn =1 |
| 0x06 | 1 | bLUQueueDepth | 0x00 | |
| 0x07 | 1 | bPSASensitive | 0x00 or 0x01 | 0x00: Enhanced memory type1 or type2 (Default) 0x01: Normal Memory Type |
| 0x08 | 1 | bMemoryType | User Conf. | 0x00: Normal Memory (Default) 0x01: System code memory type 0x02: Non-Persistent memory type 0x03: Enhanced memory type 1 0x04: Enhanced memory type 2 |
| 0x09 | 1 | bDataReliability | User Conf. | 0x00: The logical unit is not protected (Default) 0x01: The logical unit is protected |
| 0x0A | 1 | bLogicalBlockSize | User Conf. | Value range: 0x0C (Default) - 0x0Fh |
| 0x0B | 8 | qLogicalBlockCount | User Conf. | This value can be configured setting the dNumAllocUnits parameter of the Configuration Descriptor. Default value: 0x00000000_00000000 |
| 0x13 | 4 | dEraseBlockSize | 0x00000000 | Erase Block Size |
| 0x17 | 1 | bProvisioningType | User Conf. | 0x00:Thin Provisioning is disabled (Default) 0x02:Thin Provisioning is enabled and TPRZ = 0 0x03:Thin Provisioning is enabled and TPRZ = 1 |
| 0x18:0x1F | 8 | qPhyMemResourceCount | User Conf. | qPhyMemResourceCount shall be equal to qLogicalBlockCount initially |
| 0x20 | 2 | wContextCapabilities | User Conf. | Bit[6:4]: LARGE_UNIT_MAX_MULTIPLIER_M1 Default value: b000 Bit[3:0]: MaxContextID Default value: b000 |
| 0x22 | 1 | bLargeUnitGranularity_M1 | 0x00 | Large Unit Granularity = 1MB * (bLargeUnitGranularity_M1 + 1) |

3.6.4. RPMB Unit Descriptor

Table 27 RPMB Unit Descriptor

| OFFSET | SIZE | NAME | VALUE | DESCRIPTION |
|---------------|------|----------------------|-------------------------|--|
| 0x00 | 1 | bLength | 0x23 | Size of this descriptor |
| 0x01 | 1 | bDescriptorIDN | 0x02 | Unit Descriptor Type Identifier |
| 0x02 | 1 | bUnitIndex | 0xC4 | Unit Index |
| 0x03 | 1 | bLUEnable | 0x01 | 0x01: Logical Unit enabled |
| 0x04 | 1 | bBootLunID | 0x00 | 0x00: Not bootable |
| 0x05 | 1 | bLUWriteProtect | 0x00 | 0x00: LU not write protected |
| 0x06 | 1 | bLUQueueDepth | 0x01 | |
| 0x07 | 1 | bPASSensitive | 0x00 | |
| 0x08 | 1 | bMemoryType | 0x0F | 0x0F: RPMB Memory Type |
| 0x09 | 1 | bRPMBRegionEnable | 0x00 | Multi Region RPMB defined in the next version of UFS specification |
| 0x0A | 1 | bLogicalBlockSize | 0x08 | 0x08: 256 Byte Logical Block Size |
| 0x0B | 8 | qLogicalBlockCount | 0x00000000 _00010000 | 16MB |
| 0x13 | 1 | bRPMBRegion0Size | 0x80 | Multi Region RPMB defined in the next version of UFS specification |
| 0x14 | 1 | bRPMBRegion1Size | 0x00 | |
| 0x15 | 1 | bRPMBRegion2Size | 0x00 | |
| 0x16 | 1 | bRPMBRegion3Size | 0x00 | |
| 0x17 | 1 | bProvisioningType | 0x00 | 0x00:Thin Provisioning is disabled |
| 0x18: 0x1F | 8 | qPhyMemResourceCount | 0x00000000 _00010000 | 16MB |
| 0x20: 0x22 | 3 | Reserved | - | |

3.6.5. Power Parameters Descriptor

Table 28 Power Parameters Descriptor

| OFFSET | SIZE | NAME | VALUE | DESCRIPTION |
|--------|------|-------------------------|--------|---|
| 0x00 | 1 | bLength | 0x62 | Size of this descriptor |
| 0x01 | 1 | bDescriptorIDN | 0x08 | Power Parameters Descriptor Type Identifier |
| 0x02 | 2 | wActiveICCLevelsVCC(0) | 0x80C8 | 2 byte maximum VCC current value for each of the 16 active current consumption levels starting with level 0 |
| 0x04 | 2 | wActiveICCLevelsVCC(1) | 0x80C8 | |
| 0x06 | 2 | wActiveICCLevelsVCC(2) | 0x80C8 | |
| 0x08 | 2 | wActiveICCLevelsVCC(3) | 0x80C8 | |
| 0x0A | 2 | wActiveICCLevelsVCC(4) | 0x80C8 | |
| 0x0C | 2 | wActiveICCLevelsVCC(5) | 0x80C8 | |
| 0x0E | 2 | wActiveICCLevelsVCC(6) | 0x80C8 | |
| 0x10 | 2 | wActiveICCLevelsVCC(7) | 0x80C8 | |
| 0x12 | 2 | wActiveICCLevelsVCC(8) | 0x80C8 | |
| 0x14 | 2 | wActiveICCLevelsVCC(9) | 0x80C8 | |
| 0x16 | 2 | wActiveICCLevelsVCC(10) | 0x80C8 | |
| 0x18 | 2 | wActiveICCLevelsVCC(11) | 0x80C8 | |

| | | | | |
|------|---|---------------------------|--------|---|
| 0x1A | 2 | wActiveICCLevelsVCC(12) | 0x80C8 | |
| 0x1C | 2 | wActiveICCLevelsVCC(13) | 0x80C8 | |
| 0x1E | 2 | wActiveICCLevelsVCC(14) | 0x80C8 | |
| 0x20 | 2 | wActiveICCLevelsVCC(15) | 0x80C8 | |
| 0x22 | 2 | wActiveICCLevelsVCCQ(0) | 0x0000 | 2 byte maximum VCCQ current value for each of the 16 active current consumption levels starting with level 0 |
| 0x24 | 2 | wActiveICCLevelsVCCQ(1) | 0x0000 | |
| 0x26 | 2 | wActiveICCLevelsVCCQ(2) | 0x0000 | |
| 0x28 | 2 | wActiveICCLevelsVCCQ(3) | 0x0000 | |
| 0x2A | 2 | wActiveICCLevelsVCCQ(4) | 0x0000 | |
| 0x2C | 2 | wActiveICCLevelsVCCQ(5) | 0x0000 | |
| 0x2E | 2 | wActiveICCLevelsVCCQ(6) | 0x0000 | |
| 0x30 | 2 | wActiveICCLevelsVCCQ(7) | 0x0000 | |
| 0x32 | 2 | wActiveICCLevelsVCCQ(8) | 0x0000 | |
| 0x34 | 2 | wActiveICCLevelsVCCQ(9) | 0x0000 | |
| 0x36 | 2 | wActiveICCLevelsVCCQ(10) | 0x0000 | |
| 0x38 | 2 | wActiveICCLevelsVCCQ(11) | 0x0000 | |
| 0x3A | 2 | wActiveICCLevelsVCCQ(12) | 0x0000 | |
| 0x3C | 2 | wActiveICCLevelsVCCQ(13) | 0x0000 | |
| 0x3E | 2 | wActiveICCLevelsVCCQ(14) | 0x0000 | |
| 0x40 | 2 | wActiveICCLevelsVCCQ(15) | 0x0000 | |
| 0x42 | 2 | wActiveICCLevelsVCCQ2(0) | 0x8190 | 2 byte maximum VCCQ2 current value for each of the 16 active current consumption levels starting with level 0 |
| 0x44 | 2 | wActiveICCLevelsVCCQ2(1) | 0x8190 | |
| 0x46 | 2 | wActiveICCLevelsVCCQ2(2) | 0x8190 | |
| 0x48 | 2 | wActiveICCLevelsVCCQ2(3) | 0x8190 | |
| 0x4A | 2 | wActiveICCLevelsVCCQ2(4) | 0x8190 | |
| 0x4C | 2 | wActiveICCLevelsVCCQ2(5) | 0x8190 | |
| 0x4E | 2 | wActiveICCLevelsVCCQ2(6) | 0x8190 | |
| 0x50 | 2 | wActiveICCLevelsVCCQ2(7) | 0x8190 | |
| 0x52 | 2 | wActiveICCLevelsVCCQ2(8) | 0x8190 | |
| 0x54 | 2 | wActiveICCLevelsVCCQ2(9) | 0x8190 | |
| 0x56 | 2 | wActiveICCLevelsVCCQ2(10) | 0x8190 | |
| 0x58 | 2 | wActiveICCLevelsVCCQ2(11) | 0x8190 | |
| 0x5A | 2 | wActiveICCLevelsVCCQ2(12) | 0x8190 | |
| 0x5C | 2 | wActiveICCLevelsVCCQ2(13) | 0x8190 | |
| 0x5E | 2 | wActiveICCLevelsVCCQ2(14) | 0x8190 | |
| 0x60 | 2 | wActiveICCLevelsVCCQ2(15) | 0x8190 | |

3.6.6. Device Health Descriptor

Table 29 Device Health Descriptor

| OFFSET | SIZE | NAME | MDV | DESCRIPTION |
|--------|------|---------------------|------|---|
| 0x00 | 1 | bLength | 0x25 | Size of this descriptor |
| 0x01 | 1 | bDescriptorIDN | 0x09 | Device Health Descriptor Type Identifier |
| 0x02 | 1 | bPreEOLInfo | 0x01 | Pre End of Life Information This field provides indication about device life time reflected by average reserved blocks. 0x00: Not defined 0x01: Normal (Default) 0x02: Warning 0x03: Critical Others: Reserved |
| 0x03 | 1 | bDeviceLifeTimeEstA | 0x01 | This field provides indication about current averaged program erase cycle of memory relative to its maximum estimated capability. It is calculated by vendor specific method A. 0x00: Not defined 0x01: 0% - 10% device life time used (Default) 0x02: 10% - 20% device life time used 0x03: 20% - 30% device life time used 0x04: 30% - 40% device life time used 0x05: 40% - 50% device life time used 0x06: 50% - 60% device life time used 0x07: 60% - 70% device life time used 0x08: 70% - 80% device life time used 0x09: 80% - 90% device life time used 0x0A: 90% - 100% device life time used 0x0B: Exceeded its maximum estimated device life time Others: Reserved |
| 0x04 | 1 | bDeviceLifeTimeEstB | 0x01 | This field provides indication about current averaged program erase cycle of memory relative to its maximum estimated capability. It is calculated by vendor specific method B. 0x00: Not defined 0x01: 0% - 10% device life time used (Default) 0x02: 10% - 20% device life time used 0x03: 20% - 30% device life time used 0x04: 30% - 40% device life time used 0x05: 40% - 50% device life time used 0x06: 50% - 60% device life time used 0x07: 60% - 70% device life time used 0x08: 70% - 80% device life time used 0x09: 80% - 90% device life time used 0x0A: 90% - 100% device life time used 0x0B: Exceeded its maximum estimated device life time Others: Reserved |
| 0x05 | 32 | Reserved | - | |

3.6.7. Interconnect Descriptor

Table 30 Interconnect Descriptor

| OFFSET | SIZE | NAME | VALUE | DESCRIPTION |
|--------|------|------------------|--------|--|
| 0x00 | 1 | bLength | 0x06 | Size of this descriptor |
| 0x01 | 1 | bDescriptorIDN | 0x04 | Interconnect Descriptor Type Identifier |
| 0x02 | 2 | bcdUniproVersion | 0x0160 | MIPI Unipro SM Release Version Number |
| 0x04 | 2 | bcdMphyVersion | 0x0300 | MIPI M-PHY ^R Release Version Number |

3.6.8. Manufacturer Name String Descriptor

Table 31 Manufacture Name String Descriptor

| OFFSET | SIZE | NAME | VALUE | DESCRIPTION |
|--------|------|----------------|--------|-----------------------------------|
| 0x00 | 1 | bLength | 0x12 | Size of this descriptor |
| 0x01 | 1 | bDescriptorIDN | 0x05 | String Descriptor Type Identifier |
| 0x02 | 2 | UC | 0x0054 | Unicode string character("T") |
| 0x04 | 2 | UC | 0x004F | Unicode string character("O") |
| 0x06 | 2 | UC | 0x0053 | Unicode string character("S") |
| 0x08 | 2 | UC | 0x0048 | Unicode string character("H") |
| 0x0A | 2 | UC | 0x0049 | Unicode string character("I") |
| 0x0C | 2 | UC | 0x0042 | Unicode string character("B") |
| 0x0E | 2 | UC | 0x0041 | Unicode string character("A") |
| 0x10 | 2 | UC | 0x0020 | Unicode string character(" ") |

3.6.9. Product Name String Descriptor

Table 32 Product Name String Descriptor

| OFFSET | SIZE | NAME | VALUE | DESCRIPTION |
|--------|------|----------------|--------|-----------------------------------|
| 0x00 | 1 | bLength | 0x22 | Size of this descriptor |
| 0x01 | 1 | bDescriptorIDN | 0x05 | String Descriptor Type Identifier |
| 0x02 | 2 | UC | 0x0054 | Unicode string character("T") |
| 0x04 | 2 | UC | 0x0048 | Unicode string character("H") |
| 0x06 | 2 | UC | 0x0047 | Unicode string character("G") |
| 0x08 | 2 | UC | 0x0041 | Unicode string character("A") |
| 0x0A | 2 | UC | 0x0046 | Unicode string character("F") |
| 0x0C | 2 | UC | 0x0038 | Unicode string character("8") |
| 0x0E | 2 | UC | 0x0054 | Unicode string character("T") |
| 0x10 | 2 | UC | 0x0031 | Unicode string character("1") |
| 0x12 | 2 | UC | 0x0054 | Unicode string character("T") |
| 0x14 | 2 | UC | 0x0038 | Unicode string character("8") |
| 0x16 | 2 | UC | 0x0033 | Unicode string character("3") |
| 0x18 | 2 | UC | 0x0042 | Unicode string character("B") |
| 0x1A | 2 | UC | 0x0041 | Unicode string character("A") |
| 0x1C | 2 | UC | 0x0049 | Unicode string character("I") |
| 0x1E | 2 | UC | 0x0052 | Unicode string character("R") |
| 0x20 | 2 | UC | 0x0042 | Unicode string character("B") |

3.6.10. OEM ID String Descriptor

Table 33 OEM ID String Descriptor

| OFFSET | SIZE | NAME | VALUE | DESCRIPTION |
|--------|------|----------------|-------|--|
| 0x00 | 1 | bLength | 0xFE | Size of this descriptor |
| 0x01 | 1 | bDescriptorIDN | 0x05 | String Descriptor Type Identifier |
| 0x02 | 252 | UC | 0x00 | Unicode string character Data size is (bLength-2) |

3.6.11. Serial Number String Descriptor

Table 34 Serial Number String Descriptor

| OFFSET | SIZE | NAME | VALUE | DESCRIPTION |
|--------|------|----------------|------------|---|
| 0x00 | 1 | bLength | 0x16 | Size of this descriptor |
| 0x01 | 1 | bDescriptorIDN | 0x05 | String Descriptor Type Identifier |
| 0x02 | 14 | UC[0-6] | - (Note 1) | Unicode string character Valid range: 0x0030 - 0x0039, 0x0041 - 0x005A |
| 0x10 | 6 | UC[7-9] | 0x0000 | NULL |

Note:

- 1) Toshiba Memory supports 7 UNICODE characters unique serial number of each device.

3.6.12. Product Revision Level String Descriptor

Table 35 Product Revision Level String Descriptor

| OFFSET | SIZE | NAME | VALUE | DESCRIPTION |
|--------|------|----------------|--------|-----------------------------------|
| 0x00 | 1 | bLength | 0x0A | Size of this descriptor |
| 0x01 | 1 | bDescriptorIDN | 0x05 | String Descriptor Type Identifier |
| 0x02 | 2 | UC | 0x0030 | Unicode string character("0100") |
| 0x04 | 2 | UC | 0x0031 | |
| 0x06 | 2 | UC | 0x0030 | |
| 0x08 | 2 | UC | 0x0030 | |

3.7. UFS Flags

Table 36 UFS Flags

| IDN | NAME | TYPE | DEFAULT VALUE | DESCRIPTION |
|------|-----------------------------|-------------------------|---------------|--|
| 0x00 | Reserved | - | - | |
| 0x01 | fDeviceInit | Read/Set Only | 0 | 0: Device initialization completed or not started yet. 1: Device initialization in progress. |
| 0x02 | fPermanentWPEn | Read/Write Once | 0 | 0: Permanent write protection disabled 1: Permanent write protection enabled |
| 0x03 | fPowerOnWPEn | Read/ Power on reset | 0 | 0: Power on write protection disabled. 1: Power on write protection enabled. |
| 0x04 | fBackgroundOpsEn | Read/Volatile | 1 | 0: Device initiated background ops. is disabled 1: Device initiated background ops. is enabled |
| 0x05 | fDeviceLifeSpanModeEn | Read/Volatile | 0 | 0: Device Life Span Mode is disabled. |
| 0x06 | fPurgeEnable | Write Only/Volatile | 0 | 0: Purge operation is disabled. 1: Purge operation is enabled. |
| 0x07 | Reserved | - | - | |
| 0x08 | fPhyResourceRemoval | Read/Persistent | 0 | Physical Resource Removal |
| 0x09 | fBusyRTC | Read Only | 0 | 0 : Device is not executing internal operation related to RTC |
| 0x0A | Reserved | - | - | |
| 0x0B | fPermanentlyDisableFwUpdate | Read/Write Once | 0 | 0: The UFS device firmware may be modified 1: The UFS device shall permanently disallow future firmware updates to the UFS device |

3.8. UFS Attributes

Table 37 UFS Attributes

| IDN | NAME | TYPE | SIZE [Byte] | DEFAULT VALUE | DESCRIPTION |
|------|---------------------------------------|-----------------|-------------|---------------|--|
| 0x00 | bBootLunEn | Read/Persistent | 1 | 0x00 | 0x00: Boot disabled 0x01: Enabled boot from Boot LU A 0x02: Enabled boot from Boot LU B |
| 0x01 | Reserved | - | - | - | |
| 0x02 | bCurrentPowerMode ^(Note 1) | Read Only | 1 | 0x10 | Current Power Mode |
| 0x03 | bActiveICCLLevel | Read/Volatile | 1 | 0x00 | Active ICC Level |
| 0x04 | bOutOfOrderDataEn | Read/Write Once | 1 | 0x00 | 0x00: Out-of-order data transfer is disabled. |
| 0x05 | bBackgroundOpStatus | Read Only | 1 | 0x00 | Background Operations Status |
| 0x06 | bPurgeStatus | Read Only | 1 | 0x00 | Purge Operation Status |
| 0x07 | bMaxDataInSize | Read/Persistent | 1 | 0x08 | 512Bytes * 8 = 4Kbytes |
| 0x08 | bMaxDataOutSize | Read/Persistent | 1 | 0x08 | 512Bytes * 8 = 4Kbytes |
| 0x09 | dDynCapNeeded | Read Only | 4 | 0x00000000 | Dynamic Capacity Needed |
| 0x0A | bRefClkFreq | Read/Persistent | 1 | 0x01 | 0x00: 19.2MHz 0x01: 26MHz 0x02: 38.4MHz 0x03: 52MHz |
| 0x0B | bConfigDescrLock | Read/Write Once | 1 | 0x00 | 0x00: Configuration Descriptor and OEM ID String Descriptor not locked 0x01: Configuration Descriptor and OEM ID String Descriptor locked |
| 0x0C | bMaxNumOfRTT | Read/Persistent | 1 | 0x02 | 0x02: Maximum 2 RTTs |
| 0x0D | wExceptionEventControl | Read/Volatile | 2 | 0x0000 | Bit[2]: URGENT_BKOPS_EN |
| | | | | | Bit[1]: SYSPPOOL_EVENT_EN |
| | | | | | Bit[0]: DYNCAP_EVENT_EN |
| 0x0E | wExceptionEventStatus | Read Only | 2 | 0x0000 | Bit[2]: URGENT_BKOPS |
| | | | | | Bit[1]: SYSPPOOL_EXHAUSTED |
| | | | | | Bit[0]: DYNCAP_NEEDED |
| 0x0F | dSecondsPassed | Write Only | 4 | 0x00000000 | Bit[31:0]: Seconds passed from TIME BASELINE |
| 0x10 | wContextConf | Read/Volatile | 2 | 0x0000 | INDEX specifies the LU number. SELECTOR specifies the Context ID within the LU. |
| 0x14 | bDeviceFFUStatus | Read Only | 1 | 0x00 | Device FFU Status 0x00: No information 0x01: Successful microcode update 0x02: Microcode corruption error 0x03: Internal error 0x04: Microcode version mismatch 0x05 - 0xFE: Reserved 0xFF: General Error |
| 0x15 | bPSAState | Read/Persistent | 1 | 0x00 | Product State Awareness State 0x00: Off 0x01: Pre-soldering 0x02: Loading Complete 0x03: Soldered |
| 0x16 | dPSADataSize | Read/Persistent | 4 | 0x00100000 | The amount of data that the host plans to load to all logical units with bPSASensitive set to 1 |

Note:

- 1) bCurrentPowerMode value after initialization changes depending on the value of bInitPowerMode.

3.9. UFS SCSI Commands

Table 38 UFS SCSI Commands

| Command name | Opcode | Command name | Opcode |
|--------------------|--------|------------------------|--------|
| FORMAT UNIT | 0x04 | SECURITY PROTOCOL IN | 0xA2 |
| INQUIRY | 0x12 | SECURITY PROTOCOL OUT | 0xB5 |
| MODE SELECT (10) | 0x55 | SEND DIAGNOSTIC | 0x1D |
| MODE SENSE (10) | 0x5A | START STOP UNIT | 0x1B |
| PRE-FETCH (10) | 0x34 | SYNCHRONIZE CACHE (10) | 0x35 |
| PRE-FETCH (16) | 0x90 | SYNCHRONIZE CACHE (16) | 0x91 |
| READ (6) | 0x08 | TEST UNIT READY | 0x00 |
| READ (10) | 0x28 | UNMAP | 0x42 |
| READ (16) | 0x88 | VERIFY (10) | 0x2F |
| READ BUFFER | 0x3C | WRITE (6) | 0x0A |
| READ CAPACITY (10) | 0x25 | WRITE (10) | 0x2A |
| READ CAPACITY (16) | 0x9E | WRITE (16) | 0x8A |
| REPORT LUNS | 0xA0 | WRITE BUFFER | 0x3B |
| REQUEST SENSE | 0x03 | - | - |

3.10. Mode Pages

3.10.1. Control Mode Page

Table 39 Control Mode Page

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----|----------------------------------|---|----------------------|---------------|---------------|----------------------|------------|---------------|
| 0 | PS = 1b | SPF = 0b | PAGE CODE = 001010b | | | | | |
| 1 | PAGE LENGTH = 0x0A | | | | | | | |
| 2 | TST = 000b | | | TMF_ONLY = 0b | DPICZ = 0b | D_SENSE = 0b | GLTSD = 0b | RLEC = 0b |
| 3 | QUEUE ALGORITHM MODIFIER = 0001b | | | | NUAR = 0b | QERR = 00b | | Obsolete = 0b |
| 4 | VS = 0b | RAC = 0b | UA_INTLCK_CTRL = 00b | | SWP = 0b | Obsolete = 000b | | |
| 5 | ATO = 0b | TAS = 0b | ATMPE = 0b | RWWP = 0b | Reserved = 0b | AUTOLOAD MODE = 000b | | |
| 6 | Obsolete = 0x0000 | | | | | | | |
| 7 | | | | | | | | |
| 8 | (MSB) | BUSY TIMEOUT PERIOD = 0xFFFF | | | | | | (LSB) |
| 9 | | | | | | | | |
| 10 | (MSB) | EXTENDED SELF-TEST COMPLETION TIME = 0x0000 | | | | | | (LSB) |
| 11 | | | | | | | | |

3.10.2. Read-Write Error Recovery Mode Page

Table 40 Read-Write Error Recovery Mode Page

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----|--------------------------|------------------------------|---------------------|---------|----------|----------|----------------------------|----------|
| 0 | PS = 0b | SPF = 0b | PAGE CODE = 000001b | | | | | |
| 1 | PAGE LENGTH = 0x0A | | | | | | | |
| 2 | AWRE = 1b | ARRE = 0b | TB = 0b | RC = 0b | EER = 0b | PER = 0b | DTE = 0b | DCR = 0b |
| 3 | READ RETRY COUNT = 0x06 | | | | | | | |
| 4 | Obsolete = 0x00 | | | | | | | |
| 5 | Obsolete = 0x00 | | | | | | | |
| 6 | Obsolete = 0x00 | | | | | | | |
| 7 | TPERE = 0b | Reserved = 00000b | | | | | Restricted for MMC-6 = 00b | |
| 8 | WRITE RETRY COUNT = 0x03 | | | | | | | |
| 9 | Reserved = 0x00 | | | | | | | |
| 10 | (MSB) | RECOVERY TIME LIMIT = 0xFFFF | | | | | | (LSB) |
| 11 | | | | | | | | |

3.10.3. Caching Mode Page

Table 41 Caching Mode Page

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|------|--|--|--------------------|-----------------------|----------------------------------|----------------|---------|-------------|--|
| Byte | | | | | | | | | |
| 0 | PS = 0b | SPF = 0b | PAGE CODE = 01000b | | | | | | |
| 1 | PAGE LENGTH = 0x12 | | | | | | | | |
| 2 | IC = 0b | ABPF = 0b | CAP = 0b | DISC = 0b | SIZE = 0b | WCE = 1b | MF = 0b | RCD = 0b | |
| 3 | DEMAND READ RETENTION PRIORITY = 0000b | | | | WRITE RETENTION PRIORITY = 0000b | | | | |
| 4 | (MSB) | DISABLE PRE-FETCH TRANSFER LENGTH = 0x0000 | | | | | | (LSB) | |
| 5 | | | | | | | | | |
| 6 | (MSB) | MINIMUM PRE-FETCH = 0x0000 | | | | | | (LSB) | |
| 7 | | | | | | | | | |
| 8 | (MSB) | MAXIMUM PRE-FETCH = 0x0000 | | | | | | (LSB) | |
| 9 | | | | | | | | | |
| 10 | (MSB) | MAXIMUM PRE-FETCH CEILING = 0x0000 | | | | | | (LSB) | |
| 11 | | | | | | | | | |
| 12 | FSW = 0b | LBCSS = 0b | DRA = 0b | Vendor Specific = 00b | | Reserved = 00b | | NV_DIS = 0b | |
| 13 | NUMBER OF CACHE SEGMENTS = 0x00 | | | | | | | | |
| 14 | (MSB) | CACHE SEGMENT SIZE = 0x0000 | | | | | | (LSB) | |
| 15 | | | | | | | | | |
| 16 | Reserved = 0x00 | | | | | | | | |
| 17 | | | | | | | | | |
| 18 | Obsolete = 0x00 0000 | | | | | | | | |
| 19 | | | | | | | | | |

3.11. Standard INQUIRY data

Table 42 Standard INQUIRY data format

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|----------------------------------|------------------------|-----------------|--|------------------------------|-------------------|------------------|-----------------|
| Byte | | | | | | | | |
| 0 | PERIPHERAL QUALIFIER = 000b | | | PERIPHERAL DEVICE TYPE 00000b ^(Note 1) 11110b ^(Note 2) | | | | |
| 1 | RMB = 0b | Reserved = 000000b | | | | | | |
| 2 | VERSION = 0x06 | | | | | | | |
| 3 | Obsolete = 0b | Obsolete = 0b | NORMACA = 0b | HISUP = 0b | RESPONSE DATA FORMAT = 0010b | | | |
| 4 | ADDITIONAL LENGTH (n-4) = 0x1F | | | | | | | |
| 5 | SCCS = 0b | ACC = 0b | TPGS = 00b | | 3PC = 0b | Reserved = 00b | | PROTECT = 0b |
| 6 | Obsolete = 0b | ENC SERV = 0b | VS = 0b | MULTIP = 0b | Obsolete = 0b | Obsolete = 0b | Obsolete = 0b | ADDR16 = 0b |
| 7 | Obsolete = 0b | Obsolete = 0b | WBUS16 = 0b | SYNC = 0b | Obsolete = 0b | Obsolete = 0b | CMDQUE = 1b | VS = 0b |
| 8 | (MSB) | VENDOR IDENTIFICATION | | | | | | (LSB) |
| 15 | = 0x544F5348 49424120 (TOSHIBA) | | | | | | | (LSB) |
| 16 | (MSB) | PRODUCT IDENTIFICATION | | | | | | (LSB) |
| 31 | (see Table 43) | | | | | | (LSB) | |
| 32 | (MSB) | PRODUCT REVISION LEVEL | | | | | | (LSB) |
| 35 | = 0x30313030 (0100) | | | | | | (LSB) | |

Note:

- 1) Direct Access Device for logical unit (non well known)
- 2) Well known logical unit

Table 43 PRODUCT IDENTIFICATION

| TOSHIBA Part Number | Density | PRODUCT IDENTIFICATION |
|---------------------|---------|---------------------------------------|
| THGAF8T1T83BAIR | 256GB | 0x54484741 46385431 54383342 41495242 |

3.12. Vital Product Data

Table 44 Supported Vital Product Data

| Vital Product Data Name | Page Code | Well Known LU | Except Well Known LU |
|------------------------------|-----------|---------------|----------------------|
| Supported VPD Pages | 0x00 | Supported | Supported |
| Device Identification | 0x83 | Supported | Supported |
| Mode Page Policy | 0x87 | Not supported | Supported |
| Unit Serial Number | 0x80 | Supported | Supported |
| Block Limits | 0xB0 | Not supported | Supported |
| Block Device Characteristics | 0xB1 | Supported | Supported |
| Thin Provisioning | 0xB2 | Not supported | Supported |

3.12.1. Supported VPD Pages

Table 45 Supported VPD Pages (Well Known LU)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----|--|---|---|---------------------------------|---|---|---|---|
| 0 | PERIPHERAL QUALIFIER = 000b | | | PERIPHERAL DEVICE TYPE = 11110b | | | | |
| 1 | PAGE CODE = 0x00 | | | | | | | |
| 2 | PAGE LENGTH = 0x0004 | | | | | | | |
| 3 | | | | | | | | |
| 4 | Supported VPD Pages = 0x00 | | | | | | | |
| 5 | Unit Serial Number = 0x80 | | | | | | | |
| 6 | Device Identification = 0x83 | | | | | | | |
| 7 | Block Device Characteristics VPD page = 0xB1 | | | | | | | |

Table 46 Supported VPD Pages (Except Well Known LU)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----|--|---|---|---------------------------------|---|---|---|---|
| 0 | PERIPHERAL QUALIFIER = 000b | | | PERIPHERAL DEVICE TYPE = 00000b | | | | |
| 1 | PAGE CODE = 0x00 | | | | | | | |
| 2 | PAGE LENGTH = 0x0007 | | | | | | | |
| 3 | | | | | | | | |
| 4 | Supported VPD Pages = 0x00 | | | | | | | |
| 5 | Unit Serial Number = 0x80 | | | | | | | |
| 6 | Device Identification = 0x83 | | | | | | | |
| 7 | Mode Page Policy = 0x87 | | | | | | | |
| 8 | Block Limits VPD page = 0xB0 | | | | | | | |
| 9 | Block Device Characteristics VPD page = 0xB1 | | | | | | | |
| 10 | Thin Provisioning VPD page = 0xB2 | | | | | | | |

3.12.2. Device Identification

Table 47 Device Identification

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----|---------------------------------|-------------|---|--|-------------------------|---|---|---|
| 0 | PERIPHERAL QUALIFIER = 000b | | | PERIPHERAL DEVICE TYPE 00000b ^(Note 1) 11110b ^(Note 2) | | | | |
| 1 | PAGE CODE = 0x83 | | | | | | | |
| 2 | PAGE LENGTH = 0x000C | | | | | | | |
| 3 | | | | | | | | |
| 4 | PROTOCOL IDENTIFIER = 0x0 | | | | CODE SET = 0x1 | | | |
| 5 | PIV=0b | Reserved=0b | ASSOCIATION 00b ^(Note 1) 10b ^(Note 2) | | DESIGNATOR TYPE = 0010b | | | |
| 6 | Reserved = 0x00 | | | | | | | |
| 7 | DESIGNATOR LENGTH = 0x08 | | | | | | | |
| 8 | DESIGNATOR = 0x0000390000000000 | | | | | | | |
| 9 | | | | | | | | |
| 10 | | | | | | | | |
| 11 | | | | | | | | |

Note:

- 1) Direct Access Device for logical unit (non well known)
- 2) Well known logical unit

3.12.3. Mode Page Policy

Table 48 Mode Page Policy

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----|-----------------------------|-------------------|----------------------------|---------------------------------|---|---|------------------------|---|
| 0 | PERIPHERAL QUALIFIER = 000b | | | PERIPHERAL DEVICE TYPE = 00000b | | | | |
| 1 | PAGE CODE = 0x87 | | | | | | | |
| 2 | PAGE LENGTH = 0x000C | | | | | | | |
| 3 | | | | | | | | |
| 4 | Reserved = 00b | | POLICY PAGE CODE = 001010b | | | | | |
| 5 | POLICY SUB PAGE CODE = 0x00 | | | | | | | |
| 6 | MLUS = 0b | Reserved = 00000b | | | | | MODE PAGE POLICY = 01b | |
| 7 | Reserved = 0x00 | | | | | | | |
| 8 | Reserved = 00b | | POLICY PAGE CODE = 000001b | | | | | |
| 9 | POLICY SUB PAGE CODE = 0x00 | | | | | | | |
| 10 | MLUS = 0b | Reserved = 00000b | | | | | MODE PAGE POLICY = 01b | |

| | | | |
|----|-----------------------------|----------------------------|------------------------|
| 11 | Reserved = 0x00 | | |
| 12 | Reserved = 00b | POLICY PAGE CODE = 001000b | |
| 13 | POLICY SUB PAGE CODE = 0x00 | | |
| 14 | MLUS = 0b | Reserved = 00000b | MODE PAGE POLICY = 01b |
| 15 | Reserved = 0x00 | | |

3.12.4. Unit Serial Number

Table 49 Unit Serial Number

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-----------------------------|---|---|--|---|---|---|---|
| Byte | | | | | | | | |
| 0 | PERIPHERAL QUALIFIER = 000b | | | PERIPHERAL DEVICE TYPE 00000b (Note 1) 11110b (Note 2) | | | | |
| 1 | PAGE CODE = 0x80 | | | | | | | |
| 2 | PAGE LENGTH = 0x000A | | | | | | | |
| 3 | | | | | | | | |
| 4 | PRODUCT SERIAL NUMBER[0] | | | | | | | |
| 5 | PRODUCT SERIAL NUMBER[1] | | | | | | | |
| 6 | PRODUCT SERIAL NUMBER[2] | | | | | | | |
| 7 | PRODUCT SERIAL NUMBER[3] | | | | | | | |
| 8 | PRODUCT SERIAL NUMBER[4] | | | | | | | |
| 9 | PRODUCT SERIAL NUMBER[5] | | | | | | | |
| 10 | PRODUCT SERIAL NUMBER[6] | | | | | | | |
| 11 | PRODUCT SERIAL NUMBER[7] | | | | | | | |
| 12 | PRODUCT SERIAL NUMBER[8] | | | | | | | |
| 13 | PRODUCT SERIAL NUMBER[9] | | | | | | | |

Note:

- 1) Direct Access Device for logical unit (non well known)
- 2) Well known logical unit

3.12.5. Block Limits

Table 50 Block Limits

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--|--|---|---------------------------------|---|---|---|---|
| Byte | | | | | | | | |
| 0 | PERIPHERAL QUALIFIER = 000b | | | PERIPHERAL DEVICE TYPE = 00000b | | | | |
| 1 | PAGE CODE = 0xB0 | | | | | | | |
| 2 | PAGE LENGTH = 0x003C | | | | | | | |
| 3 | | | | | | | | |
| 4 | Reserved = 0x00 | | | | | | | |
| 5 | MAXIMUM COMPARE AND WRITE LENGTH = 0x00 | | | | | | | |
| 6 | OPTIMAL TRANSFER LENGTH GRANULARITY = 0x0010 *In case of Logical Block Size is default value, 4KB. | | | | | | | |
| 7 | | | | | | | | |
| 8 | MAXIMUM TRANSFER LENGTH = 0x0000 0000 | | | | | | | |
| ... | | | | | | | | |
| 11 | | | | | | | | |
| 12 | OPTIMAL TRANSFER LENGTH = 0x0000 0010 *In case of Logical Block Size is default value, 4KB. | | | | | | | |
| ... | | | | | | | | |
| 15 | | | | | | | | |
| 16 | MAXIMUM PREFETCH XDREAD XDWRITE TRANSFER LENGTH = 0x0000 0000 | | | | | | | |
| ... | | | | | | | | |
| 19 | | | | | | | | |
| 20 | MAXIMUM UNMAP LBA COUNT = qLogicalBlockCount ^(Note 1) | | | | | | | |
| ... | | | | | | | | |
| 23 | | | | | | | | |
| 24 | MAXIMUM UNMAP BLOCK DESCRIPTOR COUNT = 0x0000 0001 | | | | | | | |
| ... | | | | | | | | |
| 27 | | | | | | | | |
| 28 | OPTIMAL UNMAP GRANULARITY = 0x0000 0001 | | | | | | | |
| ... | | | | | | | | |
| 31 | | | | | | | | |
| 32 | UGAVALID = 0b | UNMAP GRANULARITY ALIGNMENT = 0000000b | | | | | | |
| 33 | UNMAP GRANULARITY ALIGNMENT = 0x00 0000 | | | | | | | |
| ... | | | | | | | | |
| 35 | Reserved = all 0x00 | | | | | | | |
| 36 | | | | | | | | |
| ... | | | | | | | | |
| 63 | | | | | | | | |

Note:

- 1) Individual value of each logical unit.

3.12.6. Block Device Characteristics

Table 51 Block Device Characteristics

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------------------------|---|---|--|-----------------------------|---|---|---|
| Byte | | | | | | | | |
| 0 | PERIPHERAL QUALIFIER = 000b | | | PERIPHERAL DEVICE TYPE 00000b ^(Note 1) 11110b ^(Note 2) | | | | |
| 1 | PAGE CODE = 0xB1 | | | | | | | |
| 2 | PAGE LENGTH = 0x003C | | | | | | | |
| 3 | | | | | | | | |
| 4 | MEDIUM ROTATION RATE = 0x0001 | | | | | | | |
| 5 | | | | | | | | |
| 6 | Reserved = 0x00 | | | | | | | |
| 7 | Reserved = 0000b | | | | NOMINAL FORM FACTOR = 0000b | | | |
| 8 | Reserved = all 0x00 | | | | | | | |
| ... | | | | | | | | |
| 63 | | | | | | | | |

Note:

- 2) Direct Access Device for logical unit (non well known)
- 3) Well known logical unit

3.12.7. Thin Provisioning

Table 52 Thin Provisioning

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--|-----------|----------------|---------------------------------|----------------|---|--------|---|
| Byte | | | | | | | | |
| 0 | PERIPHERAL QUALIFIER = 000b | | | PERIPHERAL DEVICE TYPE = 00000b | | | | |
| 1 | PAGE CODE = 0xB2 | | | | | | | |
| 2 | PAGE LENGTH = 0x0004 | | | | | | | |
| 3 | | | | | | | | |
| 4 | THRESHOLD EXPONENT ^(Note 2) | | | | | | | |
| 5 | TPU ^(Note 1) | TPWS = 0b | Reserved = 00b | | ANC_SUP = 000b | | DP = 0 | |
| 6 | Reserved = 0x0000 | | | | | | | |
| 7 | | | | | | | | |

Note:

- 1) The value of TPU is dependent on the configuration of logical units. If the logical unit is configured as thin provisioning, the value is 1. If the logical unit is configured as full provisioning, the value is 0.
- 2) The value of THRESHOLD EXPONENT is dependent on the configuration of logical units.

4. ELECTRICAL CHARACTERISTICS

4.1. Absolute Maximum Ratings

The absolute maximum ratings of a semiconductor device are a set of specified parameter values, which must not be exceeded during operation, even for an instant. If any of these rating would be exceeded during operation, the electrical characteristics of the device may be irreparably altered and the reliability and lifetime of the device can no longer be guaranteed. Moreover, these operations with exceeded ratings may cause break down, damage, and/or degradation to any other equipment. Applications using the device should be designed such that each maximum rating will never be exceeded in any operating conditions. Before using, creating, and/or producing designs, refer to and comply with the precautions and conditions set forth in this document.

Table 53 Absolute Maximum Ratings

| Parameter | Symbol | Min | Max | Unit |
|---|--------|------|-----|------|
| Supply voltage 1 | VCC | -0.3 | 3.9 | V |
| Supply voltage 3 | VCCQ2 | -0.3 | 2.4 | V |
| Input Voltage (M-PHY Signals, REF_CLK, RESET_N) | VIO | -0.3 | 1.6 | V |

4.2. H/W Reset Operation

Table 54 RESET_N Characteristics

| Parameter | Symbol | Min | Max | Unit |
|--|------------------|-----------|-----------|------|
| Input High voltage ^(Note 1) | V _{IH} | 0.65*VCCQ | VCCQ+0.3 | V |
| Input Low voltage ^(Note 1) | V _{IL} | VSS-0.3 | 0.35*VCCQ | V |
| Input Capacitance | C _{in} | - | 10 | pF |
| Input leakage Current | I _{Ikg} | - | 10 | μA |
| Pulse Width | tRSTW | 1 | - | μs |
| High Period (Interval) | tRSTH | 1 | - | μs |
| Filtering Period | tRSTF | 100 | - | ns |

Note:

- 1) Users need to input VCCQ (1.1 to 1.3V) based signals to RESET_N to meet the electrical characteristics defined by UFS specification.

4.3. Reference Clock

Table 55 REF_CLK Characteristics

| Parameter | Symbol | Min | Max | Unit |
|--|---------------|----------------------|--------------------------|------------|
| Frequency | f_{ref} | | 19.2 26 38.4 52 | MHz |
| Frequency Error | f_{ERROR} | -150 | +150 | ppm |
| Input High Voltage ^(Note 1) | V_{IH} | $0.65 \cdot V_{CCQ}$ | - | V |
| Input Low Voltage ^(Note 1) | V_{IL} | - | $0.35 \cdot V_{CCQ}$ | V |
| Clock Rise Time ^(Note 2) | t_{RISE} | - | 2 | ns |
| Clock Fall Time ^(Note 2) | t_{FALL} | - | 2 | ns |
| Duty Cycle | t_{DC} | 45 | 55 | % |
| Phase Noise | N | - | -66 | dBc |
| Noise Floor Density | $N_{density}$ | - | -140 | dBc/Hz |
| Input impedance | RLRX | 100 | - | k Ω |
| | CLRX | - | 5 | pF |

Note:

- 1) Users need to input VCCQ (1.1 to 1.3V) based signals to REF_CLK to meet the electrical characteristics defined by UFS specification.
- 2) Clock rise time and clock fall time shall be measured from 20% to 80% of the window defined by V_{IL} MAX to V_{IH} MIN.

4.4. Power Supply

4.4.1. Power Supply Voltage and Power up Sequence

Users should follow power up/down sequence defined in JEDEC UFS specification Ver.2.1 and this document. Toshiba UFS device requires the following sequence during power-up in addition to JEDEC UFS specification.

- Timing definition of tPRUH and tPRUL.

tPRUH and tPRUL are defined as the time from when VCC and VCCQ2 exceed 0.3V till when VCC and VCCQ2 reach minimum operation voltage, VCC_{MIN} and VCCQ2_{MIN}. tPRUH and tPRUL need to satisfy the values shown at the table below. Maximum values are defined by JEDEC UFS specification, but minimum values are not defined and are characteristic to TOSHIBA UFS devices.

- Timing definition after supply voltages exceed a specified values

VCC and VCCQ2 should reach valid voltage range within 1ms after exceeding 80% of VCC_{MIN} and VCCQ2_{MIN}.

- Voltage definition in case 2 step ramp-up is applied

If power-up sequence takes 2 step ramp-up approach, the voltage of 1st step should be less than 0.80 V for all supply voltages.

Table 56 Supply Voltage

| Parameter | Symbol | Min | Max | Unit |
|---|--------|------|------|------|
| Supply voltage 1 | VCC | 2.7 | 3.6 | V |
| Supply voltage 3 | VCCQ2 | 1.70 | 1.95 | V |
| Supply voltage power-up timing for 3.3V | tPRUH | 0.01 | 35 | ms |
| Supply voltage power-up timing for 1.8V | tPRUL | 0.01 | 25 | ms |

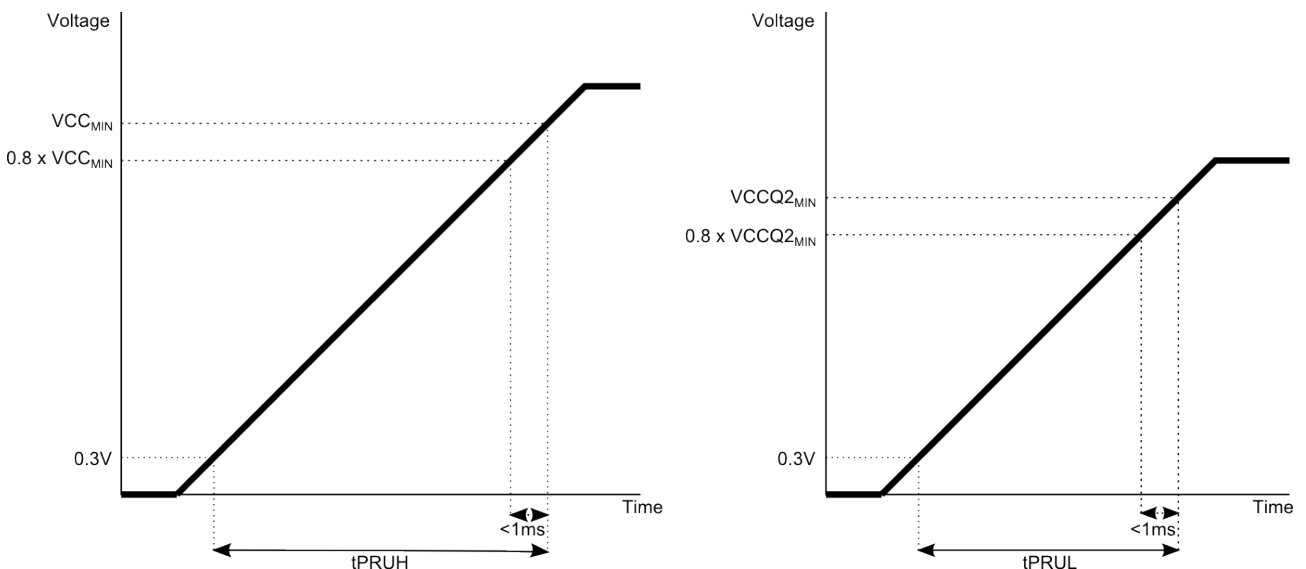


Figure 6 Power up sequence

4.4.2. Operating Current (RMS)

Table 57 Maximum Supply Current

| TOSHIBA Part Number | Density | NAND Flash Type | HS-Gear | No. of Lane | Symbol | Max. Operating Current [mA] |
|---------------------|---------|------------------------------|---------|-------------|--------|-----------------------------|
| THGAF8T1T83BAIR | 256GB | 8 x 256Gbit BiCS FLASH Gen.3 | HS-G3 | 1 | Icc | 195 |
| | | | | | Iccq2 | 345 |
| | | | | 2 | Icc | 200 |
| | | | | | Iccq2 | 475 |

Note:

- 1) The measurement for max RMS current is done as average RMS current consumption over a period of 100ms
- 2) The conditions of maximum values are 85°C, VCC = 3.6V, VCCQ2 = 1.95V.

4.4.3. Sleep Mode Current and Timing Definition

The device can transit to UFS Sleep/M-PHY Hibern8 by issuing Start Stop Unit command and Hibern8 Enter command.

Table 58 shows the current consumption during UFS Sleep/M-PHY Hibern8 and Table 59 shows the timing definition that the device transit to the status after Hibern8 Enter command is accepted in the device.

Table 58 Sleep Mode Current

| TOSHIBA Part Number | Density | NAND Flash Type | Symbol | Current [μA] | |
|---------------------|---------|------------------------------|-------------|---------------|---------------|
| | | | | Typ. (Note 1) | Max. (Note 2) |
| THGAF8T1T83BAIR | 256GB | 8 x 256Gbit BiCS FLASH Gen.3 | Iccqs2 | 270 | 2305 |
| | | | Iccs+Iccqs2 | 350 | 3505 |

Note:

- 1) The conditions of typical values are 25°C, VCC = 3.3V, VCCQ2 = 1.8V, UFS Sleep/M-PHY Hibern8.
- 2) The conditions of maximum values are 85°C, VCC = 3.6V, VCCQ2 = 1.95V, UFS Sleep/M-PHY Hibern8.

Table 59 Sleep Mode Transition Timing

| Parameter | Symbol | Min | Max | Unit |
|--|--------|-----|------|------|
| Transition timing to UFS Sleep/M-PHY Hibern8 | tSLEEP | - | 1000 | us |

Note:

- 1) The starting point of transition timing is when a host recognizes HIBERNATE_ENTER.ind. Thus, a host needs to wait for more than tSLEEP time after receiving HIBERNATE_ENTER.ind.

4.5. M-PHY Characteristics

4.5.1. Termination

Toshiba UFS modules support both terminated and unterminated states. The M-TX (D_{OUT_t}/ D_{OUT_c}) is always terminated and the M-RX (D_{IN_t}/ D_{IN_c}) includes switchable differential termination as UFS specification defines.

4.5.2. Functions

The functions of M-TX and M-RX are listed with their abbreviations as follows.

Table 60 Functions and Abbreviations

| Abbreviation | Functions |
|--------------|------------------|
| HS-TX | M-TX in HS-MODE |
| PWM-TX | M-TX in PWM-MODE |
| HS-RX | M-RX in HS-MODE |
| PWM-RX | M-RX in PWM-MODE |
| SQ-RX | M-RX in squelch |

4.5.3. M-TX Characteristics

Toshiba UFS M-TX module supports the voltage and the timing parameters, which are defined on M-PHY^R specification.

4.5.3.1. Common Characteristics

Toshiba UFS modules support two drive amplitudes, the large amplitude (LA) and the small amplitude (SA). Every M-TX in every LINK will start communication with LA after power up or reset. Option to switch to SA mode is supported via a Configuration Attribute defined on M-PHY^R specification. D_{OUT_t}/ D_{OUT_c} pair should satisfy V_{CM_TX};

$$V_{CM_TX}(t) = \frac{V_{TXDP}(t) + V_{TXDN}(t)}{2}$$

* V_{TXDP}/V_{TXDN}: Positive/Negative signal voltage

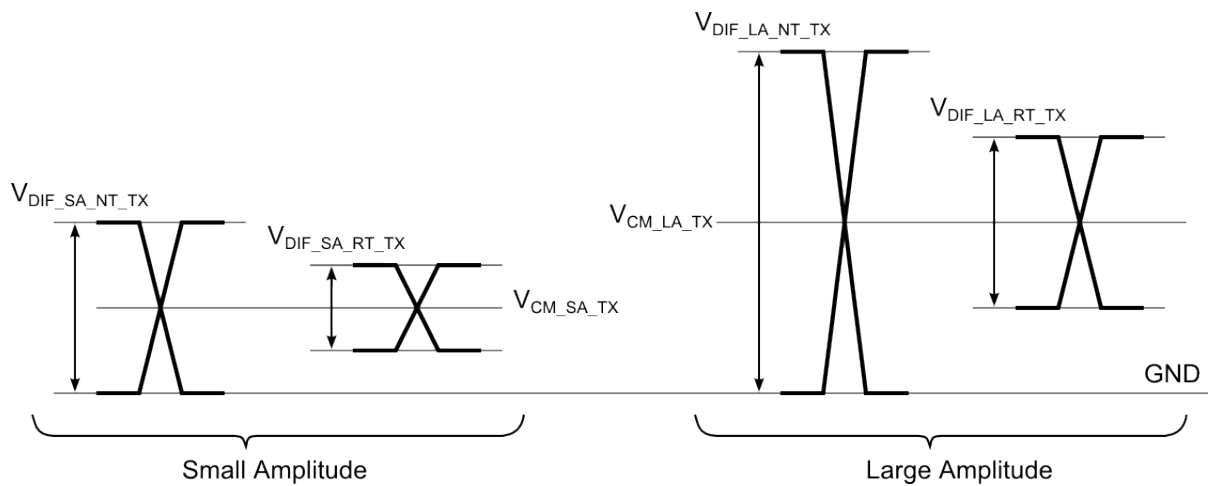


Figure 7 M-TX Signal Levels

Table 61 M-TX Parameters defined by M-PHY standard

| Parameter | Symbol | Min | Max | Unit |
|---|---------------------------|-----|-----|----------|
| Large Amplitude differential TX DC voltage in a terminated state | $V_{DIF_DC_LA_RT_TX}$ | 160 | 240 | mV |
| Large Amplitude differential TX AC voltage in a terminated state | $V_{DIF_AC_LA_RT_TX}$ | 140 | 250 | mV |
| Large Amplitude differential TX DC voltage in an unterminated state | $V_{DIF_DC_LA_NT_TX}$ | 320 | 480 | mV |
| Large Amplitude differential TX AC voltage in an unterminated state | $V_{DIF_AC_LA_NT_TX}$ | 280 | 500 | mV |
| Small Amplitude differential TX DC voltage in a terminated state | $V_{DIF_DC_SA_RT_TX}$ | 100 | 130 | mV |
| Small Amplitude differential TX AC voltage in a terminated state | $V_{DIF_AC_SA_RT_TX}$ | 80 | 140 | mV |
| Small Amplitude differential TX DC voltage in an unterminated state | $V_{DIF_DC_SA_NT_TX}$ | 200 | 260 | mV |
| Small Amplitude differential TX AC voltage in an unterminated state | $V_{DIF_AC_SA_NT_TX}$ | 160 | 280 | mV |
| Large Amplitude common-mode TX voltage | $V_{CM_LA_TX}$ | 160 | 260 | mV |
| Small Amplitude common-mode TX voltage | $V_{CM_SA_TX}$ | 80 | 190 | mV |
| Single-ended output resistance | R_{SE_TX} | 40 | 60 | Ω |

4.5.3.2. HS-TX Characteristics

Table 62 HS-TX voltage and timing parameters defined by M-PHY standard

| Parameter | Symbol | Min | Max | Unit |
|-------------------------------------|---------------------------|-----|-----|-----------|
| Differential TX AC voltage in HS-G3 | $V_{DIF_AC_HS_G3_TX}$ | 40 | - | mV |
| Fall time. | $T_{F_HS_TX}$ | 0.1 | - | U_{IHS} |
| Rise time. | $T_{R_HS_TX}$ | 0.1 | - | U_{IHS} |
| Transmitter pulse width. | T_{PULSE_TX} | 0.9 | - | U_{IHS} |

4.5.3.3. PWM-TX Characteristics

- PWM Bit Duration

A PWM bit consists out of a DIF-N LINE state followed by a DIF-P LINE state, which are either signaled for the minor duration $T_{PWM_MINOR_TX}$ or for the major duration $T_{PWM_MAJOR_TX}$. The durations $T_{PWM_MINOR_TX}$ and $T_{PWM_MAJOR_TX}$ are defined as the time between the zero crossings of the differential output signal.

The PWM transmit bit duration T_{PWM_TX} is defined as the duration between zero crossings of two consecutive falling edges of a differential signal at the PWM-TX output.

$$T_{PWM_TX} = T_{PWM_MINOR_TX} + T_{PWM_MAJOR_TX}$$

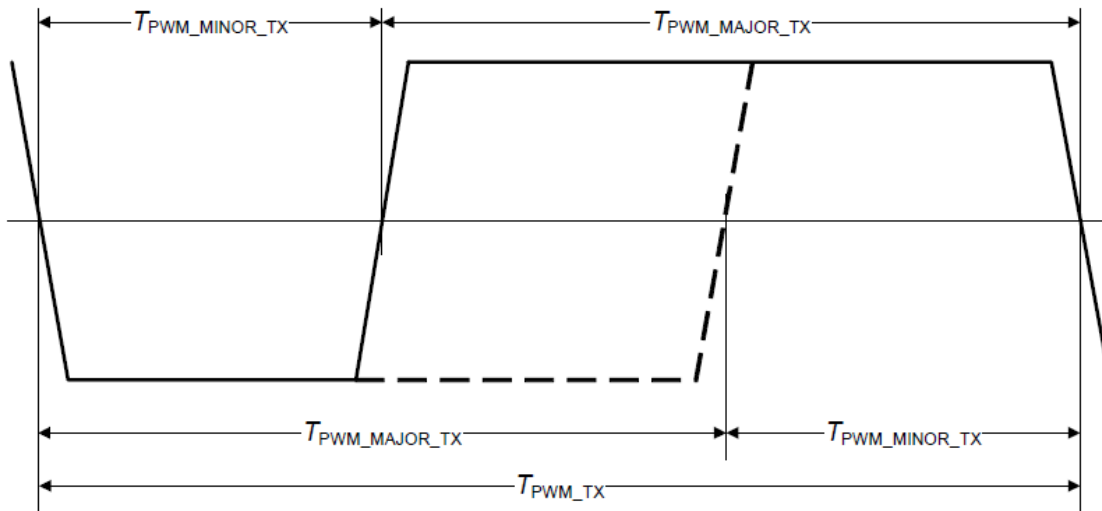


Figure 8 TX Minor and Major Duration in a PWM Signal

Table 63 PWM-TX timing parameters defined by M-PHY standard

| Parameter | Symbol | Min | Max | Unit |
|--------------------------------------|-------------------|------|-------|---------------|
| PWM transmit bit duration in PWM-G1. | $T_{PWM_G1_TX}$ | 1/9 | 1/3 | μs |
| PWM transmit bit duration in PWM-G2. | $T_{PWM_G2_TX}$ | 1/18 | 1/6 | μs |
| PWM transmit bit duration in PWM-G3. | $T_{PWM_G3_TX}$ | 1/36 | 1/12 | μs |
| PWM transmit bit duration in PWM-G4. | $T_{PWM_G4_TX}$ | 1/72 | 1/24 | μs |
| Rise time. | $T_{R_PWM_TX}$ | - | 0.070 | T_{PWM_TX} |
| Fall time. | $T_{F_PWM_TX}$ | - | 0.070 | T_{PWM_TX} |

4.5.4. M-RX Characteristics

Toshiba UFS M-RX module supports the voltage and the timing parameters, which are defined on M-PHY^R specification.

4.5.4.1. Common Characteristics

D_{IN_t}/D_{IN_c} pins are a differential input signal pair and should satisfy V_{CM_RX}, which is defined on M-PHY^R specification as follows;

$$V_{CM_RX}(t) = \frac{V_{RXDP}(t) + V_{RXDN}(t)}{2}$$

* V_{RXDP}/V_{RXDN}: Positive/Negative signal voltage

Table 64 M-RX parameters defined by M-PHY standard

| Parameter | Symbol | Min | Max | Unit |
|---|------------------------|-----|-----|------|
| Differential RX voltage amplitude in terminated state | V _{DIF_RT_RX} | 60 | 245 | mV |
| Differential RX voltage amplitude in unterminated | V _{DIF_NT_RX} | 120 | 490 | mV |
| RX common-mode voltage ^(Note 1) | V _{CM_RX} | 25 | 330 | mV |
| Differential input resistance | R _{DIFF_RX} | 80 | 110 | Ω |

Note:

1. The values include a ground shift of ±50 mV between the M-TX and M-RX

4.5.4.2. HS-RX Characteristics

- Receiver Pulse Width

The receiver pulse width, T_{PULSE_RX} , is defined as the minimum time between the zero crossings of the differential input signal $V_{DIF_RX}(t)$ when a test pattern is applied at the RXDP and RXDN PINs of an HS-RX.

An HS-RX shall detect an input signal with a receiver pulse width that conforms with the limit of T_{PULSE_RX} .

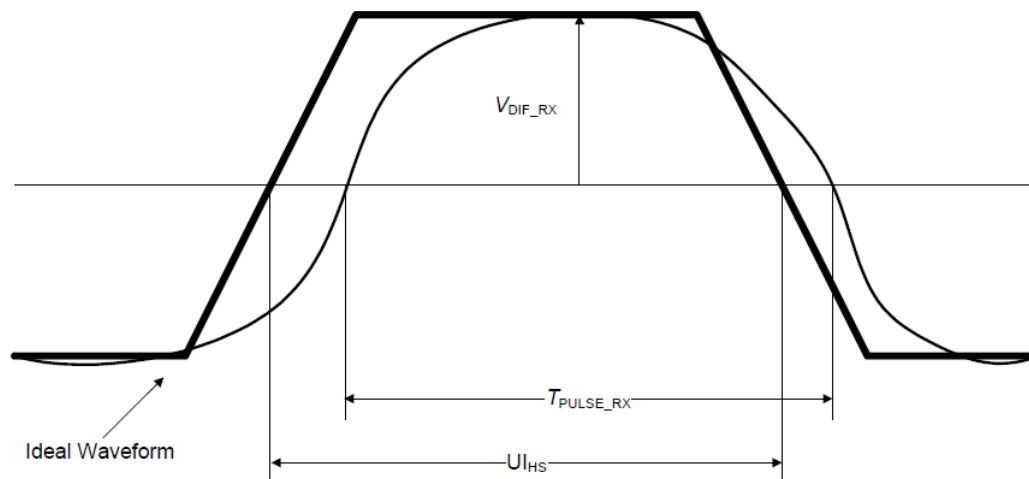


Figure 9 Receiver Pulse Width

Table 65 HS-RX voltage and timing parameters defined by M-PHY standard

| Parameter | Symbol | Min | Max | Unit |
|--|----------------------------|----------------|-----|----------|
| Accumulated differential receiver input voltage for HS-G1. | $V_{DIF_ACC_RX}$ | 40 | - | mV |
| Accumulated differential receiver input voltage for HS-G2. | $V_{DIF_ACC_HS_G2_RX}$ | 40 | - | mV |
| Accumulated differential receiver input voltage for HS-G3. | $V_{DIF_ACC_HS_G3_RX}$ | 40 | - | mV |
| Receiver eye opening. | T_{EYE_RX} | 0.20 | - | U_{HS} |
| Receiver eye opening in HS-G3. | $T_{EYE_HS_G3_RX}$ | $1-T_{J_{RX}}$ | - | U_{HS} |
| Receiver pulse width. | T_{PULSE_RX} | 0.80 | - | U_{HS} |

4.5.4.3. PWM-RX Characteristics

- PWM Bit Duration

The PWM receive bit duration is defined as the duration between zero crossings of two consecutive falling edges of a differential signal at the PWM-RX input. $T_{PWM_MINOR_RX}$, $T_{PWM_MAJOR_RX}$, and T_{PWM_RX} are shown as follows.

$$T_{PWM_RX} = T_{PWM_MINOR_RX} + T_{PWM_MAJOR_RX}$$

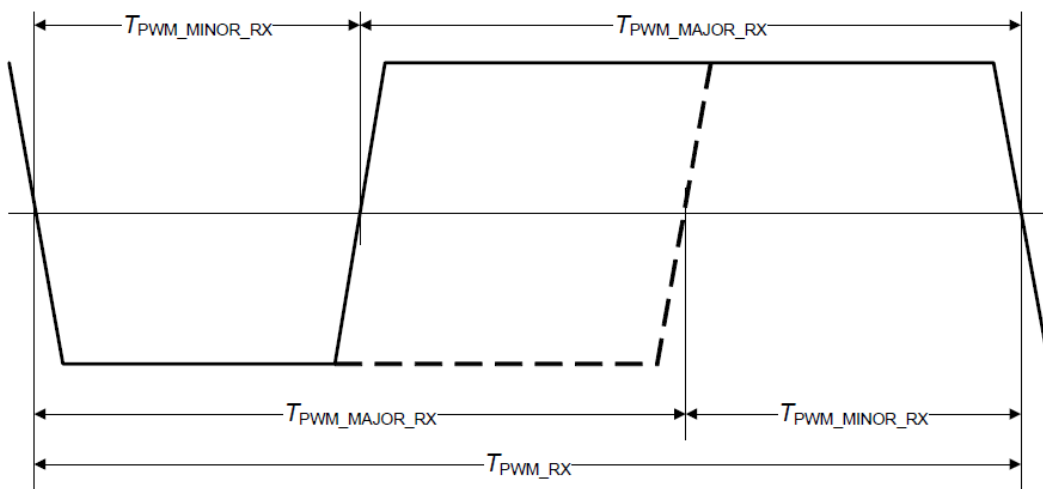


Figure 10 RX Minor and Major Duration in a PWM Signal

Table 66 PWM-RX voltage and timing parameters defined by M-PHY standard

| Parameter | Symbol | Min | Max | Unit |
|---|--------------------|------|------|---------------|
| Accumulated differential RX voltage amplitude Defined for Compliant Jitter Tolerance Pattern in SYS-MODE, PWM-G0, PWM-G1, PWM-G2, PWM-G3, and PWM-G4. | $V_{DIF_ACC_RX}$ | 40 | - | mV |
| PWM receive bit duration in PWM-G1. | $T_{PWM_G1_RX}$ | 1/9 | 1/3 | μs |
| PWM receive bit duration in PWM-G2. | $T_{PWM_G2_RX}$ | 1/18 | 1/6 | μs |
| PWM receive bit duration in PWM-G3. | $T_{PWM_G3_RX}$ | 1/36 | 1/12 | μs |
| PWM receive bit duration in PWM-G4. | $T_{PWM_G4_RX}$ | 1/72 | 1/24 | μs |
| Rise time defined for Compliant Jitter Tolerance Pattern. | $T_{R_PWM_RX}$ | - | 0.14 | T_{PWM_RX} |
| Fall time defined for Compliant Jitter Tolerance Pattern. | $T_{F_PWM_RX}$ | - | 0.14 | T_{PWM_RX} |

4.5.4.4. SQ-RX Characteristics

- Squelch Pulse and RF Rejection

The squelch noise pulse width T_{PULSE_SQ} is defined as the time the M-RX input signal $V_{RXDN}(t) - V_{RXDP}(t)$ is larger than $V_{SQ,MAX}$. The SQ-RX shall reject single input noise pulses with an amplitude beyond $V_{SQ,MAX}$ and shorter than the squelch noise pulse width T_{PULSE_SQ} . The noise pulse spacing T_{SPACE_SQ} is defined as the time between the crossings of two adjacent pulse edges of two different, but adjacent, noise pulses with $V_{SQ,MAX}$. Multiple pulses shall be rejected by the SQ-RX when the duration between adjacent pulses is larger than T_{SPACE_SQ} .

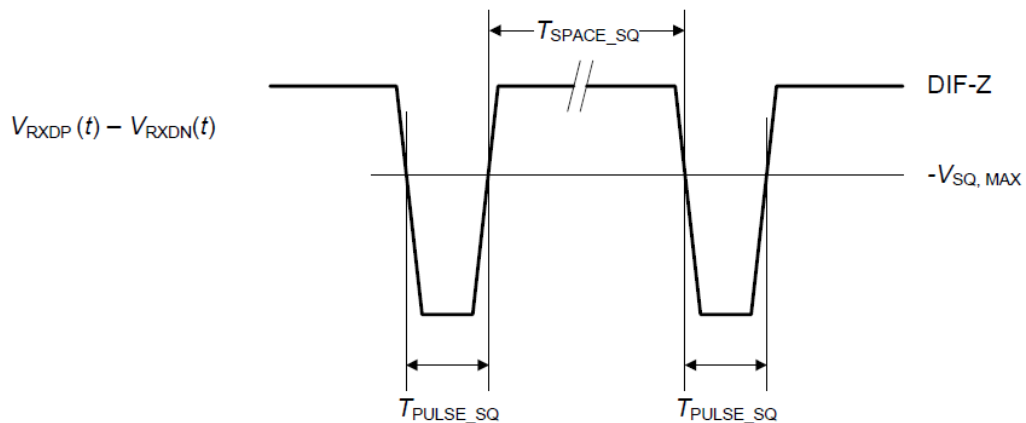


Figure 11 Pulse Rejection and Non-squelch State Detection

Table 67 SQ-RX voltage and timing parameters defined by M-PHY standard

| Parameter | Symbol | Min | Max | Unit |
|---|-----------------|-----|-----|------|
| Squelch exit voltage. | V_{SQ} | 50 | 140 | mV |
| Squelch differential voltage amplitude. | V_{DIF_SQ} | - | 20 | mV |
| Squelch common-mode voltage. | V_{CM_SQ} | 0 | 330 | mV |
| Peak interference amplitude. | V_{INT_SQ} | - | 200 | mV |
| Interference frequency. | f_{INT_SQ} | 500 | - | MHz |
| Noise pulse width. | T_{PULSE_SQ} | - | 20 | ns |
| Noise pulse spacing. | T_{SPACE_SQ} | 500 | - | ns |

5. Reliability Guidance

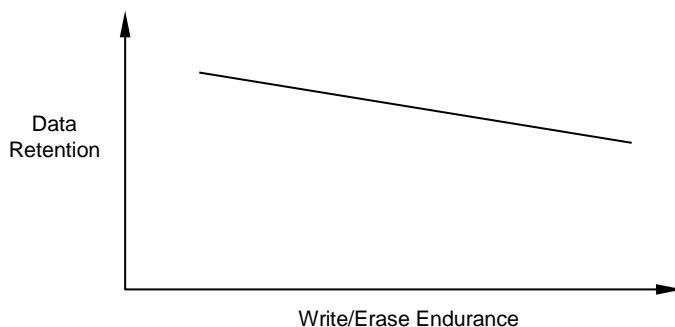
This reliability guidance is intended to notify some guidance related to using raw NAND flash. Although random bit errors may occur during use, it does not necessarily mean that a block is bad. Generally, a block should be marked as bad when a program status failure or erase status failure is detected. The other failure modes may be recovered by a block erase. ECC treatment for read data is mandatory due to the following Data Retention and Read Disturb failures.

- Write/Erase Endurance

Write/Erase endurance failures may occur in a cell, page, or block, and are detected by doing a status read after either an auto program or auto block erase operation. The cumulative bad block count will increase along with the number of write/erase cycles.

- Data Retention

The data in memory may change after a certain amount of storage time. This is due to charge loss or charge gain. After block erasure and reprogramming, the block may become usable again. Also write/erase endurance deteriorates data retention capability. The figure below shows a generic trend of relationship between write/erase endurance and data retention.



- Read Disturb

A read operation may disturb the data in memory. The data may change due to charge gain. Usually, bit errors occur on other pages in the block, not the page being read. After a large number of read cycles (between block erases), a tiny charge may build up and can cause a cell to be soft programmed to another state. After block erasure and reprogramming, the block may become usable again.

Considering the above failure modes, TOSHIBA recommends following usages:

- Please avoid any excessive iteration of resets and initialization sequences (Device identification mode) as far as possible after power-on, which may result in read disturb failure. The resets include hardware resets and software resets including Endpoint Reset and Link lost.
- Please avoid any excessive iteration of power mode change from Active or Idle power mode to UFS-Sleep or UFS-PowerDown power mode by START_STOP_UNIT. This condition could be preventable by inserting a write operation.

6. Reference

- JEDEC UFS specification Ver. 2.1
- MIPI UniProSM specification Ver. 1.6
- MIPI M-PHY^R specification Ver. 3.0

7. Document Revision History

| | | |
|---------|------------------|--|
| Rev0.00 | Aug., 25th, 2017 | Released preliminary version |
| Rev1.00 | Nov., 28th, 2017 | Released first version |
| Rev1.10 | Dec., 4th, 2017 | Clarified Serial Number String Descriptor and fixed some typos |

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