

■ Key Features

- 100 μ V Resolution
- High Impedance Differential Inputs
- Differential Reference
- Drive LCD (ICL7106) or LED (ICL7107) Directly
- Four New Convenient Features (ICL7106/ICL7107)
 - Display-Hold
 - Low-Battery Indication
 - Integration Status Indication
 - De-Integration Status Indication

■ Applications

- Digital multimeter
- pH meter
- Capacitance meter
- Thermometer
- Digital Panel meter
- Photometer

■ General Description

The ICL7106 and ICL7107 family are high performance, low power, 3-1/2 digit, dual-slope integrating A/D converters, with on-chip display drivers. The ICL7106 is designed for a single battery operated system, will drive non-multiplexed LCD display directly. The ICL7107 is designed for a dual power supply system, will directly drive common anode LED display.

These A/D converters are inherently versatile and accurate. They are immune to the high noise environments. The true differential high impedance inputs and differential reference are very useful for making ratiometric measurement, such as resistance, strain gauge and bridge transducers. The built-in auto-zero feature automatically corrects the system offset without any external adjustments.

Display-hold, low-battery flag, integration and de-integration status flags are four additional features which are available in the 44-pin package, ICL7106CM and ICL7107CM.

■ Typical Operating Circuit * For the operating circuit of the reverse-pins version, please refer to pin configuration on page 4 and pin description on page 5 & 6

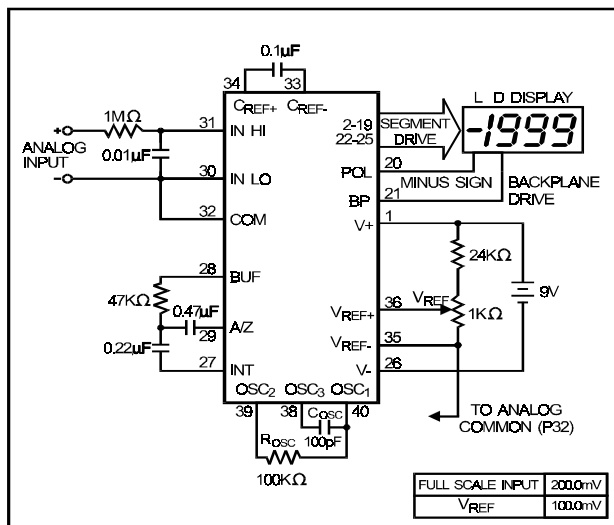


Figure 1. ICL7106 Typical Operating Circuit

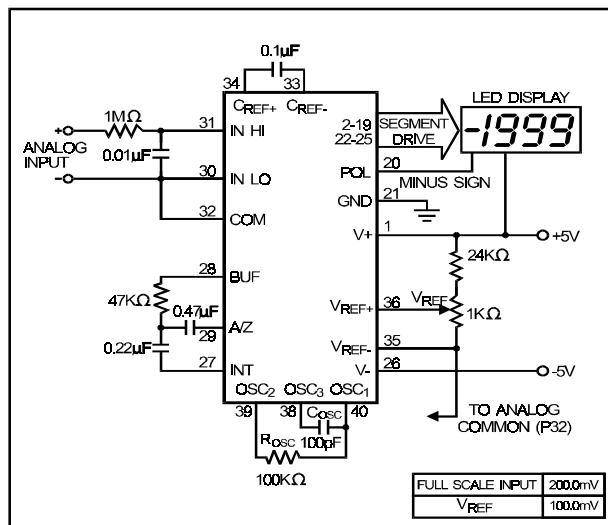


Figure 2. ICL7107 Typical Operating Circuit



■ Absolute Maximum Ratings

ICL7106

Supply Voltage (V+ to V-)	12V
Analog Input Voltage (Either inputs)	V+ TO V-
Reference Input Voltage (Either inputs)	V+ TO V-
Clock Input	Test to V+
Power Dissipation	800mW
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to 150°C
Lead Temperature (Soldering 60 seconds)	300°C

ICL7107

Supply Voltage	
V+	6V
V-	-6V
Analog Input Voltage (Either inputs)	V+ to V-
Reference Input Voltage (Either inputs)	V+ to V-
Clock Input	Gnd to V+
Power Dissipation	800mW
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to 150°C
Lead Temperature (Soldering 60 seconds)	300°C

Static sensitive device. Unused devices must be stored in the conductive material.

Protect device from static discharge and static field. Stresses exceed the above Absolute Maximum Ratings may cause permanent damage to the device. Exposure to Absolute Maximum Rating Conditions for extended periods may affect the reliability of the device.



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ICL7106CPL/ICL7106CM44

ICL7107CPL/ICL7107CM44

3-1/2 Digit A/D Converter
High Accuracy, Low Power

■ Ordering Information

Part Number	Display	Package	Temp. Range (°C)
ICL7106CPL	LCD	DIP40	-25 to 70
ICL7106CM44	LCD	QFP44	-25 to 70
ICL7107CPL	LED	DIP40	-25 to 70
ICL7107CM44	LED	QFP44	-25 to 70



■ Electrical Characteristics

Unless otherwise noted, ICL7106 & ICL7107 are specified at $T_A = 25^{\circ}\text{C}$, $f_{\text{clock}} = 48\text{KHz}$. Supply voltage = 9V (V_+ to V_-)

Parameter	Conditions	Min	Typ	Max	Unit
Zero Input Reading	$V_{\text{in}} = 0\text{V}$ Full-Scale = 200.0mV		0		Digital Reading
Ratiometric Reading	$V_{\text{in}} = V_{\text{ref}} = 100.0\text{mV}$	999	999/1000	1000	Digital Reading
Roll-Over Error (Difference in Reading for Equal Positive and Negative Reading Near Full-Scale)	$-V_{\text{in}} = +V_{\text{in}} \approx 200.0\text{mV}$	-1	-0.2	+1	Counts
Linearity (Max. Deviation From Best Straight Line Fit)	Full-Scale = 200.0mV	-1	-0.2	+1	Counts
Common-Mode Rejection Ratio	$V_{\text{cm}} = -1\text{V}$, $V_{\text{in}} = 0\text{V}$ Full-Scale = 200.0mV		50		$\mu\text{V/V}$
Noise (Pk-Pk Value Not Exceeded 95% of Time)	$V_{\text{in}} = 0\text{V}$ Full-Scale = 200.0mV		15		μV
Leakage Current at Input	$V_{\text{in}} = 0\text{V}$		1	10	pA
Zero Reading Drift	$V_{\text{in}} = 0\text{V}$, 0°C to 70°C		0.2	1	$\mu\text{V}/^{\circ}\text{C}$
Supply Current (Excluding LED current for 7107)	$V_{\text{in}} = 0\text{V}$		0.8	1.2	mA
Analog Common Voltage (With respect to V_+)	$25\text{K}\Omega$ Between Common and V_+	2.8	3.0	3.2	V
Temp. Coeff. of Analog Common (With respect to V_+)	$25\text{K}\Omega$ Between Common and V_+ $0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$		50	75	$\text{ppm}/^{\circ}\text{C}$
Low Battery Flag	V_+ to V_-	6.3	7.0	7.7	V
Test Pin Voltage (ICL7106 only)	With respect to V_+	4	5	6	V
LCD Segment Drive Voltage (ICL7106 only)	V_+ to $V_- = 9\text{V}$	4	5	6	V
Backplane Drive Voltage (ICL7106 only)	V_+ to $V_- = 9\text{V}$	4	5	6	V
Segment Sinking Current (Except Segment AB4) (ICL7107 only)	$V_+ = 5.0\text{V}$ Segment Voltage = 3V	5	8.0		mA
Segment Sinking Current (Segment AB4) (ICL7107 only)	$V_+ = 5.0\text{V}$ Segment Voltage = 3V	10	16		mA

Notes: 1. Input voltage may exceed the supply voltages provided the input current is limited to $\pm 100\mu\text{A}$.
2. Dissipation rating assumes a device is mounted with all leads soldered to printed circuit board.

Pin Configurations

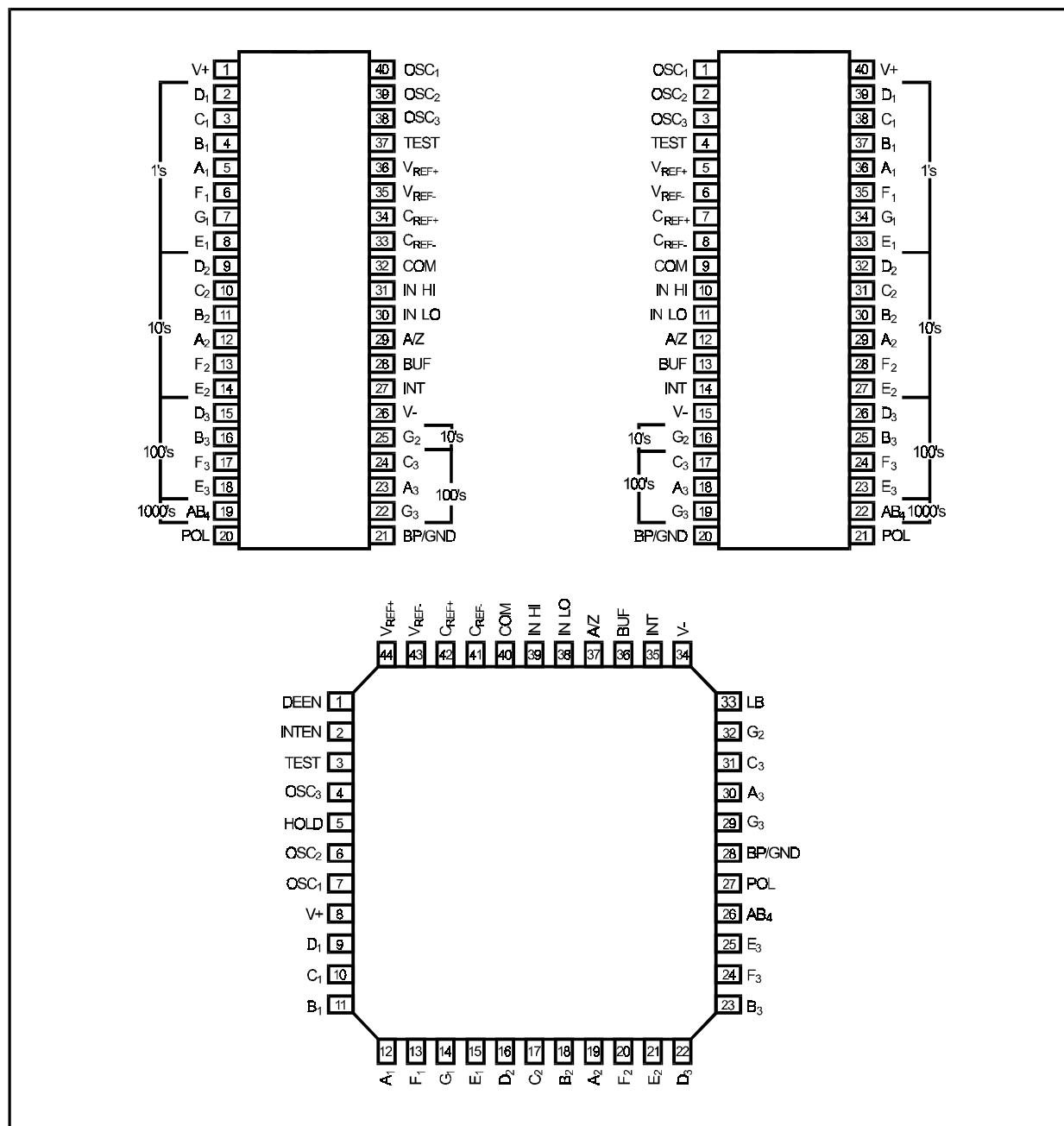
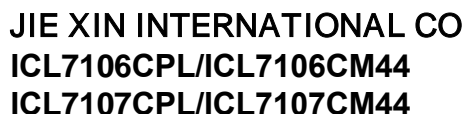


Figure 2. Pin Configurations



■ Pin Description

40-pin DIP Pin Number	40-pin DIP (Reverse)	44-pin PQFP Pin Number	Symbol	Description
1	(40)	8	V+	Positive supply voltage
2	(39)	9	D1	Units-digit D-segment driver
3	(38)	10	C1	Units-digit C-segment driver
4	(37)	11	B1	Units-digit B-segment driver
5	(36)	12	A1	Units-digit A-segment driver
6	(35)	13	F1	Units-digit F-segment driver
7	(34)	14	G1	Units-digit G-segment driver
8	(33)	15	E1	Units-digit E-segment driver
9	(32)	16	D2	Tens-digit D-segment driver
10	(31)	17	C2	Tens-digit C-segment driver
11	(30)	18	B2	Tens-digit B-segment driver
12	(29)	19	A2	Tens-digit A-segment driver
13	(28)	20	F2	Tens-digit F-segment driver
14	(27)	21	E2	Tens-digit E-segment driver
15	(26)	22	D3	Hundreds-digit D-segment driver
16	(25)	23	B3	Hundreds-digit B-segment driver
17	(24)	24	F3	Hundreds-digit F-segment driver
18	(23)	25	E3	Hundreds-digit E-segment driver
19	(22)	26	AB4	Thousands-digit, B&C segments driver
20	(21)	27	POL	Negative-polarity driver
21	(20)	28	BP/ GND	LCD backplane driver (ICL7106) Digital ground (ICL7107)
22	(19)	29	G3	Hundreds-digit G-segment driver
23	(18)	30	A3	Hundreds-digit A-segment driver
24	(17)	31	C3	Hundreds-digit C-segment driver
25	(16)	32	G2	Tens-digit G-segment driver
φw		33	LB	Low-battery flag segment driver
26	(15)	34	V-	Negative power supply voltage
27	(14)	35	INT	Integrator output. Connection point for integration capacitor.
28	(13)	36	BUF	Integrator resistor connection-point.
29	(12)	37	A/Z	Auto-zero capacitor connection-point
30	(11)	38	INLO	Analog-input low
31	(10)	39	INHI	Analog-input high
32	(9)	40	COM	Analog-common



3-1/2 Digit A/D Converter

High Accuracy, Low Power

■ Pin Description (Cont.)

40-pin DIP Pin Number	40-pin DIP (Reverse)	44-pin PQFP Pin Number	Symbol	Description
33	(8)	41	CREF-	Reference capacitor, negative terminal
34	(7)	42	CREF+	Reference capacitor, positive terminal
35	(6)	43	VREF+	Analog-reference input, negative terminal
36	(5)	44	VREF-	Analog-reference input, positive terminal
		1	DEEN	De-integration status flag
37	(4)	2	INTEN	Integration status flag
		3	TEST	Display-test pin, When pulled to V+, display should read -1888.
38	(3)	4	OSC3	See OSC1
		5	HOLD	Hold pin, Logic 1 holds display
39	(2)	6	OCS2	See OSC1
40	(1)	7	OCS1	Pin OSC1, OSC2, OSC3 make up the oscillator. See Clock section for details

■ Function Description

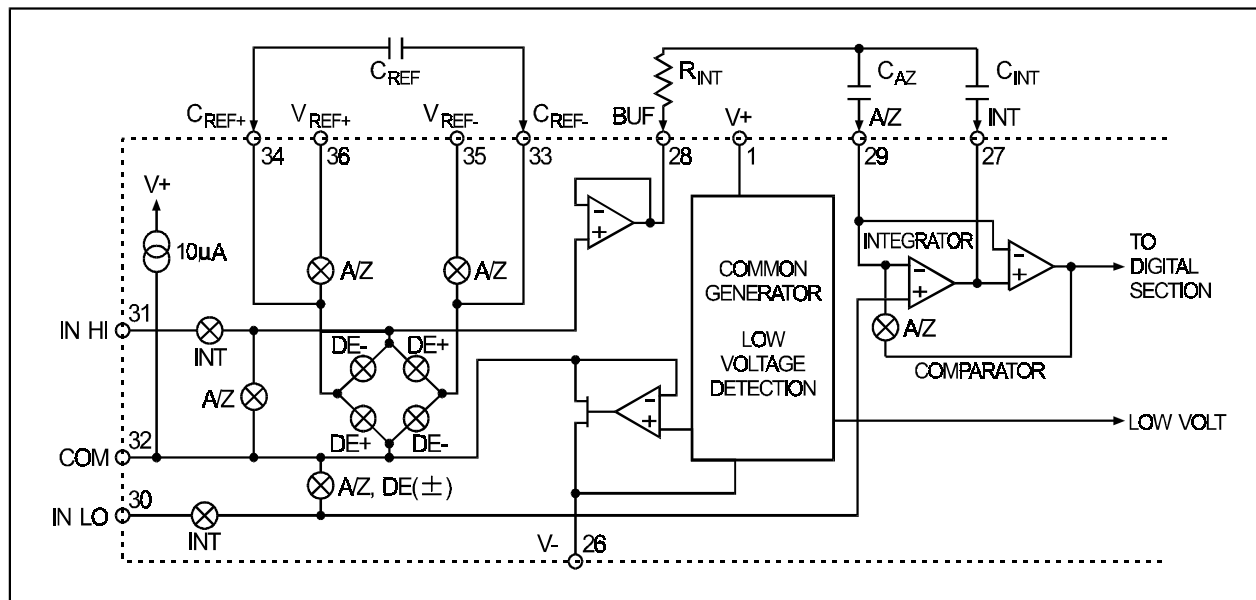


Figure 4. Analog Section



The A/D conversion has the following three phases:

1. Auto-Zero Phase
2. Integration Phase
3. De-integration Phase

Auto-Zero Phase

The INHI and INLO are shorted to analog common internally. The reference capacitor is charged to the reference voltage. A feedback loop is closed around the system to cancel the offset voltage of buffer, integrator and comparator.

Signal Integration phase

The converter integrates the differential voltage across the INHI and INLO for a fixed time, 1000 system clocks. The polarity of the signal is determined at the end of this phase.

Reference Integration Phase

INLO is internally connected to the Analog Common, INHI is connected across the reference capacitor with appropriate polarity determined by the control circuit. The integrator output will then return to zero. The time it takes to return to zero, $1000 \times V_{IN} / V_{REF}$, is the digital representation of the analog signal.

Differential Signal Inputs (INHI & INLO)

The ICL7106/ICL7107 has true differential inputs and accepts input signals within the input common mode voltage range (V_{cm}). Typical range is from 1V above the V_- to 1V below the V_+ . The integrator output can swing within 0.3 V of V_+ or V_- without increasing

linearity errors. Care must be exercised to make sure the integrator output does not saturate. In a typical application, the common mode is eliminated by connecting the INLO to COM, Analog Common.

Differential Reference (V_{REF+} & V_{REF-})

The reference voltage can be generated anywhere within the V_+ to V_- . Under a large common mode voltage, reference capacitor can gain charge during the de-integration of a positive signal. The reference capacitor will lose charge when de-integrating a negative input signal. The difference in reference voltage for positive or negative input voltages can cause the rollover error. To prevent rollover error from being induced by large common-mode voltages, reference capacitor should be large compared to stray node capacitance.

Analog Common (COM)

The Analog Common is to set a common mode voltage for the analog signal. The analog common is typically 3.0V below V_+ , set primary for the battery operated application. Analog common is capable to sink 20 mA. It's source current is limited to 10 μ A. Analog common is therefore easily pulled to a more negative voltage to override the internal reference. When supply voltage is greater than 7V, analog common can be used as reference source with temperature coefficient of typically 50 ppm/ $^{\circ}$ C. The internal heating by the LED display drivers of the ICL7107 may degrade the stability of the Analog Common. An external reference is recommended.

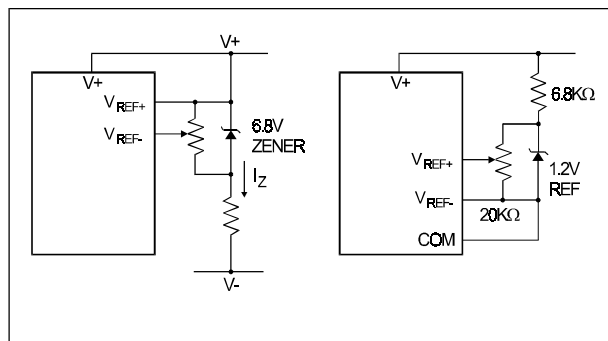


Figure 5. Using an External Reference



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■ Digital Block Diagrams

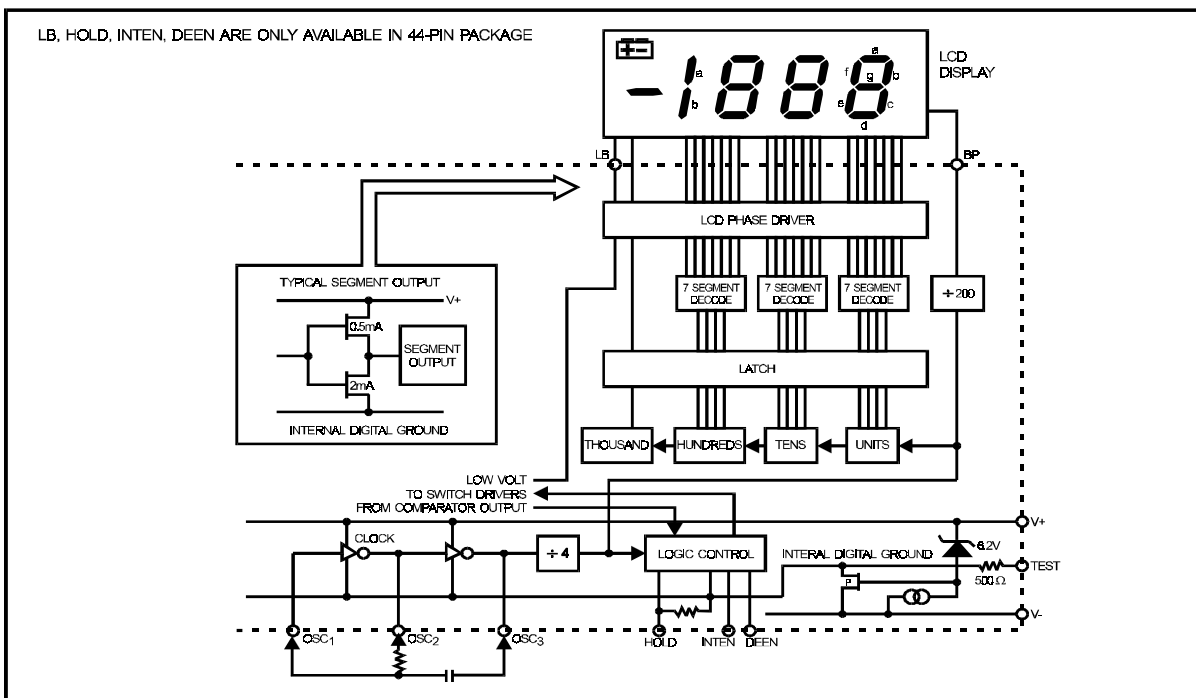


Figure 6. ICL7106 Digital Section

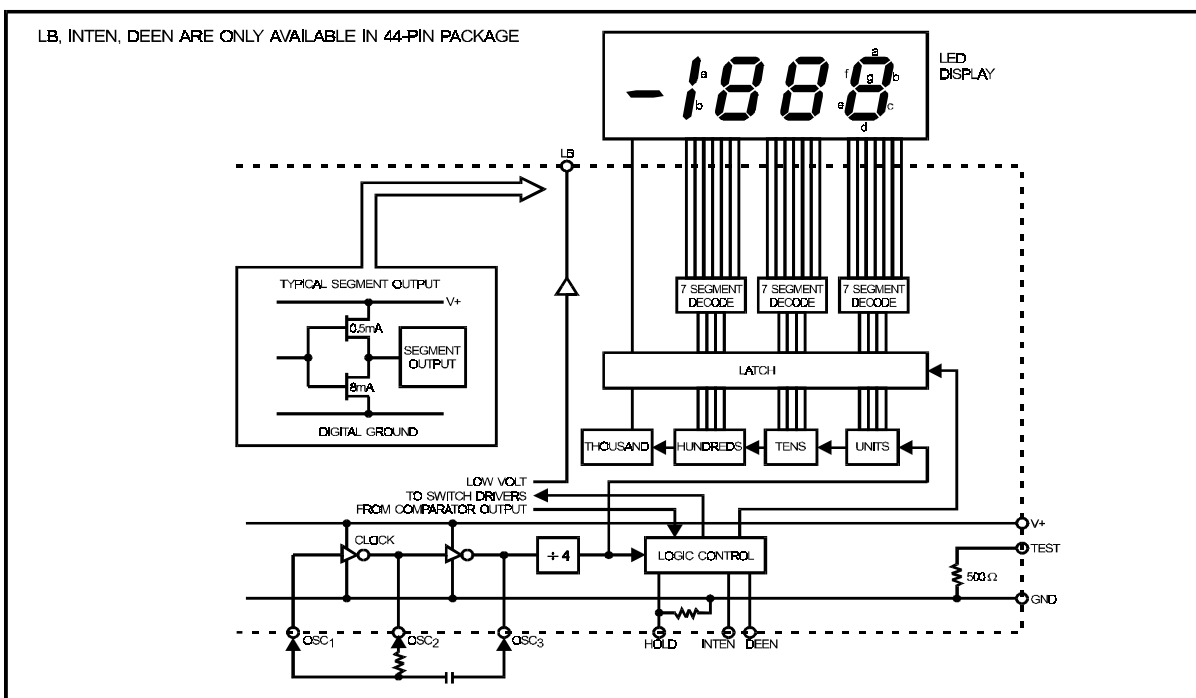


Figure 7. ICL7107 Digital Section

■ Digital Section

Digital Ground

ICL7106 generates an internal digital ground, typically 5V below the V+. The digital ground of ICL7107 is supplied externally.

Clock Circuit

The clock can be generated in either of the following three methods.

1. An external oscillator connected to "OSC1"
2. A crystal between pins "OSC1" and "OOSC2"
3. A R-C oscillator using "OOSC1", "OOSC2" and "OSC3"

Notes: There is no on-chip feedback resistor across osc1 and osc2.

Systems Timing

The oscillator frequency is divided by 4 prior to clocking the internal decade counters. Each conversion takes 4000 counts or 16000 oscillator clock pulses. The timing of each phase are as follows:

Auto-Zero Phase:	1000 to 3000 Counts
Signal Integration Phase:	1000 Counts (Fixed)
Reference Integration Phase :	0 to 2000 Counts

For signals less than full-scale, the unused reference integration time is assigned to the autozero phase.

Segment Drivers (ICL7106)

The backplane frequency is 1/800 of the oscillator clock frequency. For example if the oscillator frequency is 48 KHz (3 conversions per second) the backplane frequency will be 60 Hz. The segment and backplane are at the same frequency with a nominal 5 volt amplitude. The segment is visible (ON) when the segment and the backplane are out of phase, otherwise it is invisible (OFF). The polarity segment is "ON" for negative analog inputs. When the TEST pin on the ICL7106 is pulled to V+, all segments are turned "ON". The display reads -1888. During this mode the LCD segments have a constant DC voltage impressed. DO NOT LEAVE THE DISPLAY IN THIS MODE FOR MORE THAN SEVERAL MINUTES! LCD displays may be destroyed if operated with DC levels for extended periods.

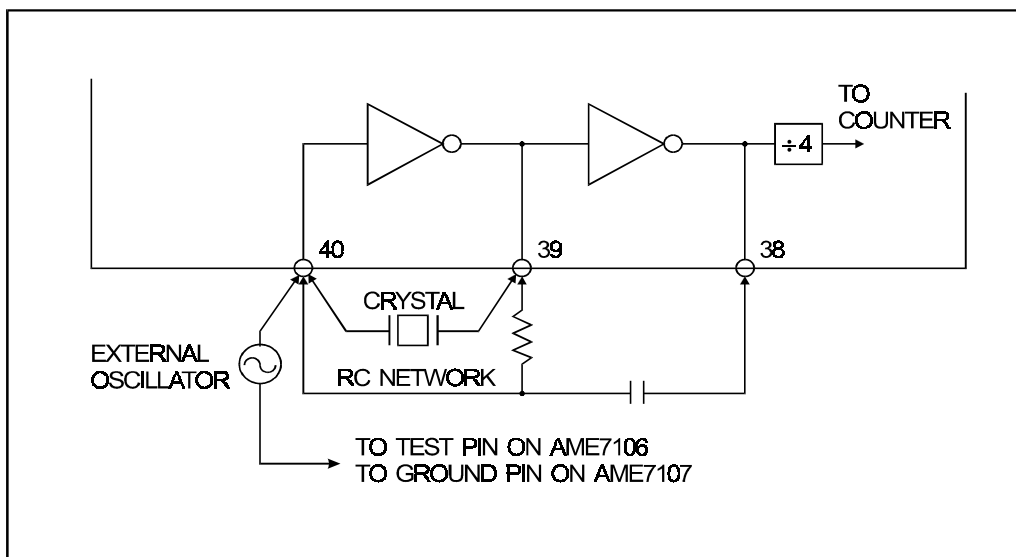


Figure 8. Clock Circuits

Segment Drivers (ICL7107)

The ICL7107 is designed to drive common anode LEDs. All segment drivers are N-channel transistors with a typically 8 mA current driving capability. The 1000's segment AB4 sinks current from two LED segments, and has a 16 mA driving capability. The polarity indication is "on" when the analog input voltage is negative.

Test

When the TEST is pulled to V+ all segments and the minus sign will be activated. The TEST pin is tied to the internally generated digital ground through a 500Ω resistor in the ICL7106. It is typically 5V lower than V+. TEST pin may be used as the negative power supply for external CMOS logic at the maximum current of 1 mA.

Data Hold

When the Hold pin is connected to V+ the conversion result will not be updated. The conversion is still free running during the hold mode. It is available in 44 pin package.

Integration Status (INTEN)

The INTEN is an output signal of the converter, it is "high" during the signal integration phase. This signal can be used as a status indicator or a control to connect the analog signal to the converter for processing. It is available in 44 pin package.

De-integration Status (DEEN)

The DEEN is an output signal of the converter, it is "high" during the reference de-integration phase. The period of the DEEN is proportional to the conversion result. Users may calculate the conversion result by counting the number of clock pulse on the OSC3 pin when DEEN is "high". The conversion result is equal to $(N/4) - 1/2$ where N is the number of the pulse at the OSC3 pin. It is available in 44 pin package.

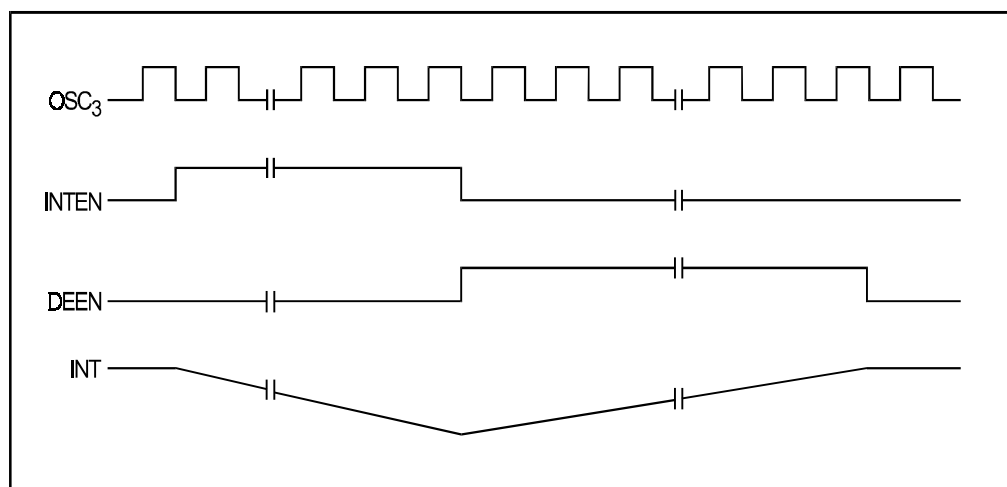


Figure 9. Timing of OSC3, INTEN, DEEN, and INTEGRATOR Output.

■ Component Value Selection

Auto-Zero Capacitor (Caz)

The Caz capacitor size has some influence on system noise. A 0.47μF capacitor is recommended for 200 mV full-scale applications. A 0.047μF capacitor is

recommended for 2.0V full-scale applications. A mylar dielectric capacitor is adequate.

Reference Capacitor (Cref)

A 0.1μF capacitor is acceptable when "INLO" is tied to analog common. If a large common-mode voltage



■ Component Value Selection

Auto-Zero Capacitor (Caz)

The Caz capacitor size has some influence on system noise. A 0.47 μ F capacitor is recommended for 200 mV full-scale applications. A 0.047 μ F capacitor is recommended for 2.0V full-scale applications. A mylar dielectric capacitor is adequate.

Reference Capacitor (Cref)

A 0.1 μ F capacitor is acceptable when "INLO" is tied to analog common. If a large common-mode voltage exists and the application requires 200 mV full-scale, increase Cref to 1.0 μ F. A mylar dielectric capacitor is adequate.

Integrating Capacitor (Cint)

Cint should be selected to maximize the integrator output voltage swing without causing output saturation. A ± 2 V full-scale integrator output swing is recommended if "ANALOG COMMON" is used as signal reference. For 3 readings/second (fosc = 48 KHz) a 0.22 μ F value is suggested. If a different oscillator frequency is used, Cint must be changed in inverse proportion to maintain the nominal 2V integrator swing. An exact expression for Cint is:

$$C_{int} = [(4000)(1/f_{osc})(V_{fs}/R_{int})] / V_{int}$$

where:

fosc = Oscillator clock frequency

Vfs = Full-scale input voltage

Rint = Integrating resistor

Vint = Desired full-scale integrator output swing

Cint must have low dielectric absorption to minimize rollover error. A polypropylene capacitor is recommended.

Integrating Resistor (Rint)

The input buffer amplifier and integrator both have a class A output stage with 100 μ A quiescent current. The integrator and buffer can supply 20 μ A drive currents with negligible linearity errors. Rint is chosen to keep the output stage in the linear region. For a 200mV full-scale, it is 47K Ω ; 2.0V full-scale requires 470K Ω .

Summary of component selection:

Full scale	200.0 m V	2.000 V
C a z	0.47 μ F	0.047 μ F
R i n t	47 K Ω	470 K Ω
C i n t	0.22 μ F	0.22 μ F
V r e f	100.0 m V	1.000 V

Note: fosc = 48 KHz

Oscillator Components

R-C Oscillator

A 100 K Ω Rosc is recommended for all frequencies. Cosc is selected by using the equation:

$$f_{osc} = 0.45/(RC)$$

For fosc of 48KHz, Cosc is 100pF nominally.

To achieve maximum line noise rejection, the signal-integrate period should be a multiple of line period. The optimum oscillator frequencies for 60 Hz and 50 Hz rejection are listed as follows:

For 60 Hz rejection:

40KHz, 48KHz, 60KHz etc.

For 50 Hz rejection:

40KHz, 50KHz, 66-2/3KHz etc.

Reference Voltage Selection

A full-scale reading (2000 counts) requires the input signal be twice the reference voltage.

Full-Scale Voltage	Vref
200.0 m V	100.0 m V
2.000 V	1.000 V

In some applications a scale factor other than unity may exist between a transducer output voltage and the required digital reading. Assume, for example, a pressure transducer output is 600 mV for 2000 lb/in². Rather than dividing the input voltage by three the reference voltage should be set to 300 mV. This permits the transducer input to be used directly. The integrator resistor would be 120K Ω . In some temperature and weighting system with variable tare, the offset reading can be generated by connecting the voltage transducer between INHI and COMMON and the variable offset voltage between COMMON and INLO.

Power Supplies

The ICL7107 is designed to work from $\pm 5V$ supplies. However, if a negative supply is not available, it can be generated from the clock output with two diodes, two capacitors, and an inexpensive IC. The 7660 DC to DC converter may also be used to generate $-5V$ from $+5V$.

Low Battery Flag (LB)

The low battery flag is set when the supply voltage ($V+$ to $V-$) is lower than seven volts, typical. Once the LB is set, the waveform of the LB will be out of phase with the BP (Back Plane) to turn on a low battery annunciator for ICL7106; LB pin will be low (Ground) for ICL7107.

for ICL7107 and is capable to sink 8 mA to turn on a LED indicator.

ICL7107 Power Dissipation Reduction

The ICL7107 sinks the LED display current and this generates heat in the IC package. If the internal voltage reference is used, the fluctuating chip temperature can cause the display to change reading. The ICL7107 package power dissipation can be reduced by reducing the LED common anode voltage.

A typical LED has 1.8 volts across it, at 7mA. When its common anode is connected to $+5V$, the ICL7107

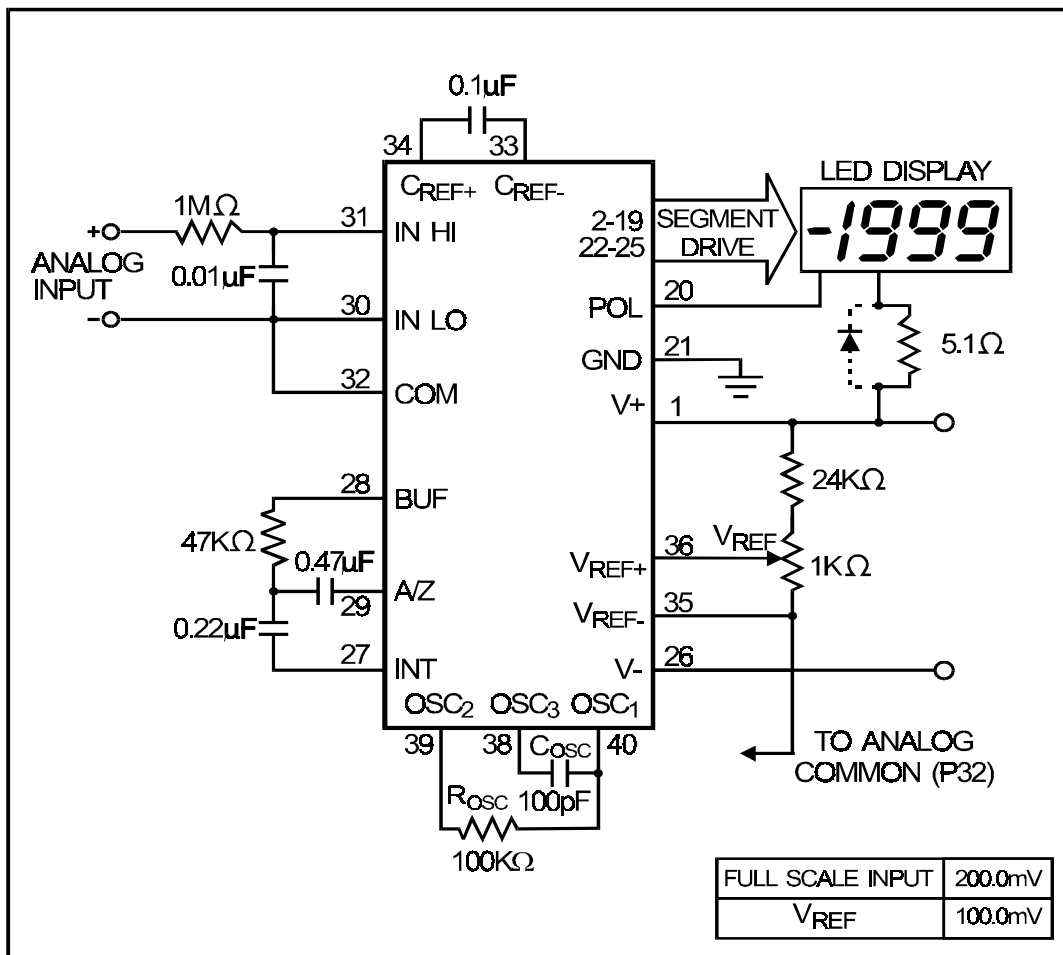


Figure 10. Limiting Power Dissipation by Diode or Resistor for ICL7107

output is at 3.2V. Maximum power dissipation is $8.1 \text{ mA} \times 3.2 \text{ V} \times 24 \text{ segments} = 622 \text{ mW}$. However, once the ICL7107 output voltage is above two volts, the LED current is essentially constant as output voltage increases. Reducing the output voltage by 0.7V, results in 7.7mA of LED current, only a 5 percent reduction. Maximum power dissipation is only $7.7 \text{ mA} \times 2.5 \text{ V} \times 24 = 462 \text{ mW}$, a reduction of 26%. An output voltage reduction of 1 volt reduces LED current by 10% (7.3mA) power dissipation by 38%. ($7.3 \text{ mA} \times 2.2 \text{ V} \times 24 = 385 \text{ mW}$).

There are two ways to reduce the power dissipation: either a 5.1 ohm resistor or a 1 Amp diode placed in series with the display (but not in series with the ICL7107). The resistor will reduce the ICL7107 output voltage, when all 24 segments are "ON". When segments turn off, the output voltage will increase. The

diode, on the other hand, will result in a relatively steady output voltage.

In addition to limiting maximum power dissipation, the resistor reduces the change in power dissipation as the display changes. As fewer segments are "ON," each "ON" output drops more voltage and current. For the best case of six segments (a "111" display) to worst case (a "1888" display) the resistor will change about 230 mW. While a circuit without the resistor will change about 470 mW. Therefore, the resistor will reduce the variation of power dissipation by about 50%.

The change in LED brightness caused by the resistor is almost unnoticeable as more segments turn off. If steady display brightness is very important, a diode is recommended.

■ Typical Applications

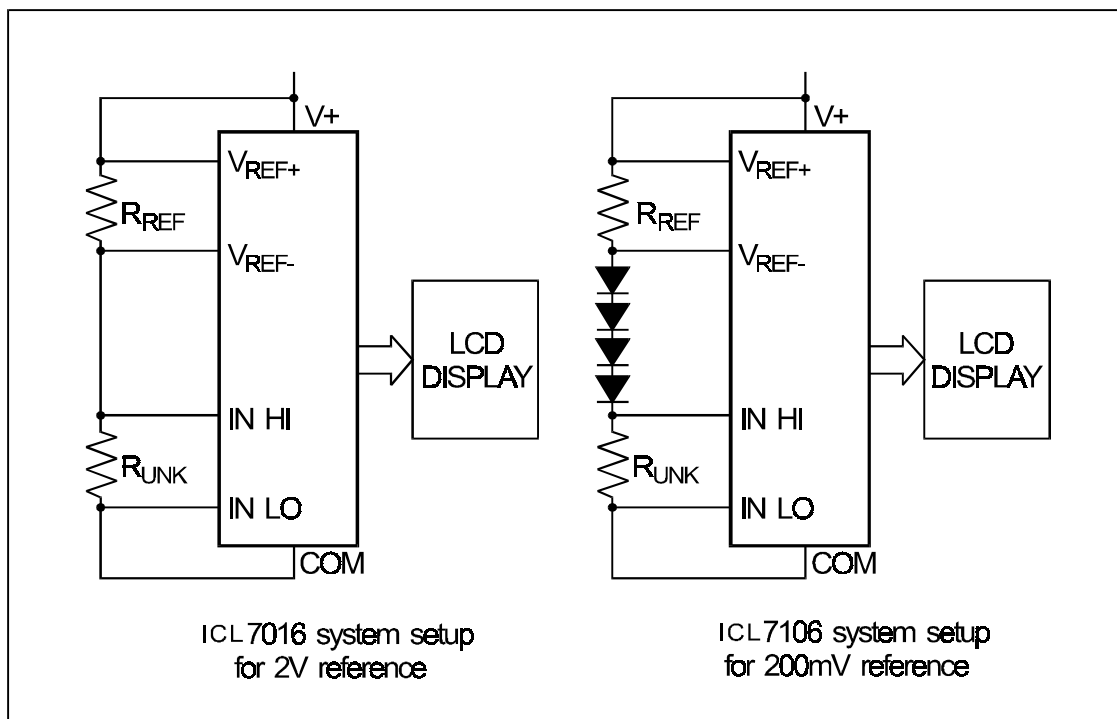


Figure 11. Ratiometric Resistance Measurement

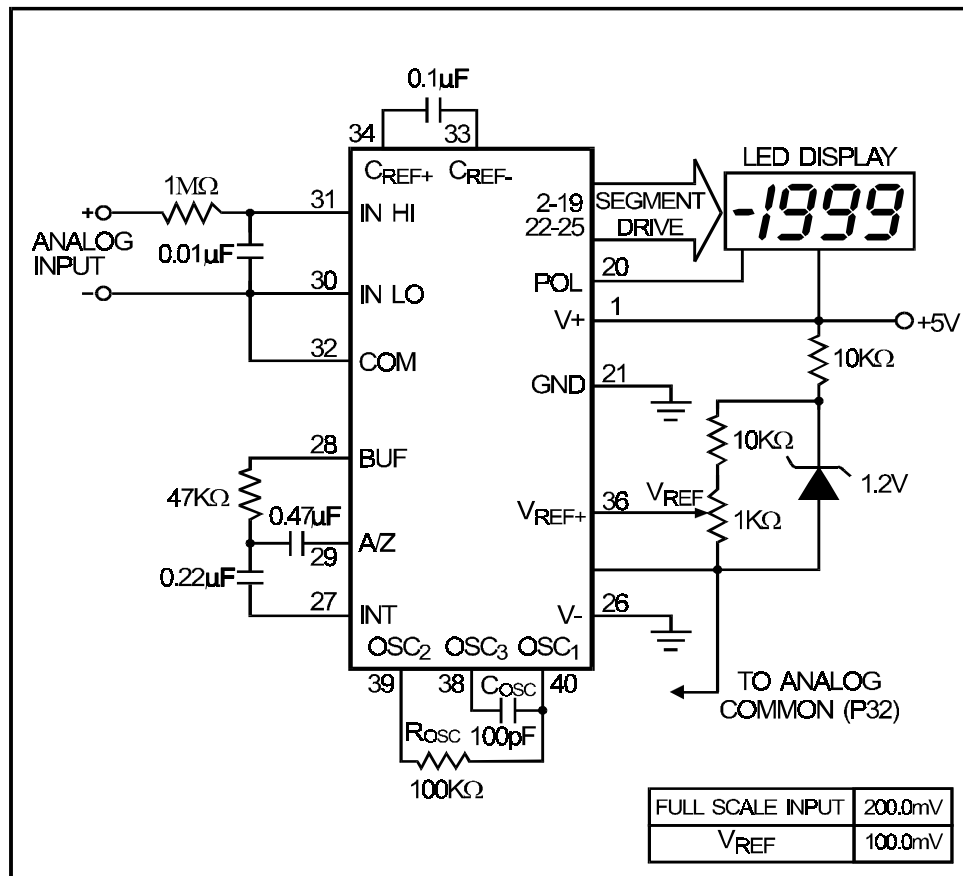


Figure 12. Operating ICL7107 from a single 5V Supply

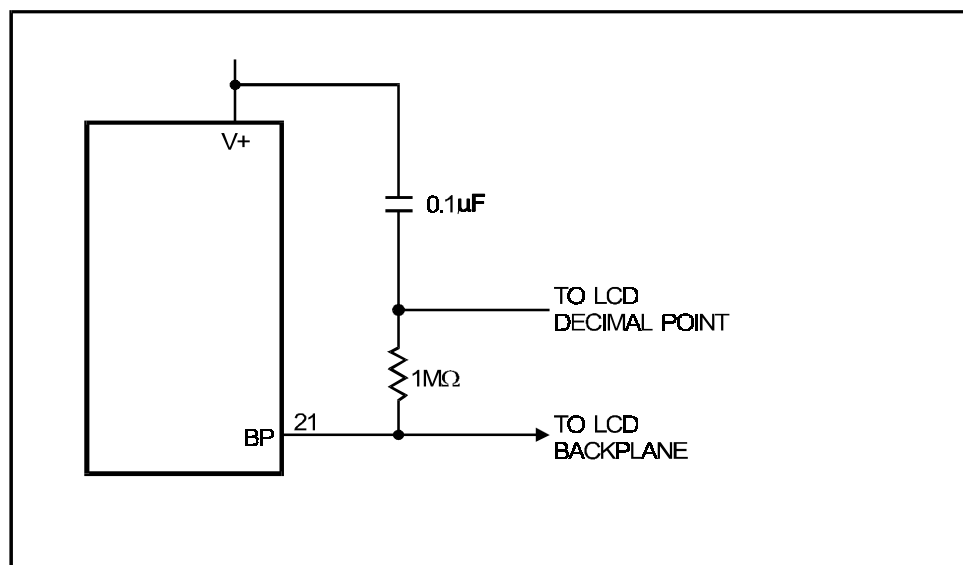


Figure 13. Fixed decimal point drivers

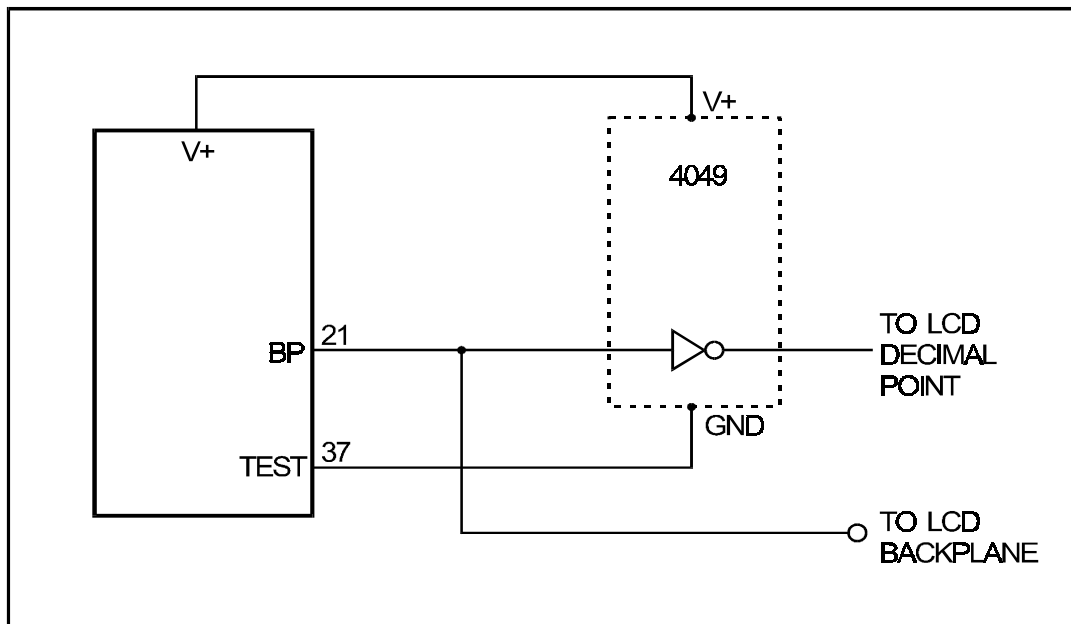


Figure 14. Fixed decimal point drivers

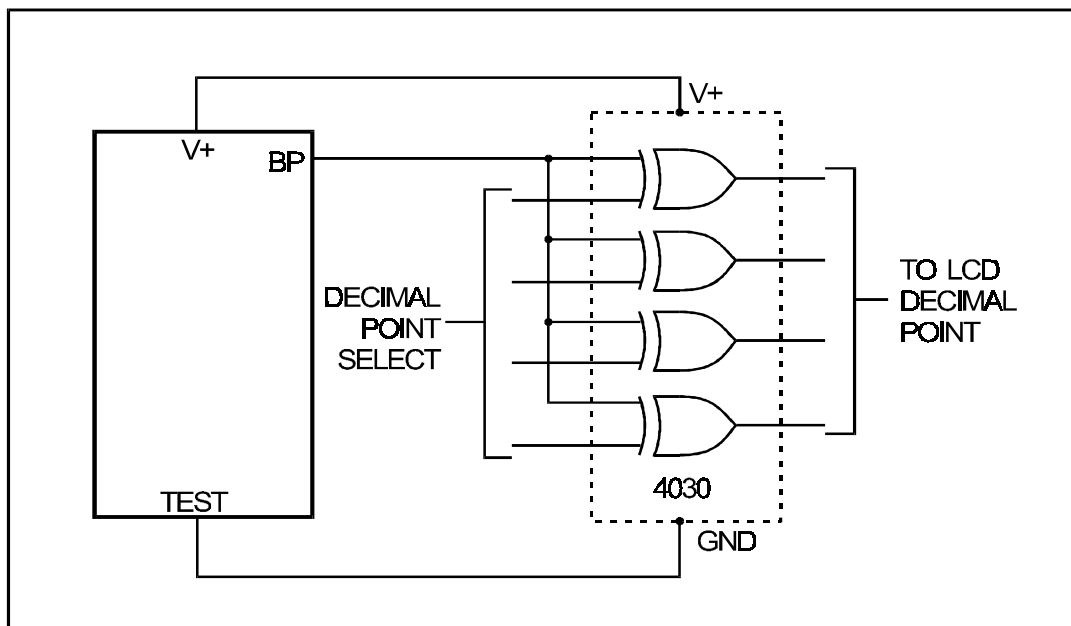


Figure 15. Decimal Point Drivers with Select

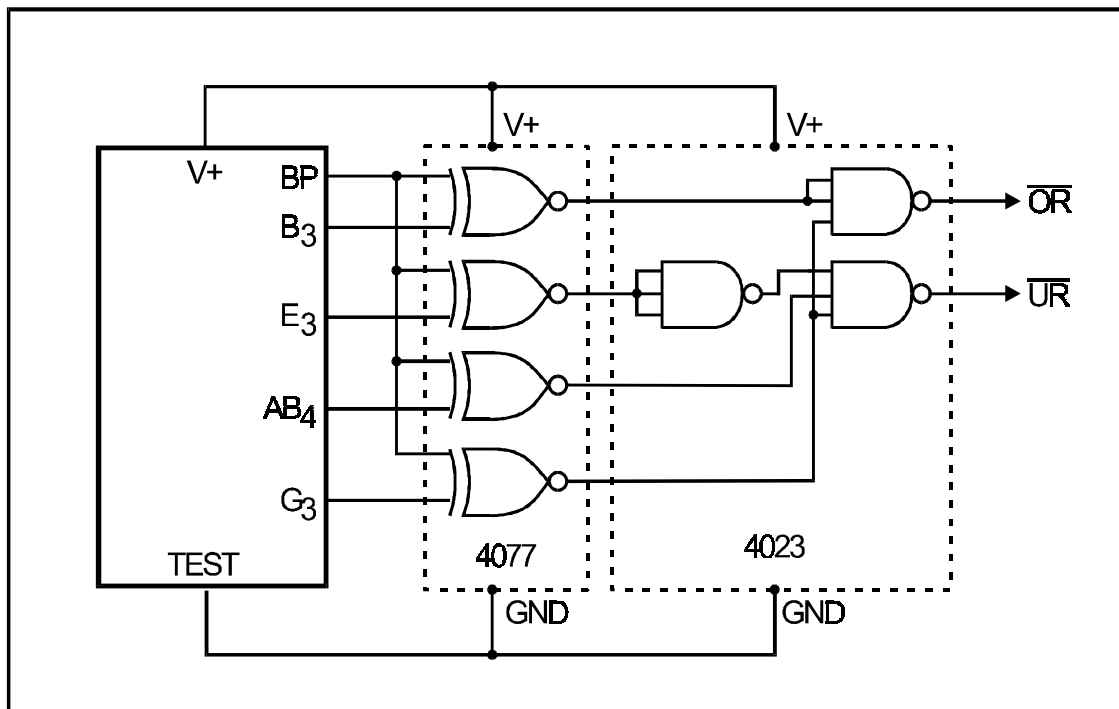


Figure 16. Generating Under Range and Over Range Signals

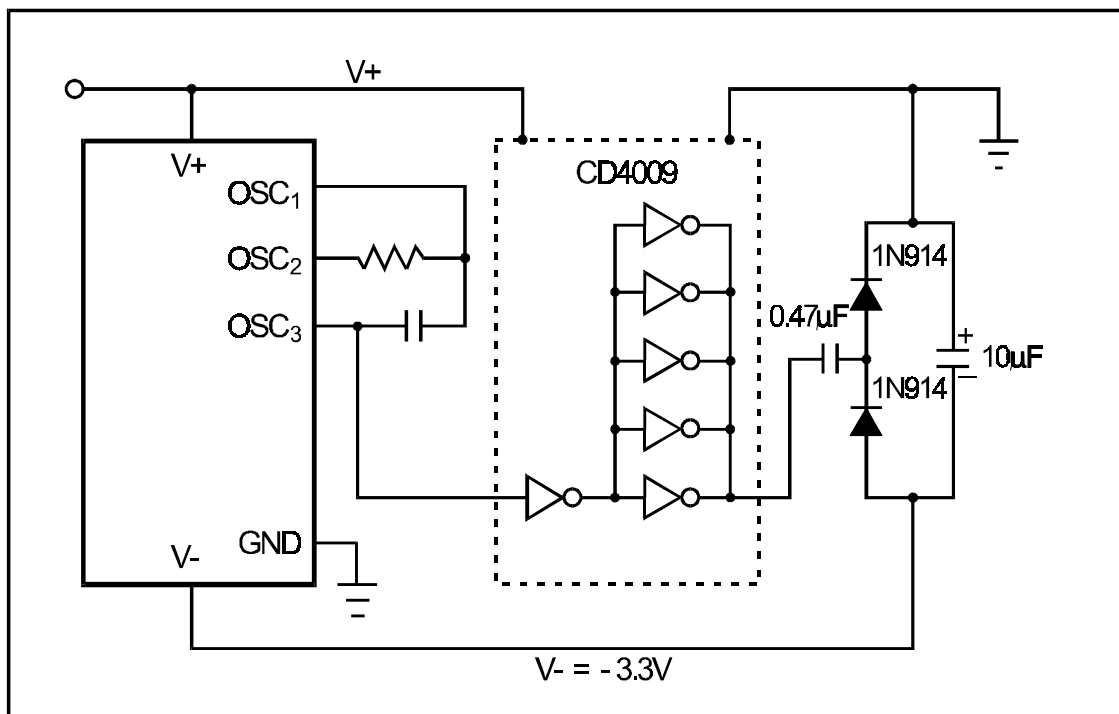


Figure 17. Generating Negative Supply from +5V

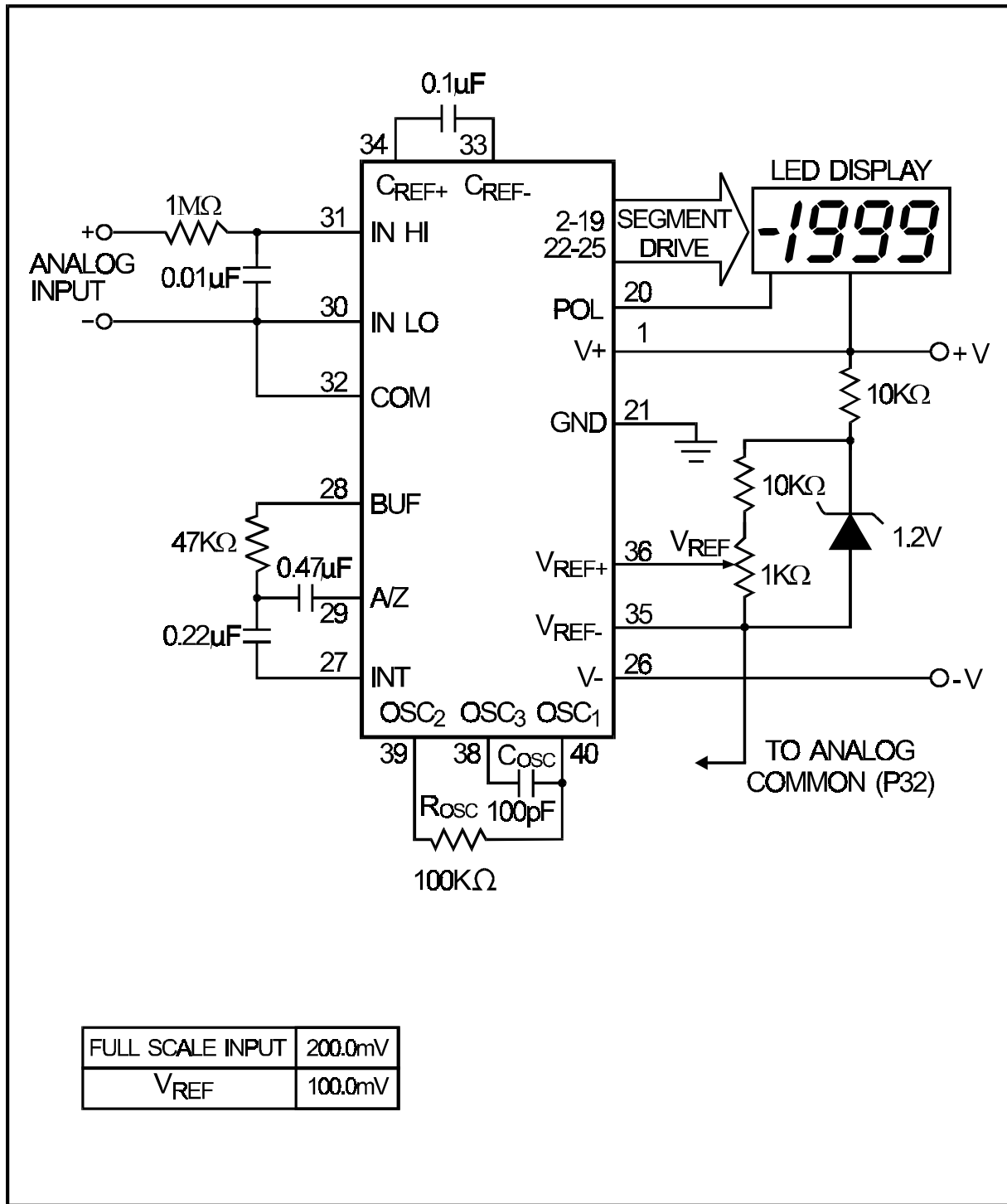
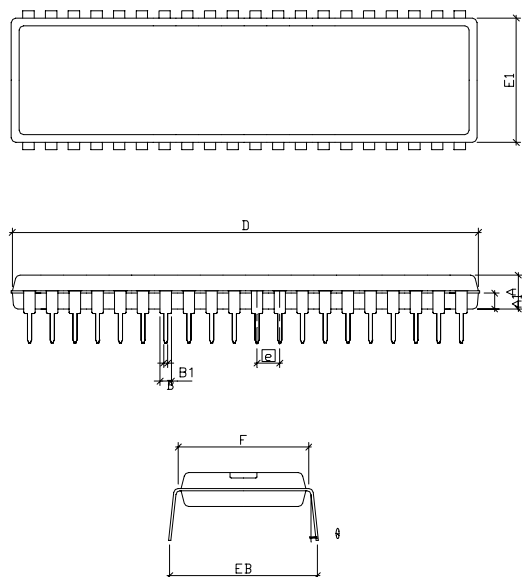


Figure 18. ICL7107 with 1.2V External Band-gap Reference

■ Package Dimension

PDIP-40



SYMBOLS	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.150	0.165	0.0059	0.0065
A₁	0.072 (TYP)		0.0028	
B	0.018(TYP)		0.0007	
B₁	0.050(TYP)		0.0020	
D	2.049	2.074	0.0807	0.0817
E₁	0.540	0.555	0.0213	0.0219
F	0.600(TYP)		0.0236	
e	0.100(TYP)		0.0039	
E_B	0.600	0.700	0.0236	0.0276
θ	0°	15°	0°	15°