HOLT INTEGRATED CIRCUITS INC.

# HI-8591

August 2006

## ARINC 429 LINE RECEIVER

## DESCRIPTION

The HI-8591 is an ARINC 429 bus interface receiver designed to operate from a single 3.3 V or 5 V supply. The part is designed with high-impedance inputs to minimize bus loading, and has an exceptional input common-mode performance in excess of +/- 30V, making it immune to ground offsets around the aircraft. The RINA and RINB inputs of the standard HI-8591 may be connected directly to the ARINC 429 bus. To enable external lightning protection circuitry to be added, the HI-8591-40 variant is available. The HI-8591-40 requires only the addition of external 40 KΩ, ¼ watt resistors in series with RINA and RINB to allow the part to meet the lightning protection requirements of DO-160D level 3.

The typical 10 volt differential ARINC 429 signal is translated and input to a window comparator and latch. The comparator levels are set just below the standard 6.5 volt minimum ARINC data threshold and just above the standard 2.5 volt maximum ARINC null threshold.

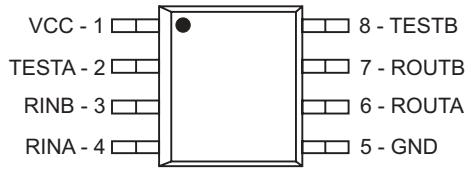
The TESTA and TESTB inputs bypass the analog inputs for testing purposes. Also if TESTA and TESTB are both taken high, the digital outputs are forced to zero.

See Holt Application Note AN-300 for more information on lightning protection.

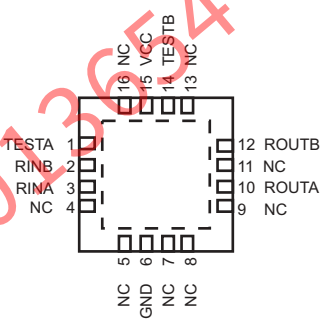
## FEATURES

- ARINC 429 line receiver interface in a small outline package
- 3.3V single rail supply voltage
- +/-30 V common-mode performance
- >140 KOhm input impedance
- Lightning protection simplified with the ability to add 40 KOhm external series resistors
- Receiver input hysteresis at least 2 volt
- Test inputs bypass analog inputs and force digital outputs to a one, zero or null state

## PIN CONFIGURATIONS




**HI-8591PSI, HI-8591PST & HI-8591PSM**
**HI-8591PSI-40, HI-8591PST-40 & HI-8591PSM-40**
**8 - PIN PLASTIC NARROW BODY SOIC**




**HI-8591PCI, HI-8591PCT, HI-8591PCI-40 & HI-8591PCT-40**
**16- pin 4mm x 4mm Chip-scale package**

## SUPPLY VOLTAGES

VCC = 3.3V ± 10%, 5.0V ± 10%

## FUNCTION TABLE

| RINA | RINB | TESTA | TESTB | ROUTA | ROUTB |
|---|---|---|---|---|---|
| -1.25V to 1.25V | -1.25V to 1.25V | 0 | 0 | 0 | 0 |
| -3.25V to -6.5V | 3.25V to 6.5V | 0 | 0 | 0 | 1 |
| 3.25V to 6.5V | -3.25V to -6.5V | 0 | 0 | 1 | 0 |
| X | X | 0 | 1 | 0 | 1 |
| X | X | 1 | 0 | 1 | 0 |
| X | X | 1 | 1 | 0 | 0 |

## PIN DESCRIPTION TABLE

| SYMBOL | FUNCTION | DESCRIPTION |
|---|---|---|
| VCC | SUPPLY | 3.3V or 5V SUPPLY |
| TESTA | LOGIC INPUT | CMOS |
| RINB | ARINC INPUT | RECEIVER B INPUT |
| RINA | ARINC INPUT | RECEIVER A INPUT |
| GND | POWER | GROUND |
| ROUTA | LOGIC OUTPUT | RECEIVER CMOS OUTPUT A |
| ROUTB | LOGIC OUTPUT | RECEIVER CMOS OUTPUT B |
| TESTB | LOGIC INPUT | CMOS |

# FUNCTIONAL DESCRIPTION

RECEIVER

Figure 1 shows the general architecture of the ARINC 429 receiver. The receiver operates off the VCC supply only. The inputs RINA and RINB each require 140KΩ of resistance between the ARINC bus and comparator. This resistance is completely on-chip for the HI-8591. In contrast, the HI-8591-40 has 100 KΩ on-chip and requires an external 40KΩ, ¼ watt resistor on each of the ARINC 429 input pins. The HI-8591-40 device is typically chosen for applications where lightning protection is a requirement.

After level translation, the inputs are buffered and become inputs to a differential amplifier. The amplitude of the differential signal is compared to levels derived from a divider between V.C. and Ground. The nominal settings correspond to a One/Zero amplitude of 6.0V and a Null amplitude of 3.3V.

The status of the ARINC receiver input is latched. A Null input resets the latches and a One or Zero input sets the latches.

The logic at the output is controlled by the test signal which is generated by the logical OR of the TESTA and TESTB pins. If TESTA and TESTB are both One, the HI-8591 outputs are pulled low. This allows the digital outputs of a transmitter to be connected to the test inputs through control logic for system self-test purposes.

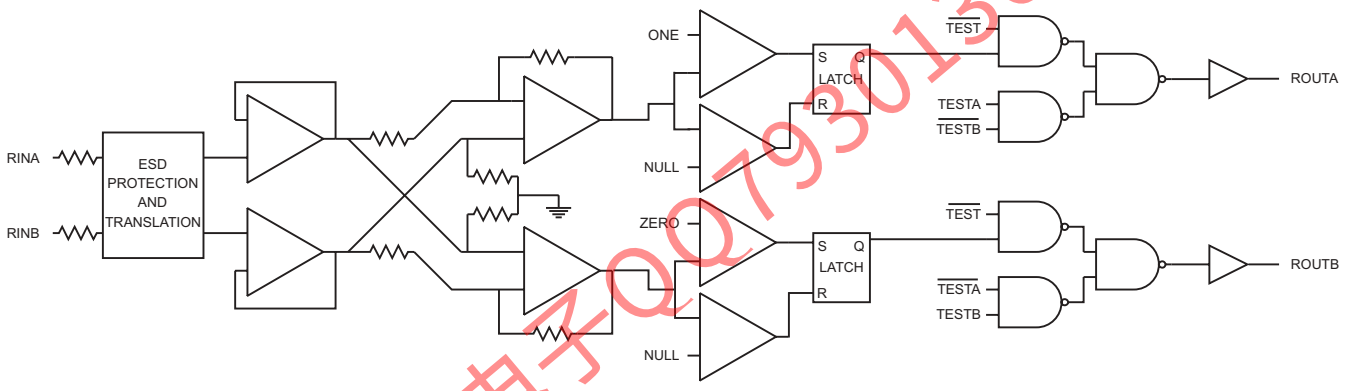



FIGURE 1 - RECEIVER BLOCK DIAGRAM



## APPLICATION INFORMATION

Figure 2 shows a possible application of the HI-8591 interfacing an ARINC 429 bus input to a 3.3V ASIC or FPGA. In this example a HI-8586 ARINC 429 line driver is used to take 3.3V logic outputs and generate the necessary 10V differential signal for driving an ARINC 429 bus.

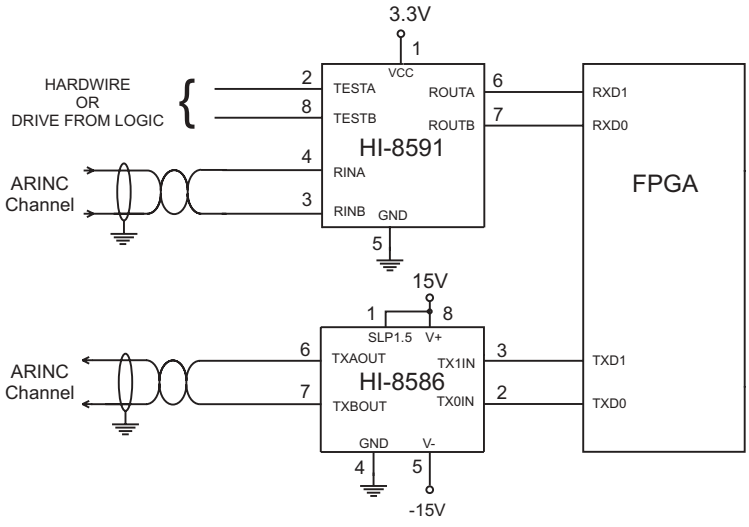



FIGURE 2 - APPLICATION DIAGRAM

## ABSOLUTE MAXIMUM RATINGS

Voltages referenced to Ground

Supply voltages
VCC.....-0.3V to +7V

ARINC input - pins 3 & 4
Voltage at either pin.....+120V to -120V

DC current per input pin..... ±10mA

Power dissipation at 25°C
plastic DIP.....0.7W
ceramic DIP.....0.5W

Solder Temperature .....275°C for 10 sec

Storage Temperature.....-65°C to +150°C

## RECOMMENDED OPERATING CONDITIONS

Supply Voltages
VCC.....3.3V to 5V ± 10%

Temperature Range
Industrial Screening.....-40°C to +85°C
Hi-Temp Screening.....-55°C to +125°C
Military Screening.....-55°C to +125°C

*NOTE: Stresses above absolute maximum ratings or outside recommended operating conditions may cause permanent damage to the device. These are stress ratings only. Operation at the limits is not recommended.*

## DC ELECTRICAL CHARACTERISTICS

OPERATING TEMPERATURE RANGE, VCC = 3.3V ± 10% or 5.0V ± 10% UNLESS OTHERWISE STATED

| PARAMETERS | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| ARINC input voltage | | | | | | |
| one or zero | $V_{DIN}$ | Differential volt., pins 3 & 4 | 6.5 | 10 | 13 | volts |
| null | $V_{NIN}$ | " " " | - | - | 2.5 | volts |
| common mode | $V_{COM}$ | with respect to ground | -30.0 | - | +30.0 | volts |
| logic input voltage | | | | | | |
| high | $V_{IH}$ | | 70% VCC | - | - | volts |
| low | $V_{IL}$ | | - | - | 30% VCC | volts |
| ARINC input resistance | | | | | | |
| RINA to RINB | $R_{DIFF}$ | Supplies floating | - | 140 | - | KΩ |
| RINA or RINB to GND | $R_{GND}$ | " " | - | 140 | - | KΩ |
| RINA or RINB to VCC | $R_{VCC}$ | " " | - | 100 | - | KΩ |
| logic input current | | | | | | |
| source | $I_{IH}$ | $V_{IN}$ = 2.0V | - | - | 20.0 | µA |
| sink | $I_{IL}$ | $V_{IN}$ = 0.8V | - | - | 20.0 | µA |
| logic output drive voltage | | | | | | |
| one | $V_{OH1}$ | VCC = 5V ± 10% $I_{OH}$ = 5mA | 2.4 | - | - | V |
| | $V_{OH2}$ | VCC= 3.3V ± 10% $I_{OH}$ = 1.5mA | 2.4 | - | - | V |
| zero | $V_{OL1}$ | VCC = 5V ± 10% $I_{OH}$ = 5mA | - | - | 0.5 | V |
| | $V_{OL2}$ | VCC = 3.3V ± 10% $I_{OH}$ = 1.5mA | - | - | 0.4 | V |
| Current drain | | | | | | |
| operating | $I_{CC1}$ | pins 2, 8 = 0V; pins 3, 4 open | - | 1.5 | 5.0 | mA |

## AC ELECTRICAL CHARACTERISTICS

OPERATING TEMPERATURE RANGE, VCC = 3.3V ± 10% or 5.0V ± 10% UNLESS OTHERWISE STATED

| PARAMETERS | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Receiver propagation delay | | defined in Figure 3, $C_L$= 50pF | | | | |
| Output high to low | $t_{phlr}$ | VCC = 3.3V ± 10% | - | 600 | 1000 | ns |
| | | VCC = 5.0V ± 10% | - | 600 | 900 | ns |
| Output low to high | $t_{plhr}$ | VCC = 3.3V ± 10% | - | 600 | 1000 | ns |
| | | VCC = 5.0V ± 10% | - | 600 | 900 | ns |
| TEST pin propagation delay | | defined in Figure 4, $C_L$= 50pF | | | | |
| Output high to low | $t_{pth}$ | VCC = 3.3V ± 10% | - | - | 100 | ns |
| | | VCC = 5.0V ± 10% | - | - | 60 | ns |
| Output low to high | $t_{ptl}$ | VCC = 3.3V ± 10% | - | - | 100 | ns |
| | | VCC = 5.0V ± 10% | - | - | 60 | ns |
| Receiver output transition times | | VCC = 3.3V or 5.0V ± 10% | | | | |
| Output high to low | $t_{fr}$ | | - | 15 | 50 | ns |
| Output low to high | $t_{rr}$ | | - | 15 | 50 | ns |
| Input capacitance (1) | | | | | | |
| ARINC differential | $C_{AD}$ | | - | 5 | 10 | pF |
| ARINC single ended to Ground | $C_{AS}$ | | - | - | 10 | pF |
| Logic | $C_{IN}$ | | - | - | 10 | pF |

Notes: 1. Guaranteed but not tested

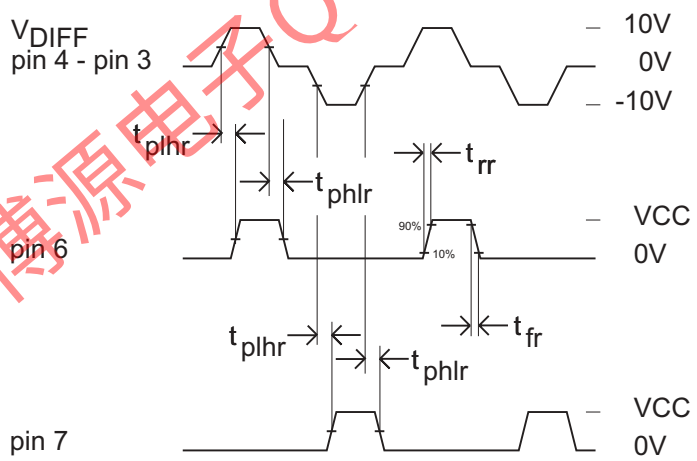



FIGURE 3 - RECEIVER TIMING

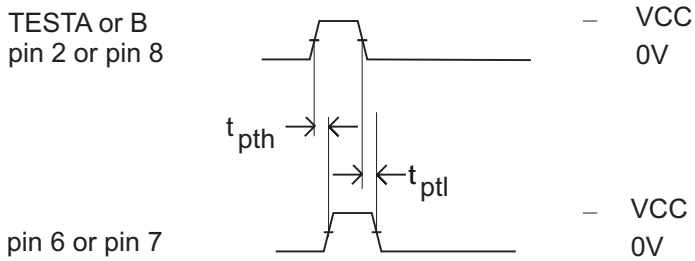



FIGURE 4 - TEST PIN TIMING

# ORDERING INFORMATION

**HI - 8591 xx x x - xx**

| PART NUMBER | INPUT SERIES RESISTANCE | |
|---|---|---|
| | BUILT-IN | REQUIRED EXTERNALLY |
| No dash number | 140 Kohm | 0 |
| -40 | 100 Kohm | 40 Kohm |

| PART NUMBER | LEAD FINISH |
|---|---|
| Blank | Tin / Lead (Sn / Pb) Solder |
| F | 100% Matte Tin (Pb-free, RoHS compliant) |

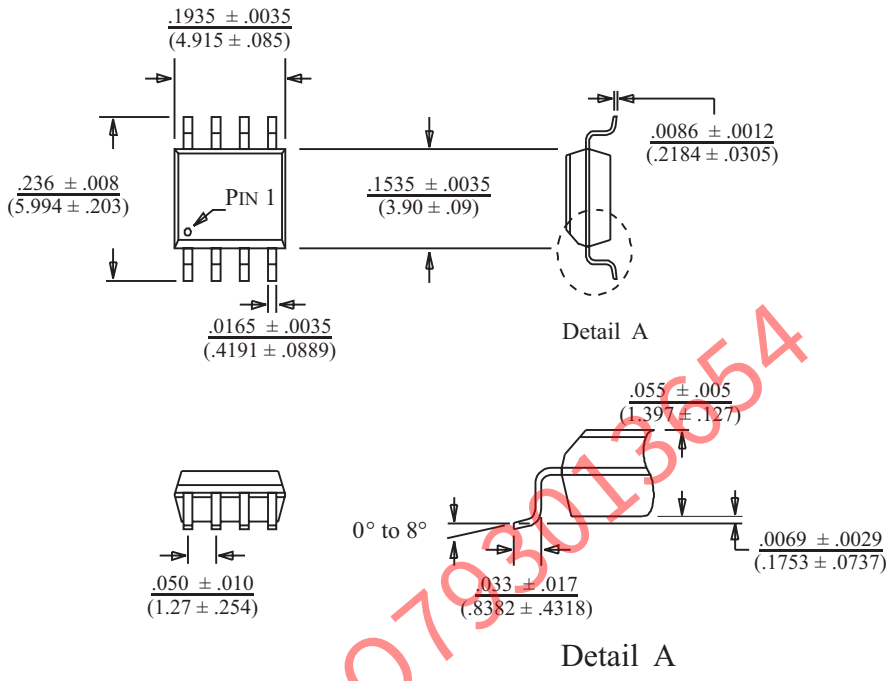
| PART NUMBER | TEMPERATURE RANGE | FLOW | BURN IN |
|---|---|---|---|
| I | -40°C TO +85°C | I | NO |
| T | -55°C TO +125°C | T | NO |
| M | -55°C TO +125°C | M | YES |

| PART NUMBER | PACKAGE DESCRIPTION |
|---|---|
| PC | 8 PIN PLASTIC 4 X 4 mm CHIP SCALE (not available with “M” flow) |
| PD | 8 PIN PLASTIC DIP (not available with “M” flow) |
| PS | 8 PIN PLASTIC NARROW BODY SOIC |
| CR | 8 PIN CERDIP (not available Pb-free) |

## 8-PIN PLASTIC SMALL OUTLINE (SOIC) - NB

(Narrow Body)

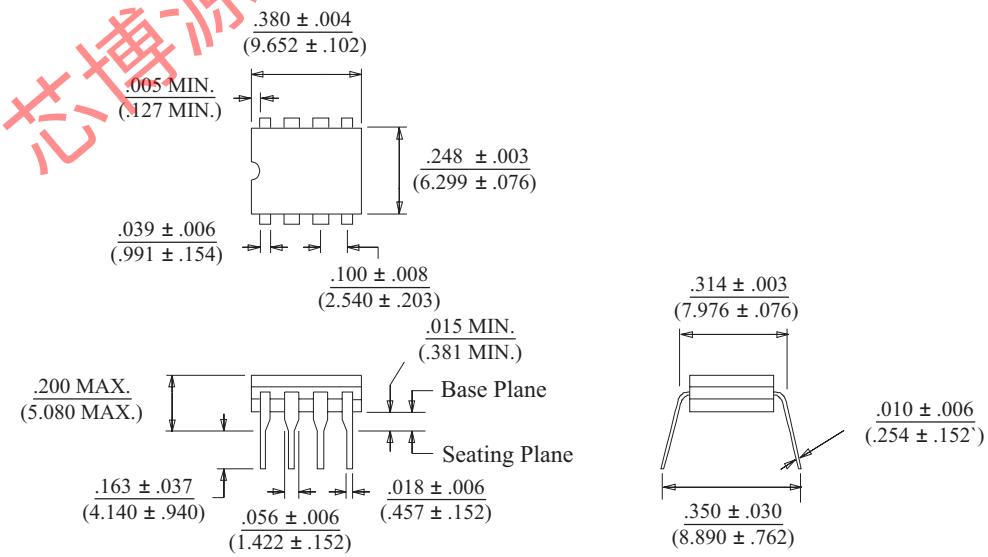
Package Type: 8HN






## 8-PIN CERDIP

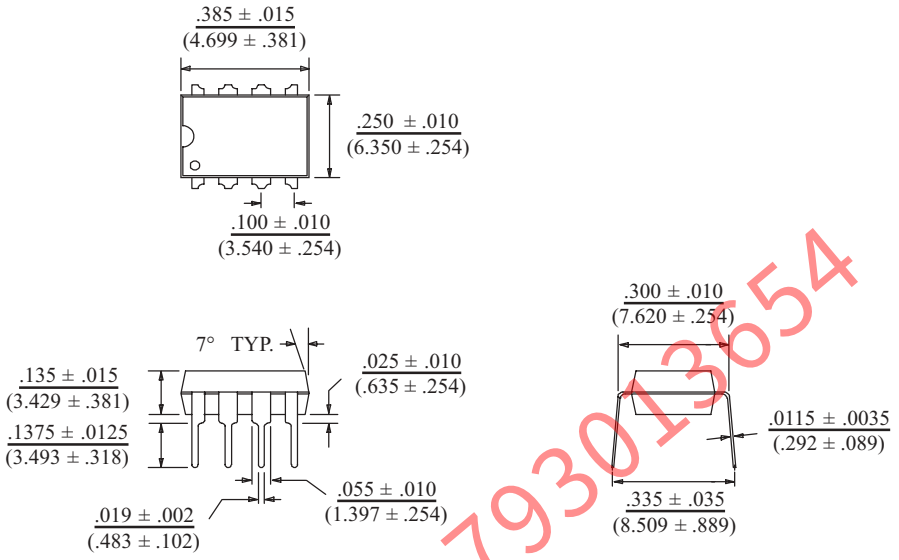
Package Type: 8D



*inches (millimeters)*

## 8-PIN PLASTIC DIP

Package Type: 8P




*millimeters*

## 16-PIN PLASTIC CHIP-SCALE PACKAGE