LONTIUM SEMICONDUCTOR CORPORATION

ClearEdge™ Technology

LT7911

Type-C/DP/eDP to Quad-port MIPI DSI/CSI with Audio

Datasheet

1. Features

- **Type-C**
  - Compliant with VESA DisplayPort Alt Mode on USB Type-C Standard version1.0
  - Compliant with USB Power Delivery Rev.2.0
  - Compatible with USB Type-C V1.1
  - Built-in CC controller for plug and orientation detection
  - Dual-port CC for charger and normal communication.
- **DP/eDP Receiver**
  - Compliant with DisplayPort Specification 1.2 for 1.62Gbps, 2.7Gbps ,5.4Gbps
  - Compliant with DisplayPort Specification version 1.2 and Embedded DisplayPort (eDP) Specification version 1.4
  - Support DisplayPort 1, 2，4 lanes
  - Support HDCP 1.3
  - Support eDP Authentication: Alternative Scramble Seed Reset and Alternative Framing
  - Fast and full Link Training for embedded DisplayPort system
  - Adaptive DisplayPort Receiver Equalization for PCB, cable and connector losses
  - Support AUX and IIC for firmware updating
- **Single/Dual-Port/Quad-Port MIPI® DSI/CSI Transmitter**
  - Compliant with DCS1.02, D-PHY1.2& DSI1.02 &CSI-2 1.0
  - 1 Clock Lane, and 1~4 Configurable Data Lanes per port
  - 1/2/4 configurable port
  - 80Mb/s~1.5Gb/s per Data Lane
  - Data Lane and Polarity Swapping
  - Maximum 64Pixels overlap for each half
  - Burst Mode and Command ModeSupported
  - Support RGB666, Loosely RGB666, RGB888, RGB565, 16-bit YCbCr4:2:2,20-bit YCbCr4:2:2,24-bit YCbCr 4:2:2, 12-bit YCbCr4:2:0Video Format
  - Video stream copy mode for each single/dual-port
  - Side-by-side 3D support
  - Port swap
- **Miscellaneous**
  - 3.3V/1.2V Supply Power
  - Internal CSC support conversions between YCbCr 4:4:4 and RGB, and between YCbCr 4:2:2 and YCbCr 4:4:4
  - Support SPDIF and 8-channel IIS audio output
  - Support 100KHz and 400KHz I2C slave
  - Power from phone or adapter mode selection
  - Integrated Microprocessor
  - Embedded EDID shadow.
  - Temperature Range: -40°C ~ +85°C
  - ESD 4kV HBM

2. Description

The LT7911 is a high performance Type-C/DP1.2 to MIPI®DSI/CSI chip for VR/Smart phone/Display application.

For DP1.2 input, LT7911 can be configured as 1,2,4 lane, also support lane swap function. Adaptive equalization makes it suitable for long cable application and the maximum bandwidth is up to 21.6Gbps

For MIPI®DSI/CSI output, LT7911 features configurable single-port or dual-port or quad-port MIPI®DSI/CSI with 1 high-speed clock lane and 1~4 high-speed data lanes operating at maximum 1.5Gb/s/lane, which can support a totalbandwidth of up to 24Gbps. LT7911 supports Burst mode DSI video data transferring, also support flexible video data mapping path.

For 2D video stream, the same video stream can be mapped to two separated panel, for 3D video format, left side data can be sent to one panel, and right side data can be sent to another panel.

With sophisticated MCU and the Embedded Flash, LT7911 support EDID buffer, DP/eDP input detection and determine to enter into power saving mode automatically. When the receiver of LT7911 locks the input signal, MCU can read the recovered timing parameters by MSA registers to match the ASSR. The DPCD registers are accessible via system I2C when debugging the full link training. Once the fast link training used, system time will save at least 400ms.

3. Applications

- Mobile system
- VR

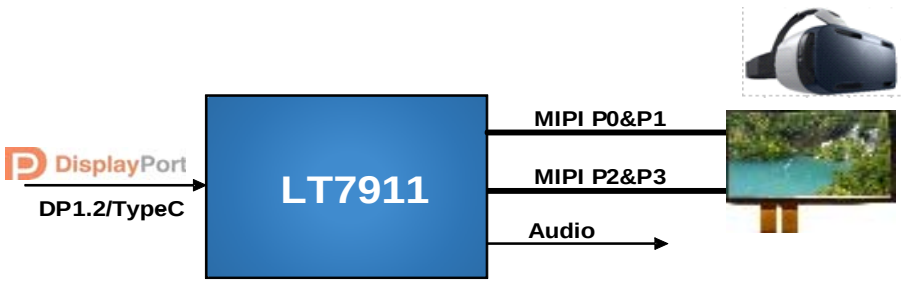

Figure 3.1 Application Diagram

4. Ordering Information

Table 4.1 Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
LT7911	-40℃ to+85℃	QFN128 (14*14)	Tray

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5. Revision History

Version	Owner	Content	Date
R1.0	XF CH	Initial datasheet creation	03/09/2017
R1.1	N W	Update package information	03/28/2017
R1.2	Terry	Update pin and package information	05/22/2017
R1.3	Terry	Update about features information	07/11/2017

6. Pinning Information

6.1 Pin Configuration

To improve signal integrity, all differential pairs should be routed with 100Ω±10% differential impedance. Maximum trace length mismatch should be less than 5mil and keep total trace length to a minimum for all differential traces. Routing differential pairs on the top or bottom layer with no vias as on signal path is highly recommended.

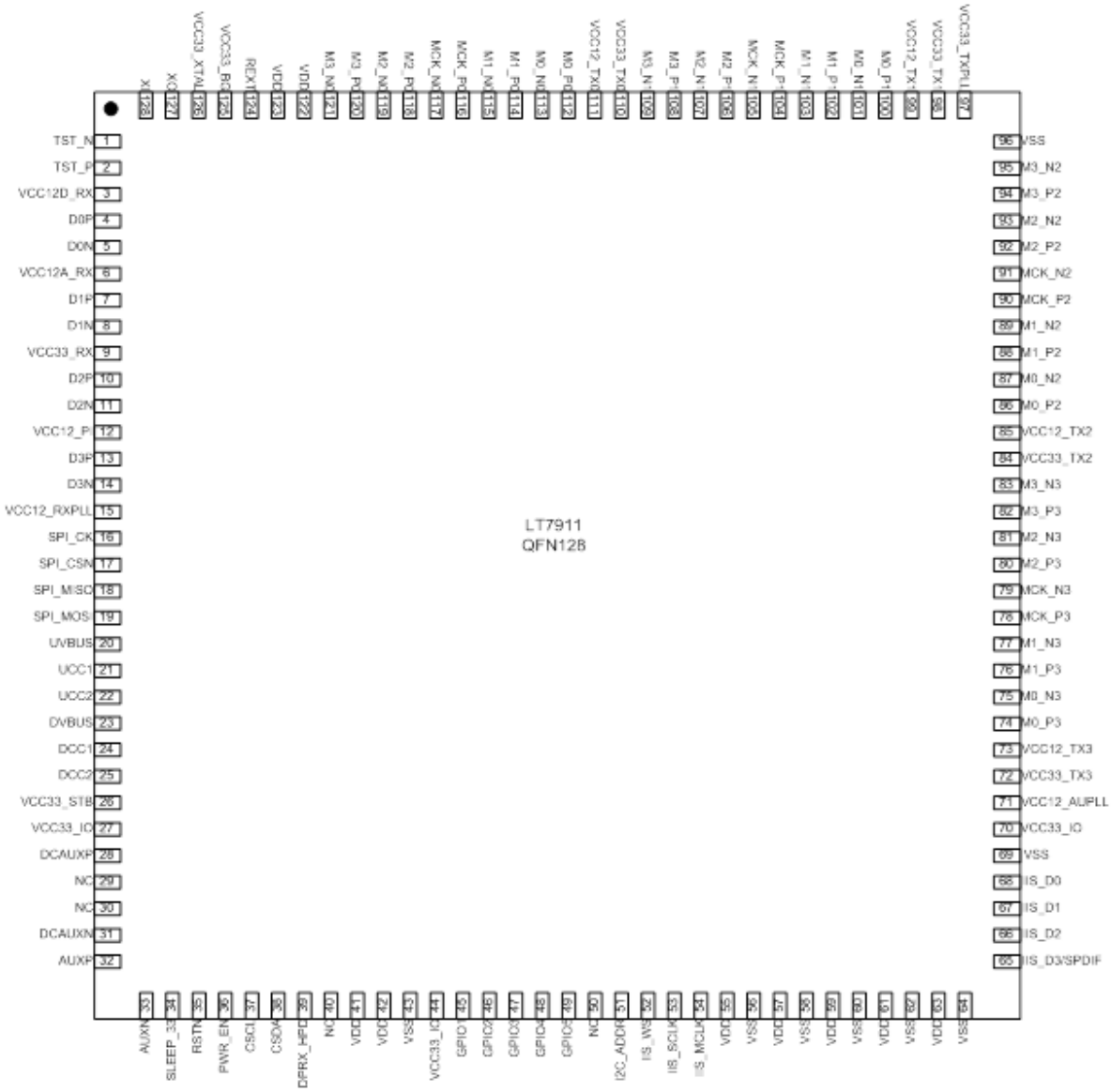


Figure 6.1.1 LT7911 Pin Assignment (Top View)

To minimize the power supply noise floor, at least one 0.1μF and one 0.01μF decoupling capacitors recommended to be installed near all the LT7911 power pins. To avoid large current loops and trace inductance, thetrace length between decoupling capacitor and device power inputs pins must be minimized.

6.2 Pin Description

Table 6.2.1 Pin Description

Pin#	Pin Name	I/O Type	I/O Dir	Description
129	EPAD	PG	I/O	Ground
43,56,58,60,62,64,69,96	VSS	PG	I/O	Ground
27,44,70	VCC33_IO	PG	I/O	3.3V IO Power
26	VCC33_STB	PG	I/O	3.3V Standby Power
126	VCC33_XTAL	PG	I/O	3.3V Power for XTAL
125	VCC33_BG	PG	I/O	3.3V Power for BG
9	VCC33_RX	PG	I/O	3.3V Power for RX
110	VCC33_TX0	PG	I/O	3.3V Power for MIPI TX Port0
98	VCC33_TX1	PG	I/O	3.3V Power for MIPI TX Port1
84	VCC33_TX2	PG	I/O	3.3V Power for MIPI TX Port2
72	VCC33_TX3	PG	I/O	3.3V Power for MIPI TX Port3
97	VCC33_TXPLL	PG	I/O	3.3V Power for TXPLL
41,42,55,57,59,61,63,122,123	VDD	PG	I/O	1.2V Core Power
71	VCC12_AUPLL	PG	I/O	1.2V Power for AUPLL
12	VCC12_PI	PG	I/O	1.2V Power for PI
15	VCC12_RXPLL	PG	I/O	1.2V Power for RXPLL
6	VCC12A_RX	PG	I/O	1.2V Power for RX Analog Part
3	VCC12D_RX	PG	I/O	1.2V Power for RX Digital Part
111	VCC12_TX0	PG	I/O	1.2V Power for MIPI TX Port0
99	VCC12_TX1	PG	I/O	1.2V Power for MIPI TX Port1
85	VCC12_TX2	PG	I/O	1.2V Power for MIPI TX Port2
73	VCC12_TX3	PG	I/O	1.2V Power for MIPI TX Port3
13	D3P	Analog	I	RX Data Channel Lane-3 Positive Input Maximum data rate is 5.4Gbps.
14	D3N	Analog	I	RX Data Channel Lane-3 Negative Input Maximum data rate is 5.4Gbps.
10	D2P	Analog	I	RX Data Channel Lane-2 Positive Input Maximum data rate is 5.4Gbps.
11	D2N	Analog	I	RX Data Channel Lane-2 Negative Input Maximum data rate is 5.4Gbps.
7	D1P	Analog	I	RX Data Channel Lane-1 Positive Input Maximum data rate is 5.4Gbps.
8	D1N	Analog	I	RX Data Channel Lane-1 Negative Input Maximum data rate is 5.4Gbps.
4	D0P	Analog	I	RX Data Channel Lane-0 Positive Input Maximum data rate is 5.4Gbps.
5	D0N	Analog	I	RX Data Channel Lane-0 Negative Input Maximum data rate is 5.4Gbps.
32	AUXP	Analog	I/O	AUX Positive Input
33	AUXN	Analog	I/P	AUX Negative Input
28	DCAUXP	Schmitt	I	DCAUXP for DP Source Connection Detect
31	DCAUXN	Schmitt	I	DCAUXN for DP Source Connection Detect
24	DCC1	Analog	I/O	CC1 Connected with Adapter

Pin#	Pin Name	I/O Type	I/O Dir	Description
25	DCC2	**Analog**	**I/O**	**CC2 Connected with Adapter**
23	DVBUS	**Analog**	**I**	**One Tenth of VBUS Connected with Adapter**
21	UCC1	**Analog**	**I/O**	**CC1 Connected with Source**
22	UCC2	**Analog**	**I/O**	CC2 Connected with Adapter
20	UVBUS	**Analog**	**I**	One Tenth of VBUS Connected with Source
128	XI	**Analog**	**I/O**	**XTAI for Debug**
127	XO	**Analog**	**I/O**	**XTAO for Debug**
120	M3_P0	**Analog**	**O**	**MIPI TX Port0/Lane3 Channel Positive Input** Maximum data rate is 1.5Gbps.
121	M3_N0	**Analog**	**O**	**MIPI TX Port0/Lane3 Channel Negative Input** Maximum data rate is 1.5Gbps.
118	M2_P0	**Analog**	**O**	**MIPI TX Port0/Lane2 Channel Positive Input** Maximum data rate is 1.5Gbps.
119	M2_N0	**Analog**	**O**	**MIPI TX Port0/Lane2 Channel Negative Input** Maximum data rate is 1.5Gbps.
116	MCK_P0	**Analog**	**O**	**MIPI TX Port0/Clock Channel Positive Input** Maximum Frequency is 750MHz.
117	MCK_N0	**Analog**	**O**	**MIPI TX Port0/Clock Channel Negative Input** Maximum Frequency is 750MHz.
114	M1_P0	**Analog**	**O**	**MIPI TX Port0/Lane1 Channel Positive Input** Maximum data rate is 1.5Gbps.
115	M1_N0	**Analog**	**O**	**MIPI TX Port0/Lane1 Channel Negative Input** Maximum data rate is 1.5Gbps.
112	M0_P0	**Analog**	**O**	**MIPI TX Port0/Lane0 Channel Positive Input** Maximum data rate is 1.5Gbps.
113	M0_N0	**Analog**	**O**	**MIPI TX Port0/Lane0 Channel Negative Input** Maximum data rate is 1.5Gbps.
108	M3_P1	**Analog**	**O**	**MIPI TX Port1/Lane3 Channel Positive Input** Maximum data rate is 1.5Gbps.
109	M3_N1	**Analog**	**O**	**MIPI TX Port1/Lane3 Channel Negative Input** Maximum data rate is 1.5Gbps.
106	M2_P1	**Analog**	**O**	**MIPI TX Port1/Lane2 Channel Positive Input** Maximum data rate is 1.5Gbps.
107	M2_N1	**Analog**	**O**	**MIPI TX Port1/Lane2 Channel Negative Input** Maximum data rate is 1.5Gbps.
104	MCK_P1	**Analog**	**O**	**MIPI TX Port1/Clock Channel Positive Input** Maximum Frequency is 750MHz.
105	MCK_N1	**Analog**	**O**	**MIPI TX Port1/Clock Channel Negative Input** Maximum Frequency is 750MHz.
102	M1_P1	**Analog**	**O**	**MIPI TX Port1/Lane1 Channel Positive Input** Maximum data rate is 1.5Gbps.
103	M1_N1	**Analog**	**O**	**MIPI TX Port1/Lane1 Channel Negative Input** Maximum data rate is 1.5Gbps.
100	M0_P1	**Analog**	**O**	**MIPI TX Port1/Lane0 Channel Positive Input** Maximum data rate is 1.5Gbps.
101	M0_N1	**Analog**	**O**	**MIPI TX Port1/Lane0 Channel Negative Input** Maximum data rate is 1.5Gbps.
94	M3_P2	**Analog**	**O**	**MIPI TX Port2/Lane3 Channel Positive Input** Maximum data rate is 1.5Gbps.
95	M3_N2	**Analog**	**O**	**MIPI TX Port2/Lane3 Channel Negative Input** Maximum data rate is 1.5Gbps.
92	M2_P2	**Analog**	**O**	**MIPI TX Port2/Lane2 Channel Positive Input** Maximum data rate is 1.5Gbps.
93	M2_N2	**Analog**	**O**	**MIPI TX Port2/Lane2 Channel Negative Input** Maximum data rate is 1.5Gbps.

Pin#	Pin Name	I/O Type	I/O Dir	Description
90	MCK_P2	Analog	O	**MIPI TX Port2/Clock Channel Positive Input** Maximum Frequency is 750MHz.
91	MCK_N2	Analog	O	**MIPI TX Port2/Clock Channel Negative Input** Maximum Frequency is 750MHz.
88	M1_P2	Analog	O	**MIPI TX Port2/Lane1 Channel Positive Input** Maximum data rate is 1.5Gbps.
89	M1_N2	Analog	O	**MIPI TX Port2/Lane1 Channel Negative Input** Maximum data rate is 1.5Gbps.
86	M0_P2	Analog	O	**MIPI TX Port2/Lane0 Channel Positive Input** Maximum data rate is 1.5Gbps.
87	M0_N2	Analog	O	**MIPI TX Port2/Lane0 Channel Negative Input** Maximum data rate is 1.5Gbps.
82	M3_P3	Analog	O	**MIPI TX Port3/Lane3 Channel Positive Input** Maximum data rate is 1.5Gbps.
83	M3_N3	Analog	O	**MIPI TX Port3/Lane3 Channel Negative Input** Maximum data rate is 1.5Gbps.
80	M2_P3	Analog	O	**MIPI TX Port3/Lane2 Channel Positive Input** Maximum data rate is 1.5Gbps.
81	M2_N3	Analog	O	**MIPI TX Port3/Lane2 Channel Negative Input** Maximum data rate is 1.5Gbps.
78	MCK_P3	Analog	O	**MIPI TX Port3/Clock Channel Positive Input** Maximum Frequency is 750MHz.
79	MCK_N3	Analog	O	**MIPI TX Port3/Clock Channel Negative Input** Maximum Frequency is 750MHz.
76	M1_P3	Analog	O	**MIPI TX Port3/Lane1 Channel Positive Input** Maximum data rate is 1.5Gbps.
77	M1_N3	Analog	O	**MIPI TX Port3/Lane1 Channel Negative Input** Maximum data rate is 1.5Gbps.
74	M0_P3	Analog	O	**MIPI TX Port3/Lane0 Channel Positive Input** Maximum data rate is 1.5Gbps.
75	M0_N3	Analog	O	**MIPI TX Port3/Lane0 Channel Negative Input** Maximum data rate is 1.5Gbps.
2	TST_P	Analog	O	**For Debug**
1	TST_N	Analog	O	**For Debug**
19	SPI_MOSI	LVTTL	O	**MOSI for SPI Interface**
18	SPI_MISO	Schmitt	I	**MISO for SPI Interface**
17	SPI_CSN	LVTTL	O	**Chip Select Signal for SPI Interface**
16	SPI_CK	LVTTL	O	**Clock for SPI Interface**
53	IIS_SCLK	LVTTL	I/O	**SCLK of IIS**
52	IIS_WS	LVTTL	I/O	**WS of IIS**
54	IIS_MCLK	LVTTL	I/O	**MCLK of IIS**
68	IIS_D0	LVTTL	I/O	**D0 of IIS**
67	IIS_D1	LVTTL	I/O	**D1 of IIS**
66	IIS_D2	LVTTL	I/O	**D2 of IIS**
65	IIS_D3/SPDIF	LVTTL	I/O	**D3/SPDIF of IIS**
45	GPIO1	LVTTL	I/O	**GPIO**
46	GPIO2	LVTTL	I/O	**GPIO**
47	GPIO3	LVTTL	I/O	**GPIO**
48	GPIO4	LVTTL	I/O	**GPIO**
49	GPIO5	LVTTL	I/O	**GPIO**

Pin#	Pin Name	I/O Type	I/O Dir	Description
35	RSTN	**Schmitt**	**I**	External Reset Signal, Low is Reset.
39	DPRX_HPD	**LVTTL**	**O**	**HPD Signal Of RX**
36	PWR_EN	**LVTTL**	**O**	**External 1.2V Power Control When Enter Sleep Mode, high is Enable.**
51	I2C_ADDR	**Schmitt**	**I**	**I2C Device Physical Address Select Pin** 0 = I2C device address @ 0x56; 1 = I2C device address @ 0x5E.
34	SLEEP_33	**Schmitt**	**I**	**External Sleep Mode Control Signal**
38	CSDA	**Schmitt，OD**	**I/O**	Slave I2C SDA Signal For Program Register
37	CSCL	**Schmitt，OD**	**I**	**Slave I2C SCL Signal For Program Register**
124	REXT	**Analog**	**O**	**External 7.68Kohm Resistor For BG**
29	NC	NA	NA	Reserve pin
30	NC	NA	NA	**Reserve pin**
40	NC	NA	NA	**Reserve pin**
50	NC	NA	NA	**Reserve pin**

7. Function Description

7.1 Function Block Diagram

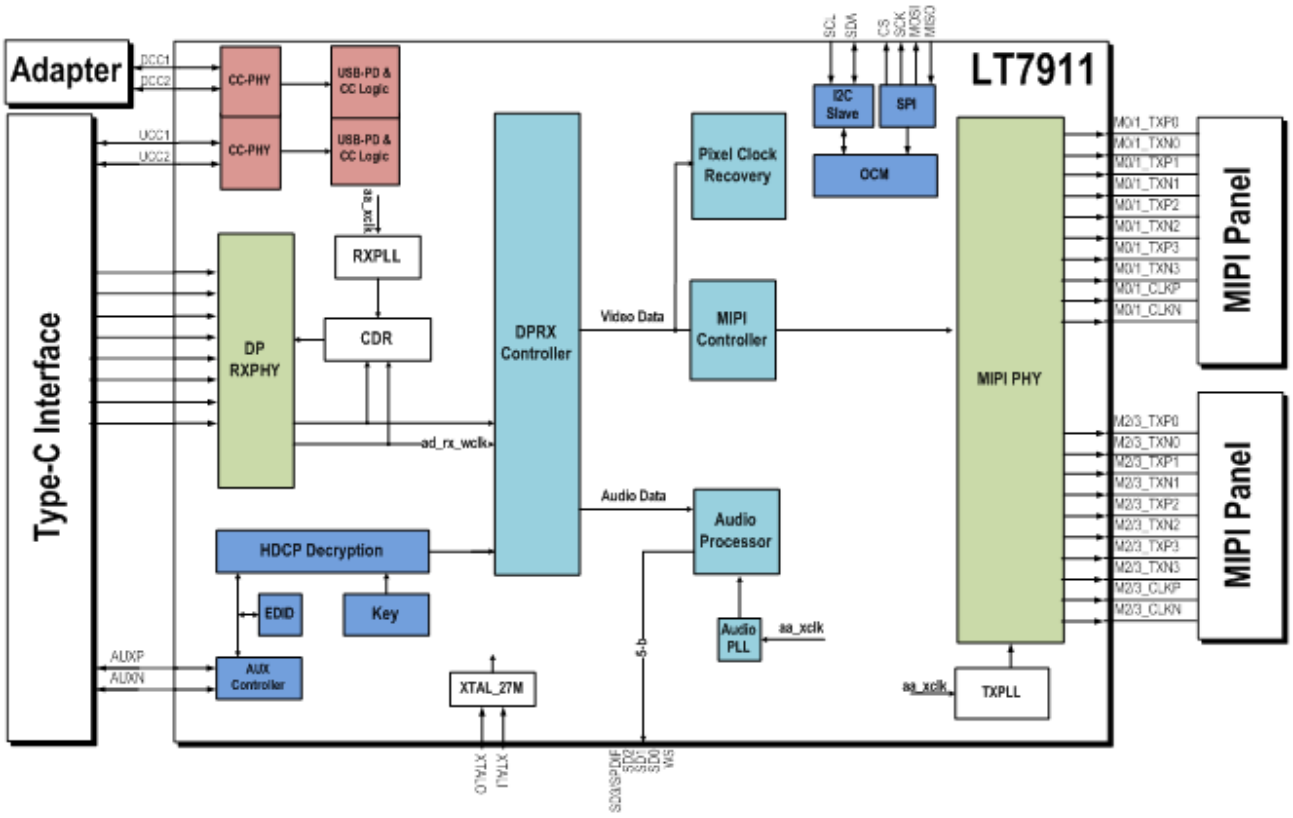


Figure 7.1.1 Function Block Diagram

8. Specification

8.1 Absolute Maximum Conditions

Table 8.1.1 Absolute Maximum Conditions

Symbol	Description	Min	Typ	Max	Unit
VCC33_IO, VCC33_TX0,VCC33_TX1,VCC33_TX2,VCC33_TX3,VCC33_BG, VCC33_TXPLL,VCC33_XTAL, VCC33_RX	3.3V Power Supply Voltage	-0.3		3.63	V
VDD,VCC12_TX0,VCC12_TX1, VCC12_TX2,VCC12_TX3, VCC12A_RX,VCC12D_RX,VCC12_PI,VCC12_RXPLL,VCC12_AUPLL	1.2V Power Supply Voltage	-0.3		1.2	V
V_I	CMOS Terminal Input Voltage Range	-0.3		3.63	V
V_O	CMOS Terminal Output Voltage Range	-0.3		3.63	V
T_S	Storage Temperature	-40		125	℃
ESD	HBM Elastrostatic Discharge Level		4000		V

Notes:
1.Permanent device damage may occur if absolute maximum conditions are exceeded.
2.Function operation should be restricted to the conditions described under Normal Operating Conditions.

8.2 Normal Operating Conditions

Table 8.2.1 Normal Operating Conditions

Symbol	Description	Min	Typ	Max	Unit
VCC33_IO, VCC33_TX0,VCC33_TX1,VCC33_TX2,VCC33_TX3,VCC33_BG, VCC33_TXPLL,VCC33_XTAL, VCC33_RX	3.3V Power Supply Voltage	2.97	3.3	3.63	V
VDD,VCC12_TX0,VCC12_TX1, VCC12_TX2,VCC12_TX3, VCC12A_RX,VCC12D_RX,VCC12_PI,VCC12_RXPLL,VCC12_AUPLL	1.2V Power Supply Voltage	1.08		1.32	V
VCC_N	Power Supply Voltage Noise			50	mV
T_A	Operating Free-air Temperature	-40	27	85	℃

8.3 DC Characteristics

Table 8.3.1 DC Characteristics

DP RX DC Specifications					
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**
Vidiff	Differential input peak-peak voltage level	90			mV
Rterm	Single-ended termination resistance	45	50	55	Ω
MIPI HS Line Transmitter DC Specifications					
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**
VIDTH	Differential input high voltage threshold			70	mV
VIDTL	Differential input low voltage threshold	-70			mV
VIHHS	Single ended input high voltage			460	mV
VILHS	Single ended input low voltage	-40			mV
VCMRXDC	Input common mode voltage	70		330	mV
	Differential input impedance	80		125	Ω
MIPI LP Line Transmitter DC Specifications					
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**
VIL-ULPS	Logic 0 input voltage, in ULP State			300	mV
VIL	Logic 0 input voltage, not in ULP State			550	mV
VIH	Input high voltage	880			mV
VHYST	Input hysteresis	25			mV

8.4 AC Characteristics

Table 8.4.1 AC Characteristics

DP RX AC Specifications					
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**
$T_{rx\_eye\_conn\_RBR}$	Minimum Receiver EYEWidth at RX-sideconnector pins for RBR	0.25			UI
$T_{rx\_eye\_conn\_HBR2}$	Minimum Receiver EYEWidth at RX-sideconnector pins for HBR2	0.38			UI
$T_{intra\_skew\_HRB2}$	Intra-pair skew at sink connector for HBR2	50			ps
$T_{intra\_skew\_HRB}$	Intra-pair skew at sink connector for HBR	60			ps
$T_{intra\_skew\_RBR}$	Intra-pair skew at sink connector for RBR	260			ps
MIPI HS Line Transmitter AC Specifications					
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**
ΔVCMRX(HF)	Common mode interference beyond 450MHz			200	mVpp
ΔVCMRX(LF)	Common mode interference between 50MHz and 450MHz.	-50		50	mVpp
Ccm	Common mode termination			60	pF
Rterm	Termination Resister	80	100	125	Ω

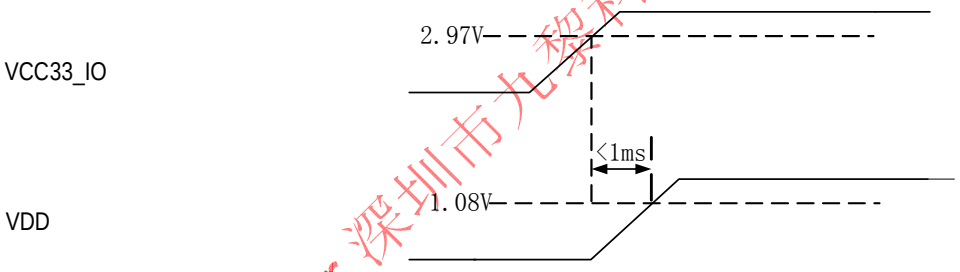
MIPI LP Line Transmitter AC Specifications					
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**
eSPIKE	Input pulse rejection			300	V.ps
TMIN	Minimum pulse response	20			ns
VINT	Peak interference voltage			200	mV
fINT	Interference frequency	450			MHz

8.5 Power Consumption

Table 8.5.1 Power Consumption

Condition	Supply Voltage	Supply Current	Unit
DP5.4G_4lane, TX 4port	5V	TBD	mA
DP2.7G_4lane, TX 2port	5V	TBD	mA

8.6 Power-up and Reset Sequence

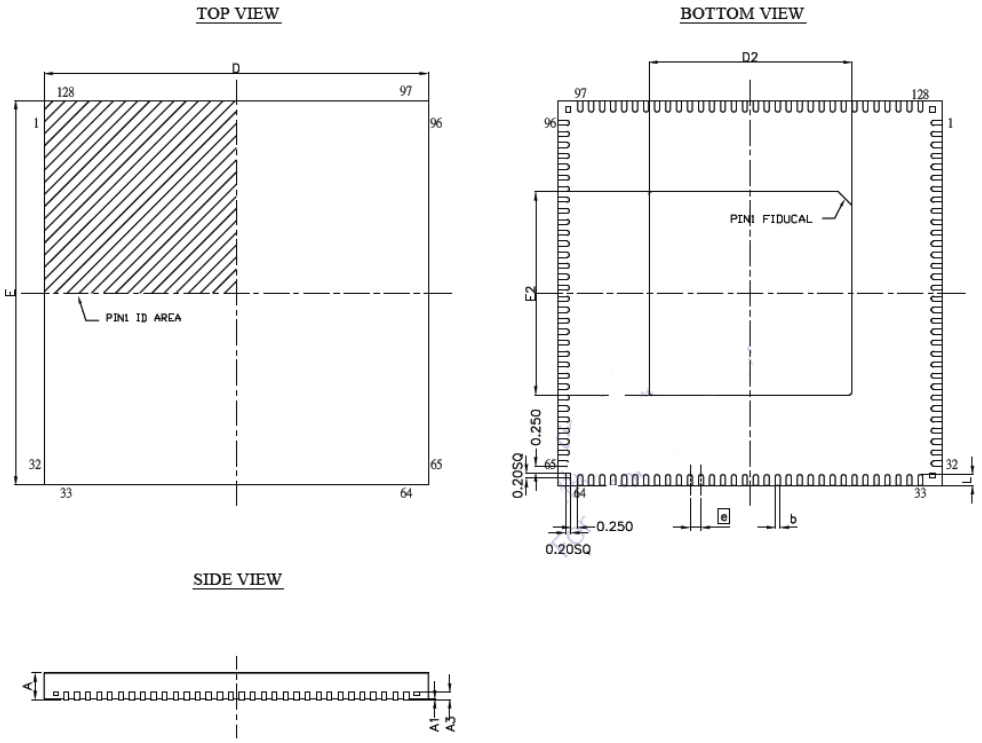


Note: 1.2V power should be ready before3.3V power or maximum 1ms later than 3.3V, the reset signal should be released after1.2V power is ready.

Figure 8.6.1 Power-up and Reset Sequence

9. Package Information

The LT7911 is available in QFN128 14mm x 14mm package.



SYMBOL	DIMENSION (MM)		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0	0.02	0.05
A3		0.20 REF	
b	0.13	0.18	0.25
D	13.90	14.00	14.10
D2	7.30	7.40	7.50
E	13.90	14.00	14.10
E2	7.30	7.40	7.50
e		0.40 BSC	
L	0.30	0.40	0.50

Figure 9.1 Package Dimensions

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