KH25V80066

2.3V-3.6V, 8M-BIT [x 1/x 2]
CMOS MXSMIO® (SERIAL MULTI I/O)
FLASH MEMORY

Key Features

- 2.3V-3.6V *for Read, Erase and Program Operations*
- *Multi I/O Support - Single I/O and Dual I/O*

Contents

2.3V-3.6V 8M-BIT [x 1/x 2] CMOS MXSMIO® (SERIAL MULTI I/O) FLASH MEMORY

1. FEATURES

GENERAL

- Supports Serial Peripheral Interface -- Mode 0 and Mode 3
- 8,388,608 x 1 bit structure or 4,194,304 x 2 bits (Dual Output mode) structure
- Equal Sectors with 4K byte each, Equal Blocks with 32K byte each, or Equal Blocks with 64K byte each
  - Any Block can be erased individually
- Single Power Supply Operation
  - Operation Voltage: 2.3V-3.6V for Read, Erase and Program Operations
- Latch-up protected to 100mA from -1V to Vcc +1V

PERFORMANCE

- High Performance
  - Fast read
    - 1 I/O: 80MHz with 8 dummy cycles
    - 1I/2O: 80MHz with 8 dummy cycles, equivalent to 160MHz
  - Fast program and erase time
- Low Power Consumption
- Typical 100,000 erase/program cycles
- 20 years data retention

SOFTWARE FEATURES

- Input Data Format
  - 1-byte Command code
- Advanced Security Features
  - Block lock protection

  The BP0-BP3 status bit defines the size of the area to be software protection against program and erase instructions
- Auto Erase and Auto Program Algorithm
  - Automatically erases and verifies data at selected sector or block
  - Automatically programs and verifies data at selected page by an internal algorithm that automatically times the program pulse widths (Any page to be programed should have page in the erased state first)
- Status Register Feature
- Electronic Identification
  - JEDEC 1-byte manufacturer ID and 2-byte device ID
  - RES command for 1-byte Device ID
  - REMS command for 1-byte manufacturer ID and 1-byte device ID
- Support Serial Flash Discoverable Parameters (SFDP) mode
- Support Unique ID (Please contact local Macronix sales for detail information)

HARDWARE FEATURES

- SCLK Input
  - Serial clock input
- SI/SIO0
  - Serial Data Input or Serial Data Input/Output for 2 x I/O read mode
- SO/SIO1
  - Serial Data Output or Serial Data Input/Output for 2 x I/O read mode
- WP#
  - Hardware write protection
- PACKAGE
  - 8-pin SOP (150mil)
  - 8-pin SOP (200mil)
  - **All devices are RoHS Compliant and Halogen-free**

2. GENERAL DESCRIPTION

KH25V80066 is 8Mb bits Serial NOR Flash memory, which is configured as 1,048,576 x 8 internally.

KH25V80066 features a serial peripheral interface and software protocol allowing operation on a simple 3-wire bus while it is in single I/O mode. The three bus signals are a clock input (SCLK), a serial data input (SI), and a serial data output (SO). Serial access to the device is enabled by CS# input.

When it is in two I/O read mode, the SI pin and SO pin become SIO0 pin and SIO1 pin for address/dummy bits input and data output.

The KH25V80066 MXSMIO® (Serial Multi I/O) provides sequential read operation on the whole chip.

After program/erase command is issued, auto program/erase algorithms which program/erase and verify the specified page or sector/block locations will be executed. Program command is executed on byte basis, or page (256 bytes) basis, or word basis. Erase command is executed on 4K-byte sector, or 32KB block (32K-byte), or 64K-byte block, or whole chip basis.

To provide user with ease of interface, a status register is included to indicate the status of the chip. The status read command can be issued to detect completion status of a program or erase operation via WIP bit.

Advanced security features enhance the protection and security functions, please see security features section for more details.

The KH25V80066 utilizes Macronix's proprietary memory cell, which reliably stores memory contents even after typical 100,000 program and erase cycles.

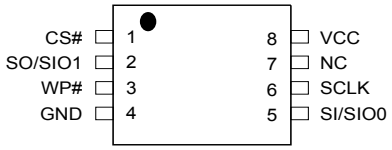
Table 1. Additional Feature

Protection and Security	**KH25V80066**
Flexible Block Protection (BP0-BP3)	V

Fast Read Performance		
I/O	1 I/O	1I/2O
Dummy Cycle	8	8
Frequency	80MHz	80MHz

3. PIN CONFIGURATIONS

8-PIN SOP (150mil) /8-PIN SOP (200mil)

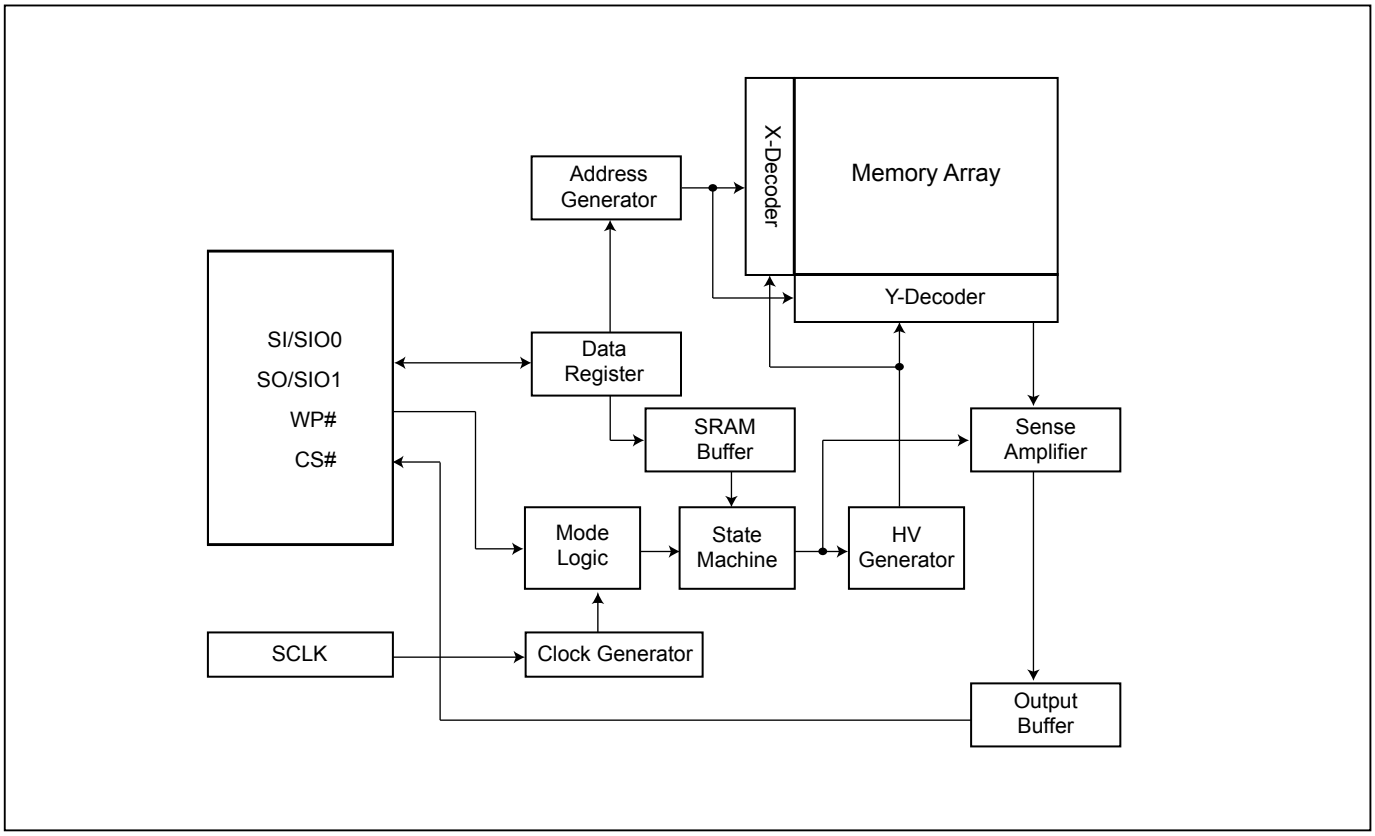


4. PIN DESCRIPTION

SYMBOL	DESCRIPTION
CS#	Chip Select
SI/SIO0	Serial Data Input (for 1 x I/O)/ Serial Data Input & Output (for 2xI/O read mode)
SO/SIO1	Serial Data Output (for 1 x I/O)/ Serial Data Input & Output (for 2xI/O read mode)
SCLK	Clock Input
WP#	Write Protection Active Low
VCC	Power Supply
GND	Ground
NC	No Connection

Note: The pin of WP# will remain internal pull up function while this pin is not physically connected in system configuration.
However, the internal pull up function will be disabled if the system has physical connection to WP# pin.

5. BLOCK DIAGRAM



6. DATA PROTECTION

During power transition, there may be some false system level signals which result in inadvertent erasure or programming. The device is designed to protect itself from these accidental write cycles.

The state machine will be reset as standby mode automatically during power up. In addition, the control register architecture of the device constrains that the memory contents can only be changed after specific command sequences have completed successfully.

In the following, there are several features to protect the system from the accidental write cycles during VCC power-up and power-down or from system noise.

- Power-on reset: to avoid sudden power switch by system power supply transition, the power-on reset may protect the Flash.
- Valid command length checking: The command length will be checked whether it is at byte base and completed on byte boundary.
- Write Enable (WREN) command: WREN command is required to set the Write Enable Latch bit (WEL) before issuing other commands to change data.
- Deep Power Down Mode: By entering deep power down mode, the flash device is under protected from writing all commands except toggling the CS#. For more detail please see *"9-18. Deep Power-down (DP)"*.
- Advanced Security Features: there are some protection and security features which protect content from inadvertent write and hostile access.

I. Block lock protection

- The Software Protected Mode (SPM) use (BP3, BP2, BP1, BP0) bits to allow part of memory to be protected as read only. The protected area definition is shown as *"Table 2. Protected Area Sizes"*, the protected areas are more flexible which may protect various area by setting value of BP0-BP3 bits.

- The Hardware Protected Mode (HPM) use WP#/SIO2 to protect the (BP3, BP2, BP1, BP0) bits and Status Register Write Protect (SRWD) bit. If the system goes into four I/O mode, the feature of HPM will be disabled.

Table 2. Protected Area Sizes

Protected Area Sizes

Status bit				Protect Level
BP3	**BP2**	**BP1**	**BP0**	**8Mb**
0	0	0	0	0 (none)
0	0	0	1	1 (1block, block 15th)
0	0	1	0	2 (2blocks, block 14th-15th)
0	0	1	1	3 (4blocks, block 12th-15th)
0	1	0	0	4 (8blocks, block 8th-15th)
0	1	0	1	5 (16blocks, protect all)
0	1	1	0	6 (16blocks, protect all)
0	1	1	1	7 (16blocks, protect all)
1	0	0	0	8 (16blocks, protect all)
1	0	0	1	9 (16blocks, protect all)
1	0	1	0	10 (16blocks, protect all)
1	0	1	1	11 (16blocks, protect all)
1	1	0	0	12 (16blocks, protect all)
1	1	0	1	13 (16blocks, protect all)
1	1	1	0	14 (16blocks, protect all)
1	1	1	1	15 (16blocks, protect all)

Note: The device is ready to accept a Chip Erase instruction if, and only if, all Block Protect (BP3, BP2, BP1, BP0) are 0.

7. MEMORY ORGANIZATION

Table 3. Memory Organization

Block (64KB)	Block (32KB)	Sector (4KB)	Address Range	
15	31	255	0FF000h	0FFFFFh
	|	:	:	:
	30	240	0F0000h	0F0FFFh
14	29	239	0EF000h	0EFFFFh
	|	:	:	:
	28	224	0E0000h	0E0FFFh
13	27	223	0DF000h	0DFFFFh
	|	:	:	:
	26	208	0D0000h	0D0FFFh
12	25	207	0CF000h	0CFFFFh
	|	:	:	:
	24	192	0C0000h	0C0FFFh
11	23	191	0BF000h	0BFFFFh
	|	:	:	:
	22	176	0B0000h	0B0FFFh
10	21	175	0AF000h	0AFFFFh
	|	:	:	:
	20	160	0A0000h	0A0FFFh
9	19	159	09F000h	09FFFFh
	|	:	:	:
	18	144	090000h	090FFFh
8	17	143	08F000h	08FFFFh
	|	:	:	:
	16	128	080000h	080FFFh
7	15	127	07F000h	07FFFFh
	|	:	:	:
	14	112	070000h	070FFFh
6	13	111	06F000h	06FFFFh
	|	:	:	:
	12	96	060000h	060FFFh
5	11	95	05F000h	05FFFFh
	|	:	:	:
	10	80	050000h	050FFFh
4	9	79	04F000h	04FFFFh
	|	:	:	:
	8	64	040000h	040FFFh
3	7	63	03F000h	03FFFFh
	|	:	:	:
	6	48	030000h	030FFFh
2	5	47	02F000h	02FFFFh
	|	:	:	:
	4	32	020000h	020FFFh
1	3	31	01F000h	01FFFFh
	|	:	:	:
	2	16	010000h	010FFFh
0	1	15	00F000h	00FFFFh
	|	:	:	:
	0	2	002000h	002FFFh
		1	001000h	001FFFh
		0	000000h	000FFFh

8. DEVICE OPERATION

1. Before a command is issued, status register should be checked to ensure device is ready for the intended operation.

2. When incorrect command is inputted to this device, it enters standby mode and remains in standby mode until next CS# falling edge. In standby mode, SO pin of the device is High-Z.

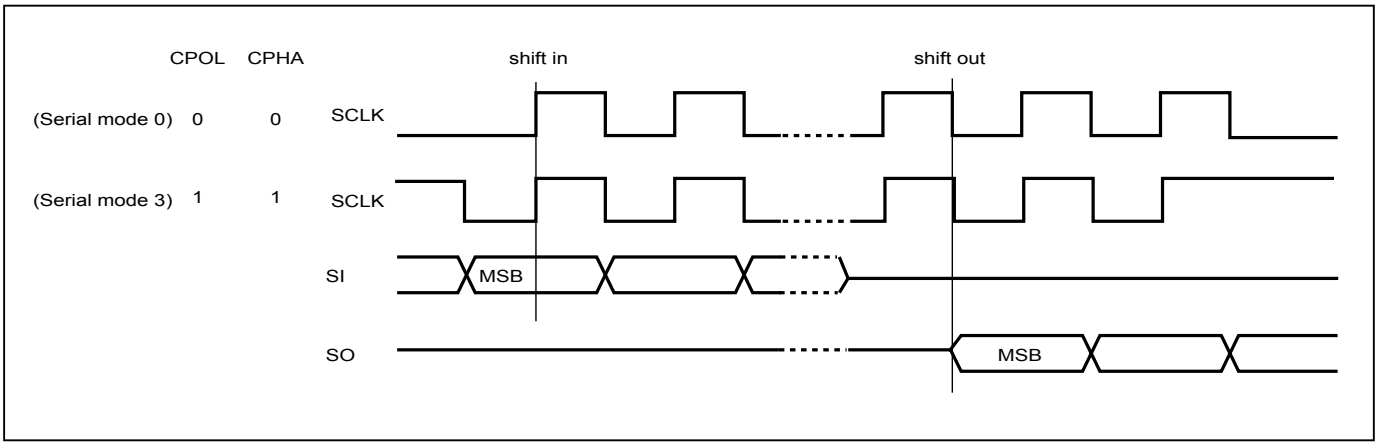
3. When correct command is inputted to this device, it enters active mode and remains in active mode until next CS# rising edge.

4. Input data is latched on the rising edge of Serial Clock (SCLK) and data shifts out on the falling edge of SCLK. The difference of Serial mode 0 and mode 3 is shown as *"Figure 1. Serial Modes Supported"*.

5. For the following instructions: RDID, RDSR, READ, FAST_READ, DREAD, RDSFDP, RES, REMS, the shifted-in instruction sequence is followed by a data-out sequence. After any bit of data being shifted out, the CS# can be high. For the following instructions: WREN, WRDI, WRSR, SE, BE32K, BE, CE, PP, DP the CS# must go high exactly at the byte boundary; otherwise, the instruction will be rejected and not executed.

6. While a Write Status Register, Program or Erase operation is in progress, access to the memory array is neglected and will not affect the current operation of Write Status Register, Program, Erase.

Figure 1. Serial Modes Supported



Note:
CPOL indicates clock polarity of Serial master, CPOL=1 for SCLK high while idle, CPOL=0 for SCLK low while not transmitting. CPHA indicates clock phase. The combination of CPOL bit and CPHA bit decides which Serial mode is supported.

Figure 2. Serial Input Timing

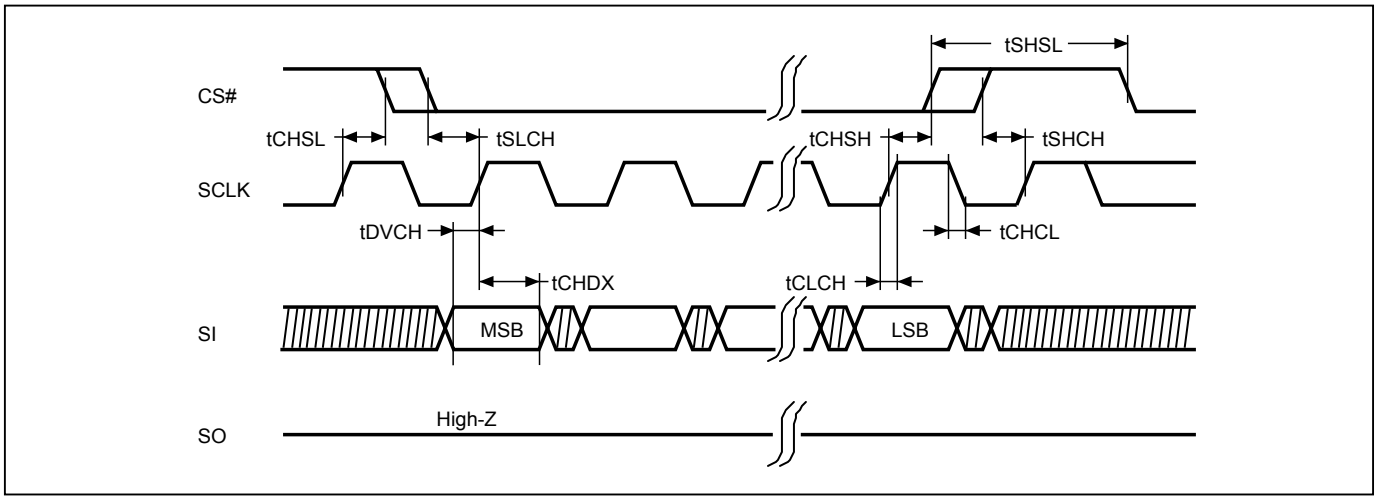
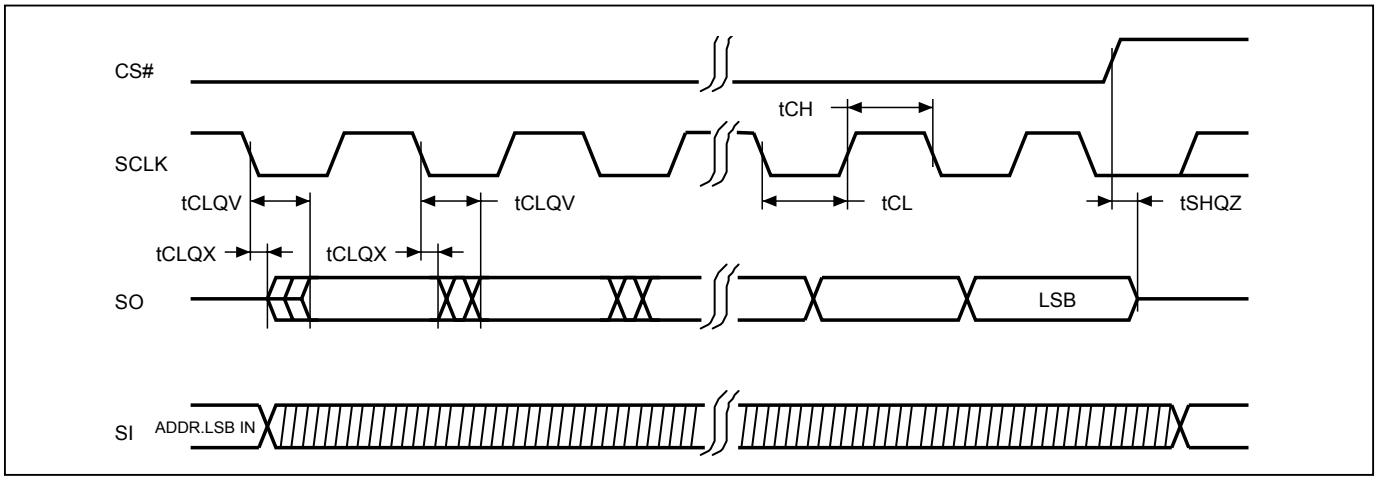


Figure 3. Output Timing



9. COMMAND DESCRIPTION

Table 4. Command Set

Command	Command Code	Address Byte				Dummy Cycle	Data Byte
		Total ADD Byte	Byte 1	Byte 2	Byte 3		
Array access							
READ (normal read)	03 (hex)	3	ADD1	ADD2	ADD3	0	1- ∞
FAST READ (fast read data)	0B (hex)	3	ADD1	ADD2	ADD3	8 *	1- ∞
DREAD (1I 2O read)	3B (hex)	3	ADD1	ADD2	ADD3	8 *	1- ∞
PP (page program)	02 (hex)	3	ADD1	ADD2	ADD3	0	1-256
SE (sector erase)	20 (hex)	3	ADD1	ADD2	ADD3	0	0
BE 32K (block erase 32KB)	52 (hex)	3	ADD1	ADD2	ADD3	0	0
BE (block erase 64KB)	D8 (hex)	3	ADD1	ADD2	ADD3	0	0
CE (chip erase)	60 or C7 (hex)	0				0	0
RDSFDP (Read SFDP)	5A (hex)	3	ADD1	ADD2	ADD3	8	1- ∞
Device operation							
WREN (write enable)	06 (hex)	0				0	0
WRDI (write disable)	04 (hex)	0				0	0
DP (Deep power down)	B9 (hex)	0				0	0
FMEN (factory mode enable)	41 (hex)	0				0	0
RSTEN (Reset Enable)	66 (hex)	0				0	0
RST (Reset Memory)	99 (hex)	0				0	0
Register Access							
RDID (read identification)	9F (hex)	0				0	3
RES (read electronic ID)	AB (hex)	0	Dummy	Dummy	Dummy	0	1
RES (release from deep power down)	AB (hex)	0				0	0
REMS (read electronic manufacturer & device ID)	90 (hex)	1	Dummy	Dummy	ADD Note1	0	2
RDSR (read status register)	05 (hex)	0				0	1
WRSR (write status register)	01 (hex)	0				0	1

Note 1: ADD=00H will output the manufacturer ID first and ADD=01H will output device ID first.

Note 2: It is not recommended to adopt any other code not in the command definition table, which will potentially enter the hidden mode.

Note 3: The RSTEN command must be executed before executing the RST command. If any other command is issued in-between RSTEN and RST, the RST command will be ignored.

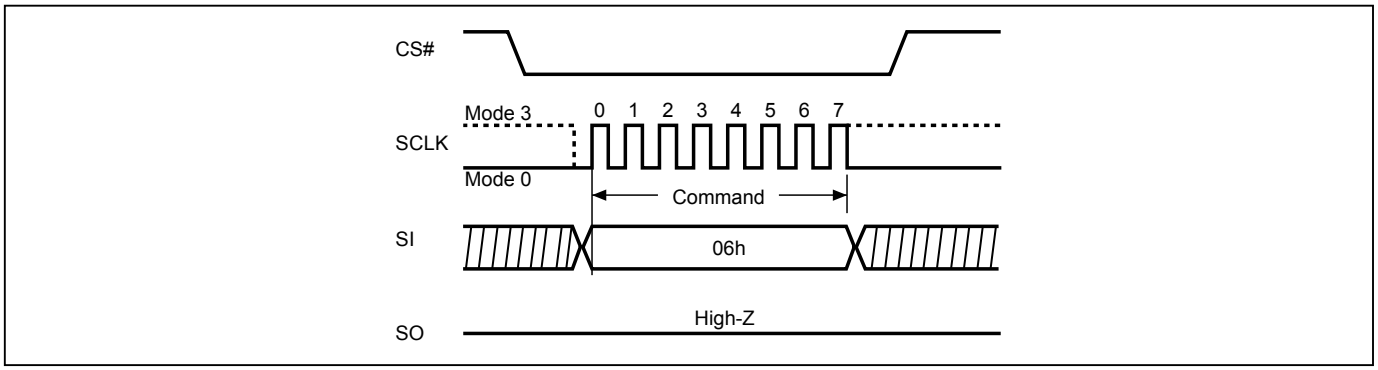
9-1. Write Enable (WREN)

The Write Enable (WREN) instruction is for setting Write Enable Latch (WEL) bit. For those instructions like PP, SE, BE32K, BE, CE, and WRSR, which are intended to change the device content WEL bit should be set every time after the WREN instruction setting the WEL bit.

The sequence of issuing WREN instruction is: CS# goes low→sending WREN instruction code→ CS# goes high.

The SIO[3:1] are "don't care" .

Figure 4. Write Enable (WREN) Sequence



9-2. Write Disable (WRDI)

The Write Disable (WRDI) instruction is to reset Write Enable Latch (WEL) bit.

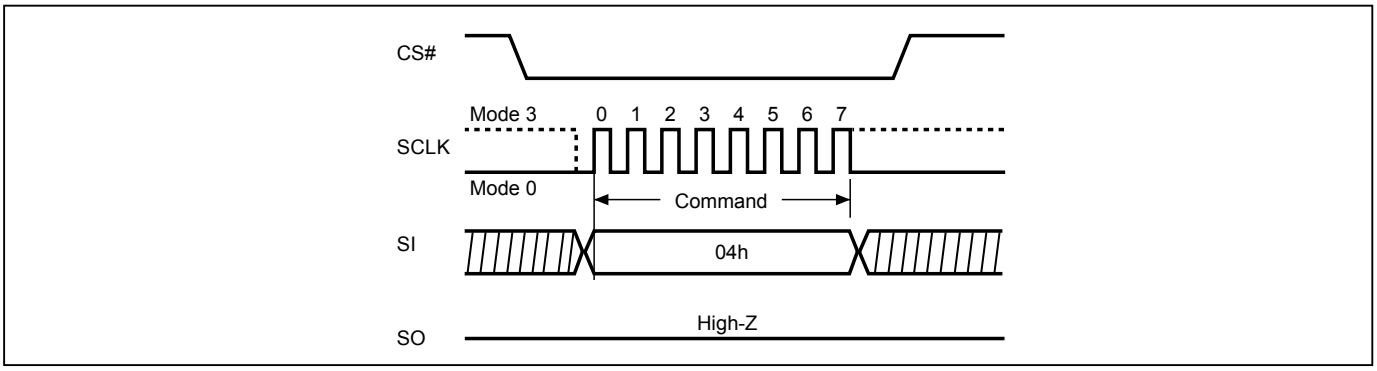
The sequence of issuing WRDI instruction is: CS# goes low→sending WRDI instruction code→CS# goes high.

The SIO[3:1] are "don't care".

The WEL bit is reset by following situations:

- Power-up
- Completion of Write Disable (WRDI) instruction
- Completion of Write Status Register (WRSR) instruction
- Completion of Page Program (PP) instruction
- Completion of Sector Erase (SE) instruction
- Completion of Block Erase 32KB (BE32K) instruction
- Completion of Block Erase (BE) instruction
- Completion of Chip Erase (CE) instruction

Figure 5. Write Disable (WRDI) Sequence



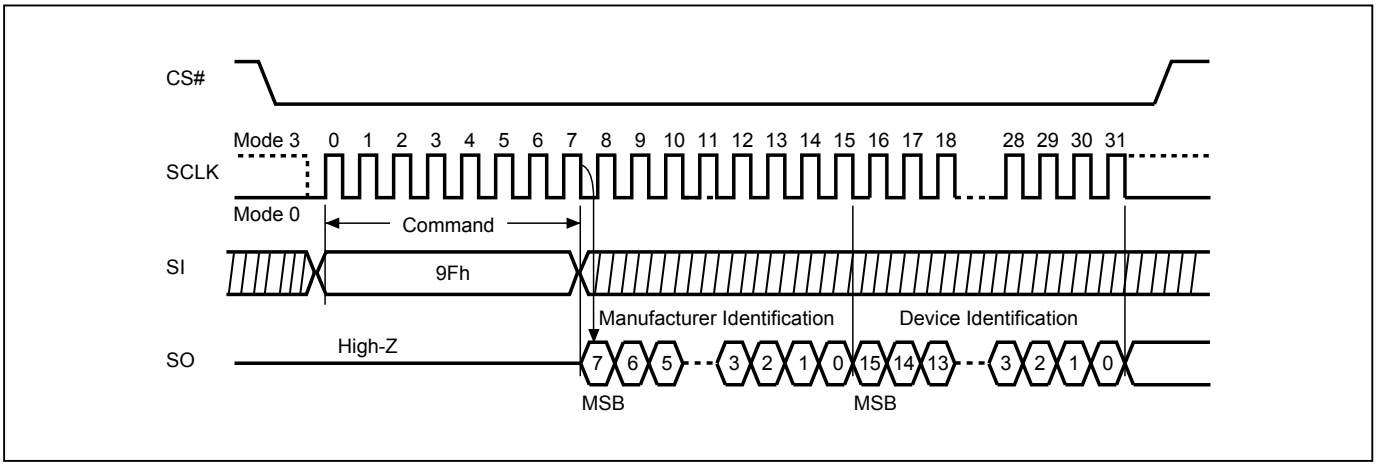
9-3. Read Identification (RDID)

The RDID instruction is for reading the manufacturer ID of 1-byte and followed by Device ID of 2-byte. The Macronix Manufacturer ID and Device ID are listed as *"Table 5. ID Definitions"*.

The sequence of issuing RDID instruction is: CS# goes low→ sending RDID instruction code→24-bits ID data out on SO→ to end RDID operation can drive CS# to high at any time during data out.

While Program/Erase operation is in progress, it will not decode the RDID instruction, therefore there's no effect on the cycle of program/erase operation which is currently in progress. When CS# goes high, the device is at standby stage.

Figure 6. Read Identification (RDID) Sequence



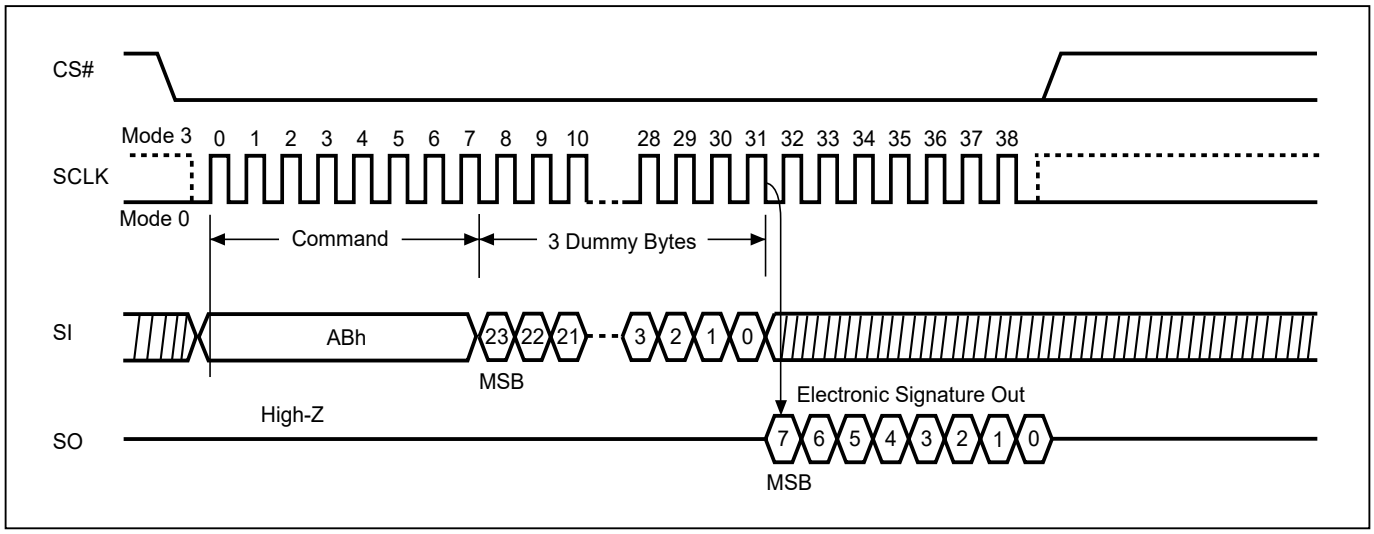
9-4. Read Electronic Signature (RES)

RES instruction is for reading out the old style of 8-bit Electronic Signature, whose values are shown as *"Table 5. ID Definitions"*. This is not the same as RDID instruction. It is not recommended to use for new design. For new design, please use RDID instruction.

The SIO[3:1] are "don't care".

The RES instruction is ended by CS# goes high after the ID been read out at least once. The ID outputs repeatedly if continuously send the additional clock cycles on SCLK while CS# is at low.

Figure 7. Read Electronic Signature (RES) Sequence



9-5. Factory Mode Enable (FMEN)

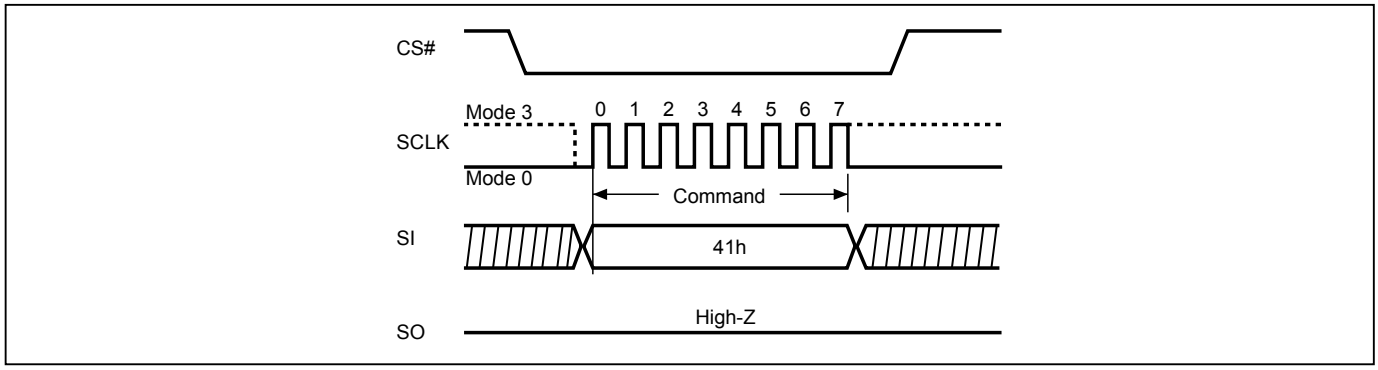
The Factory Mode Enable (FMEN) instruction is for enhance Program and Erase performance for increase factory production throughput. The FMEN instruction need to combine with the instructions which are intended to change the device content, like SE, BE32K, BE, and CE.

The sequence of issuing FMEN instruction is: CS# goes low→sending FMEN instruction code→ CS# goes high. A valid factory mode operation need to included three sequences: WREN instruction → FMEN instruction→ Erase instruction.

The FMEN is reset by following situations

- Power-up
- SE command completion
- BE32K command completion
- BE command completion
- CE command completion
- PGM command completion

Figure 8. Factory Mode Enable (FMEN) Sequence

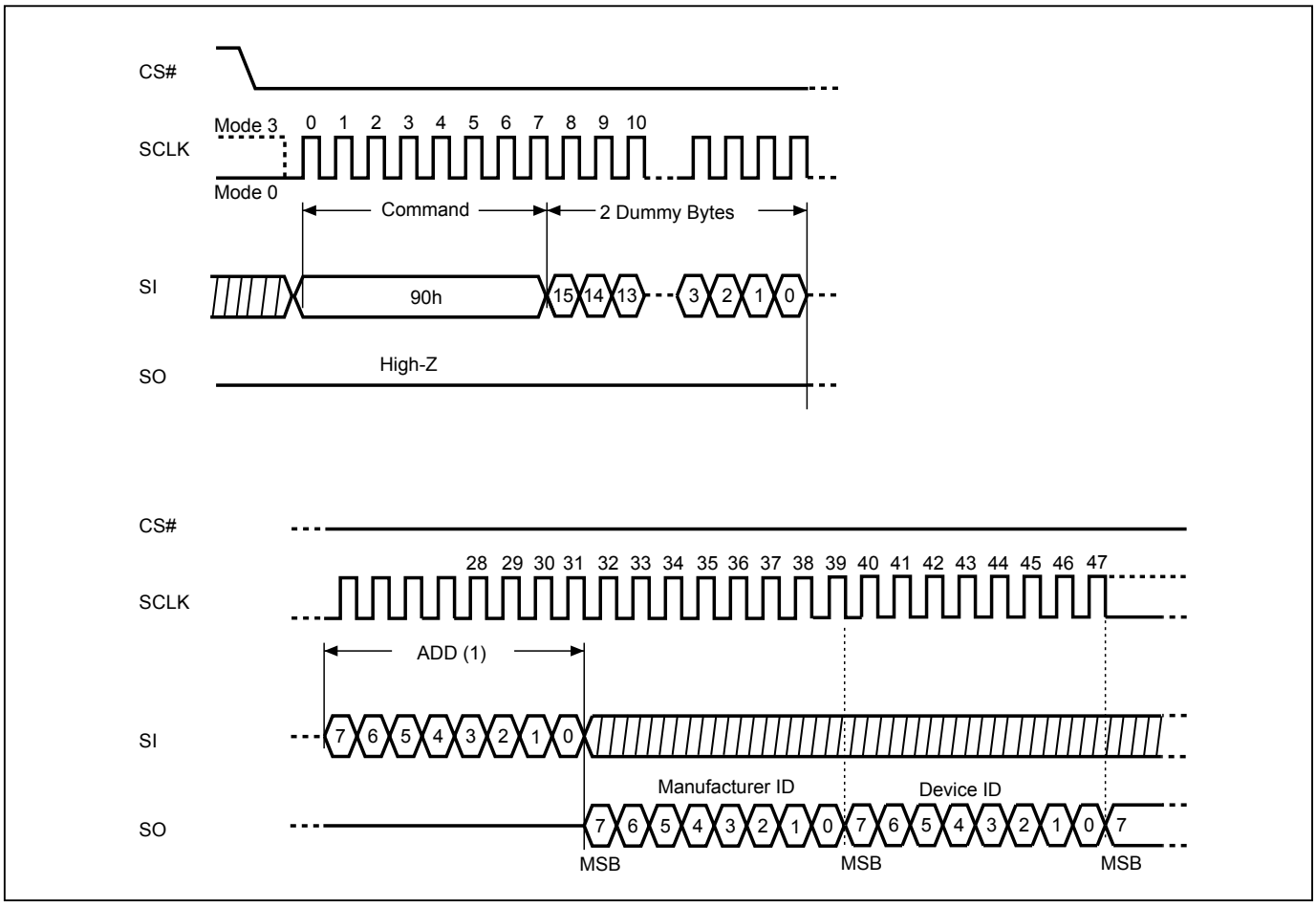


9-6. Read Electronic Manufacturer ID & Device ID (REMS)

The REMS instruction returns both the JEDEC assigned manufacturer ID and the device ID. The Device ID values are listed in *"Table 5. ID Definitions".*

The REMS instruction is initiated by driving the CS# pin low and sending the instruction code "90h" followed by two dummy bytes and one address byte (A7-A0). After which the manufacturer ID for Macronix (C2h) and the device ID are shifted out on the falling edge of SCLK with the most significant bit (MSB) first. If the address byte is 00h, the manufacturer ID will be output first, followed by the device ID. If the address byte is 01h, then the device ID will be output first, followed by the manufacturer ID. While CS# is low, the manufacturer and device IDs can be read continuously, alternating from one to the other. The instruction is completed by driving CS# high.

Figure 9. Read Electronic Manufacturer & Device ID (REMS) Sequence



Notes:
(1) ADD=00H will output the manufacturer's ID first and ADD=01H will output device ID first.

9-7. ID Read

User can execute this ID Read instruction to identify the Device ID and Manufacturer ID. The sequence of issuing RDID instruction is: CS# goes low→ sending RDID instruction code→24-bits ID data out on SO→ to end RDID operation can drive CS# to high at any time during data out.

After the command cycle, the device will immediately output data on the falling edge of SCLK. The manufacturer ID, memory type, and device ID data byte will be output continuously, until the CS# goes high.

While Program/Erase operation is in progress, it will not decode the RDID instruction, therefore there's no effect on the cycle of program/erase operation which is currently in progress. When CS# goes high, the device is at standby stage.

Table 5. ID Definitions

Command Type	**KH25V80066**		
RDID	Manufacturer ID	Memory type	Memory density
	C2	20	14
RES	Electronic ID		
	13		
REMS	Manufacturer ID	Device ID	
	C2	13	

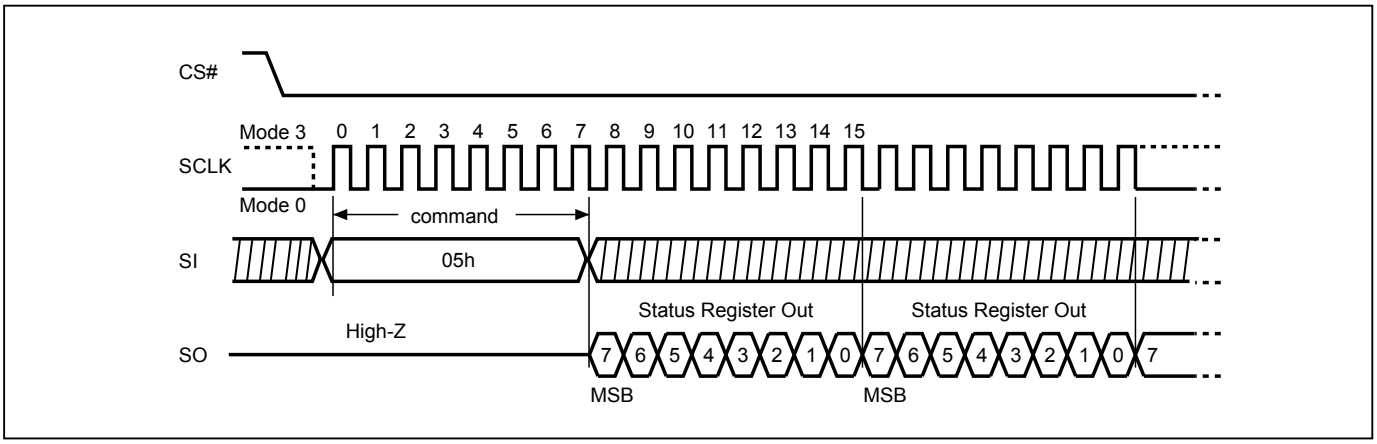
9-8. Read Status Register (RDSR)

The RDSR instruction is for reading Status Register Bits. The Read Status Register can be read at any time (even in program/erase/write status register condition). It is recommended to check the Write in Progress (WIP) bit before sending a new instruction when a program, erase, or write status register operation is in progress.

The sequence of issuing RDSR instruction is: CS# goes low→ sending RDSR instruction code→ Status Register data out on SO.

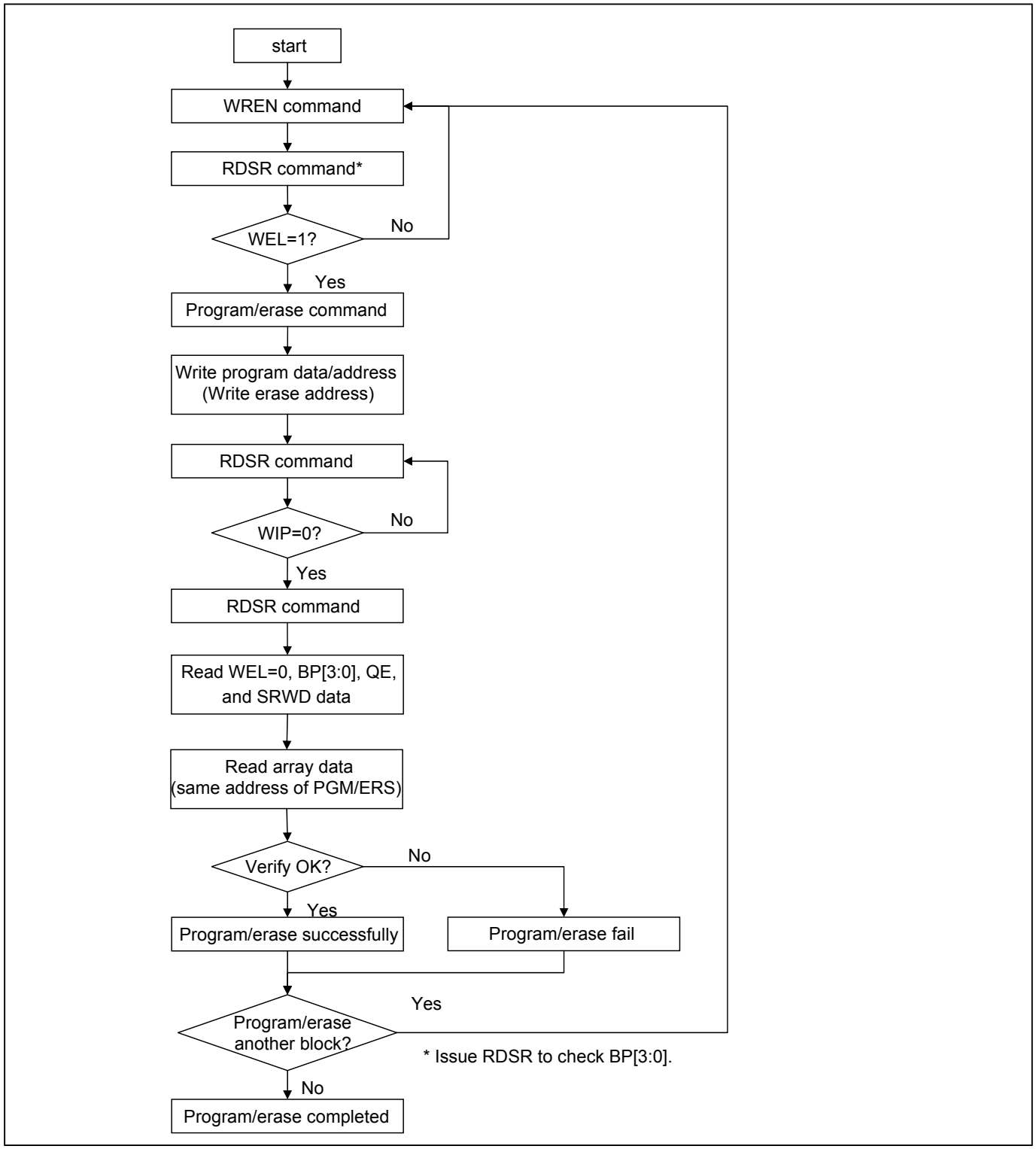
The SIO[3:1] are "don't care".

Figure 10. Read Status Register (RDSR) Sequence



For user to check if Program/Erase operation is finished or not, RDSR instruction flow are shown as follows:

Figure 11. Program/Erase flow with read array data



Status Register

The definition of the status register bits is as below:

WIP bit. The Write in Progress (WIP) bit, a volatile bit, indicates whether the device is busy in program/erase/write status register progress. When WIP bit sets to 1, which means the device is busy in program/erase/write status register progress. When WIP bit sets to 0, which means the device is not in progress of program/erase/write status register cycle.

WEL bit. The Write Enable Latch (WEL) bit, a volatile bit, indicates whether the device is set to internal write enable latch. When WEL bit sets to 1, which means the internal write enable latch is set, the device can accept program/erase/write status register instruction. When WEL bit sets to 0, which means no internal write enable latch; the device will not accept program/erase/write status register instruction. The program/erase command will be ignored if it is applied to a protected memory area. To ensure both WIP bit & WEL bit are both set to 0 and available for next program/erase/operations, WIP bit needs to be confirm to be 0 before polling WEL bit. After WIP bit confirmed, WEL bit needs to be confirmed as 0.

BP3, BP2, BP1, BP0 bits. The Block Protect (BP3, BP2, BP1, BP0) bits, non-volatile bits, indicate the protected area (as defined in *"Table 2. Protected Area Sizes"*) of the device to against the program/erase instruction without hardware protection mode being set. To write the Block Protect (BP3, BP2, BP1, BP0) bits requires the Write Status Register (WRSR) instruction to be executed. Those bits define the protected area of the memory to against Page Program (PP), Sector Erase (SE), Block Erase (BE/BE32K) and Chip Erase (CE) instructions (only if Block Protect bits (BP3:BP0) set to 0, the CE instruction can be executed). The BP3, BP2, BP1, BP0 bits are "0" as default, which is un-protected.

SRWD bit. The Status Register Write Disable (SRWD) bit, non-volatile bit, is operated together with Write Protection (WP#/SIO2) pin for providing hardware protection mode. The hardware protection mode requires SRWD sets to 1 and WP#/SIO2 pin signal is low stage. In the hardware protection mode, the Write Status Register (WRSR) instruction is no longer accepted for execution and the SRWD bit and Block Protect bits (BP3, BP2, BP1, BP0) are read only. The SRWD bit defaults to be "0".

Table 6. Status Register

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
SRWD (status register write protect)	Reserved	BP3 (level of protected block)	BP2 (level of protected block)	BP1 (level of protected block)	BP0 (level of protected block)	WEL (write enable latch)	WIP (write in progress bit)
1=status register write disabled 0=status register write enabled	Reserved	*(note 1)*	*(note 1)*	*(note 1)*	*(note 1)*	1=write enable 0=not write enable	1=write operation 0=not in write operation
Non-volatile bit	Non-volatile bit	Non-volatile bit	Non-volatile bit	Non-volatile bit	Non-volatile bit	volatile bit	volatile bit

Note 1: Please refer to the *"Table 2. Protected Area Sizes"*.

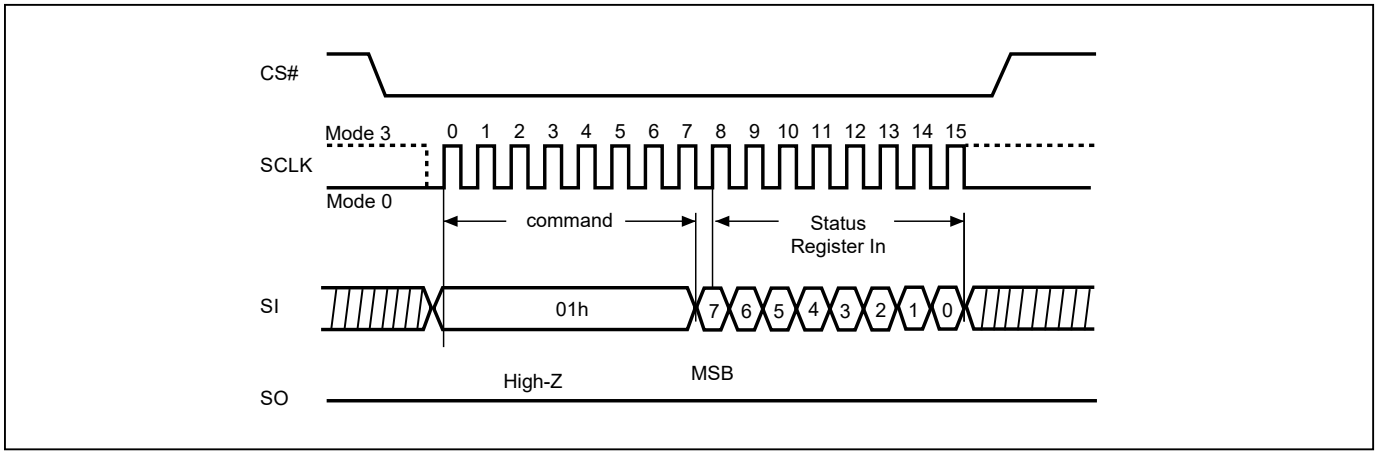
9-9. Write Status Register (WRSR)

The WRSR instruction is for changing the values of Status Register Bits. Before sending WRSR instruction, the Write Enable (WREN) instruction must be decoded and executed to set the Write Enable Latch (WEL) bit in advance. The WRSR instruction can change the value of Block Protect (BP3, BP2, BP1, BP0) bits to define the protected area of memory (as shown in *"Table 2. Protected Area Sizes"*). The WRSR also can set or reset the Status Register Write Disable (SRWD) bit in accordance with Write Protection (WP#) pin signal, but has no effect on bit1(WEL) and bit0 (WIP) of the status register. The WRSR instruction cannot be executed once the Hardware Protected Mode (HPM) is entered.

The sequence of issuing WRSR instruction is: CS# goes low→ sending WRSR instruction code→ Status Register data on SI→CS# goes high.

The CS# must go high exactly at the 8 bits data boundary; otherwise, the instruction will be rejected and not executed. The self-timed Write Status Register cycle time (tW) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked during the Write Status Register cycle is in progress. The WIP sets 1 during the tW timing, and sets 0 when Write Status Register Cycle is completed, and the Write Enable Latch (WEL) bit is reset. For more detail please check *"Table 11. AC Characteristics"*.

Figure 12. Write Status Register (WRSR) Sequence



Software Protected Mode (SPM):

- When SRWD bit=0, no matter WP# is low or high, the WREN instruction may set the WEL bit and can change the values of SRWD, BP3, BP2, BP1, BP0. The protected area, which is defined by BP3, BP2, BP1, BP0, is at software protected mode (SPM).
- When SRWD bit=1 and WP# is high, the WREN instruction may set the WEL bit can change the values of SRWD, BP3, BP2, BP1, BP0. The protected area, which is defined by BP3, BP2, BP1, BP0, is at software protected mode (SPM)

Note:

If SRWD bit=1 but WP#/SIO2 is low, it is impossible to write the Status Register even if the WEL bit has previously been set. It is rejected to write the Status Register and not be executed.

Hardware Protected Mode (HPM):

- When SRWD bit=1, and then WP# is low (or WP# is low before SRWD bit=1), it enters the hardware protected mode (HPM). The data of the protected area is protected by software protected mode by BP3, BP2, BP1, BP0 and hardware protected mode by the WP# to against data modification.

Note:

To exit the hardware protected mode requires WP# driving high once the hardware protected mode is entered. If the WP# pin is permanently connected to high, the hardware protected mode can never be entered; only can use software protected mode via BP3, BP2, BP1, BP0.

Table 7. Protection Modes

Mode	Status register condition	WP# and SRWD bit status	Memory
Software protection mode (SPM)	Status register can be written in (WEL bit is set to "1") and the SRWD, BP0-BP3 bits can be changed	WP#=1 and SRWD bit=0, or WP#=0 and SRWD bit=0, or WP#=1 and SRWD=1	The protected area cannot be program or erase.
Hardware protection mode (HPM)	The SRWD, BP0-BP3 of status register bits cannot be changed	WP#=0, SRWD bit=1	The protected area cannot be program or erase.

Note:

1. As defined by the values in the Block Protect (BP3, BP2, BP1, BP0) bits of the Status Register, as shown in *"Table 2. Protected Area Sizes"*.

Figure 13. WRSR flow

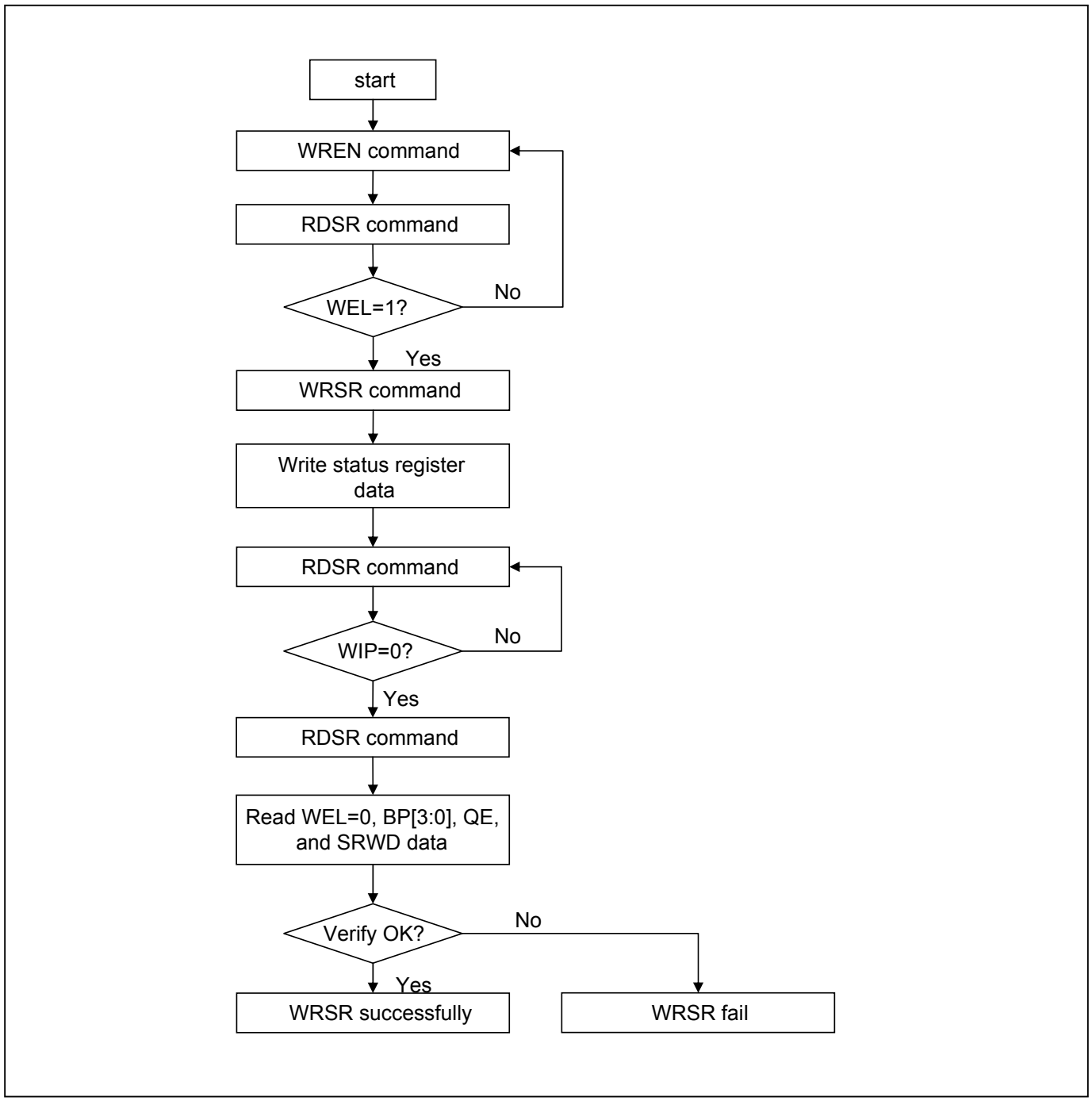
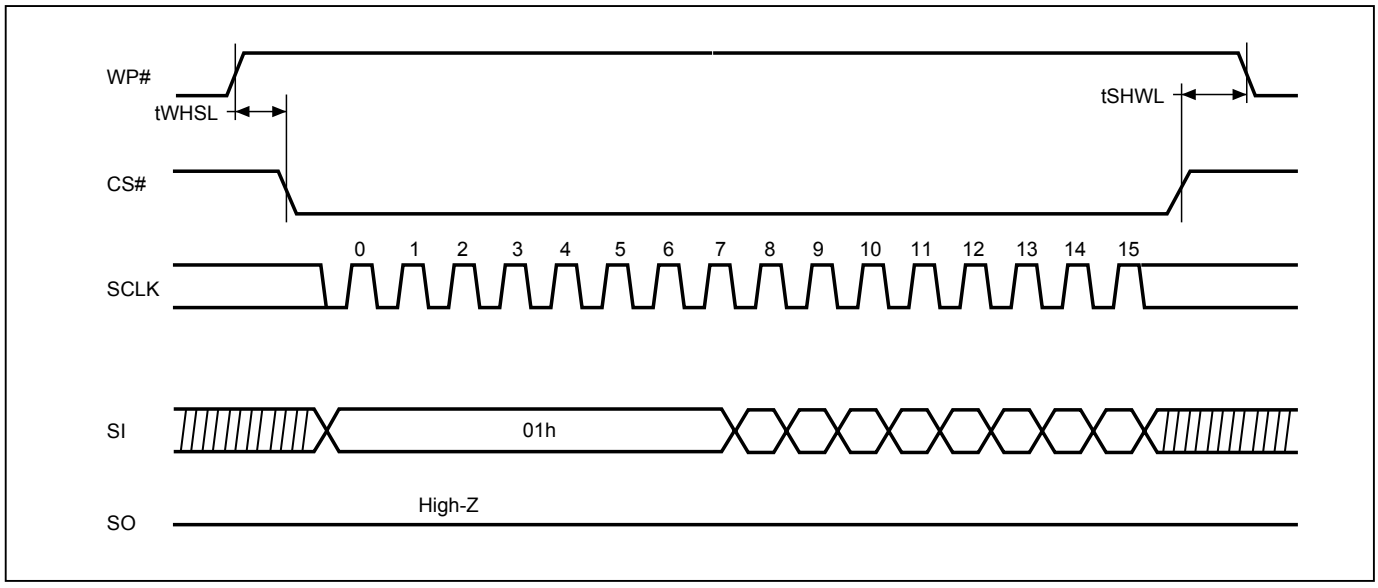


Figure 14. WP# Setup Timing and Hold Timing during WRSR when SRWD=1



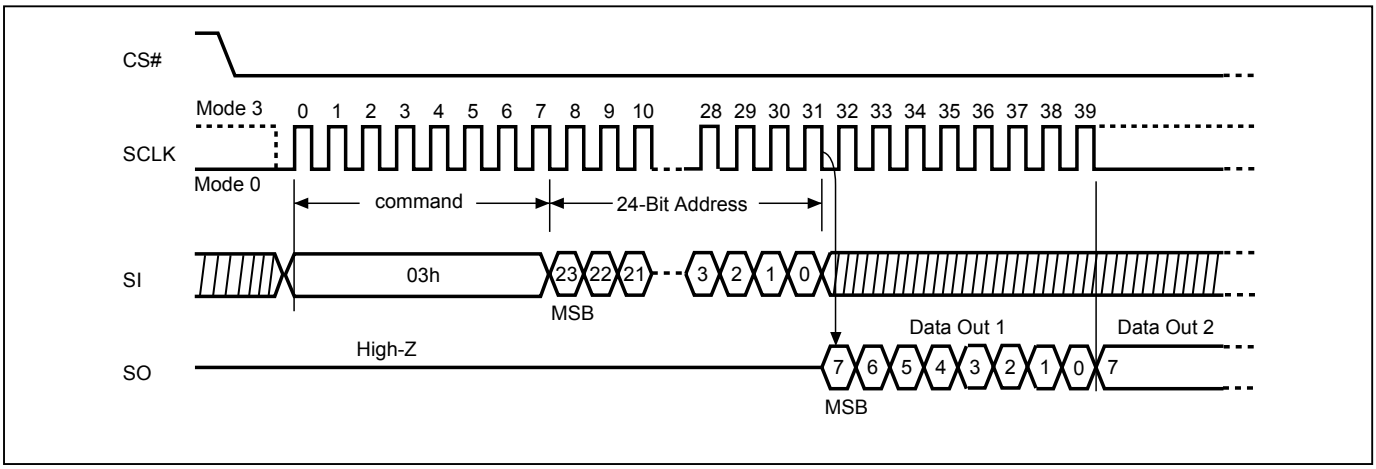
Note: WP# must be kept high until the embedded operation finish.

9-10. Read Data Bytes (READ)

The read instruction is for reading data out. The address is latched on rising edge of SCLK, and data shifts out on the falling edge of SCLK at a maximum frequency fR. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single READ instruction. The address counter rolls over to 0 when the highest address has been reached.

The sequence of issuing READ instruction is: CS# goes low→sending READ instruction code→ 3-byte address on SI→ data out on SO→to end READ operation can use CS# to high at any time during data out.

Figure 15. Read Data Bytes (READ) Sequence



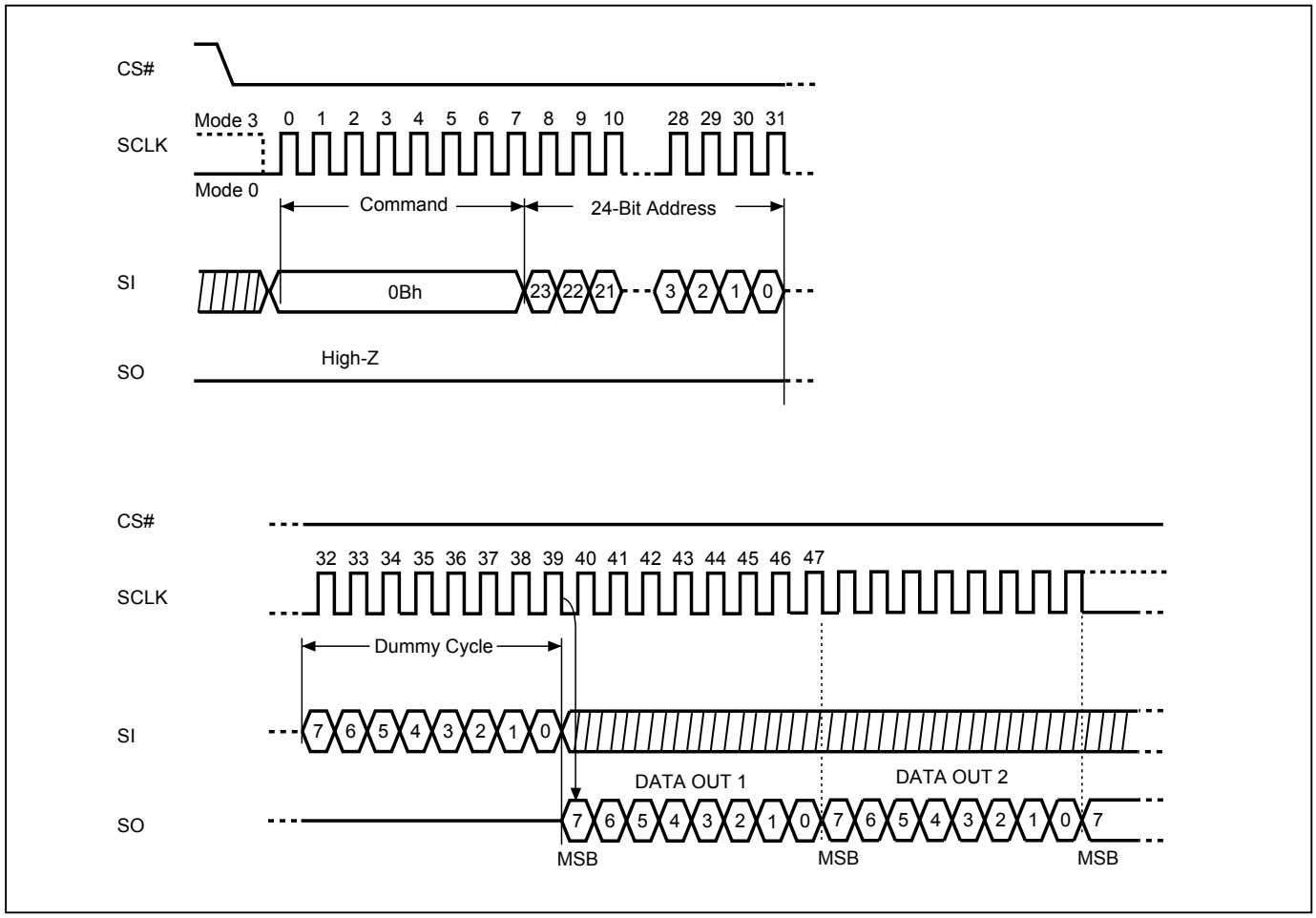
9-11. Read Data Bytes at Higher Speed (FAST_READ)

The FAST_READ instruction is for quickly reading data out. The address is latched on rising edge of SCLK, and data of each bit shifts out on the falling edge of SCLK at a maximum frequency fC. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single FAST_READ instruction. The address counter rolls over to 0 when the highest address has been reached.

The sequence of issuing FAST_READ instruction is: CS# goes low→ sending FAST_READ instruction code→ 3-byte address on SI→1-dummy byte (default) address on SI→ data out on SO→ to end FAST_READ operation can use CS# to high at any time during data out.

While Program/Erase/Write Status Register cycle is in progress, FAST_READ instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

Figure 16. Read at Higher Speed (FAST_READ) Sequence



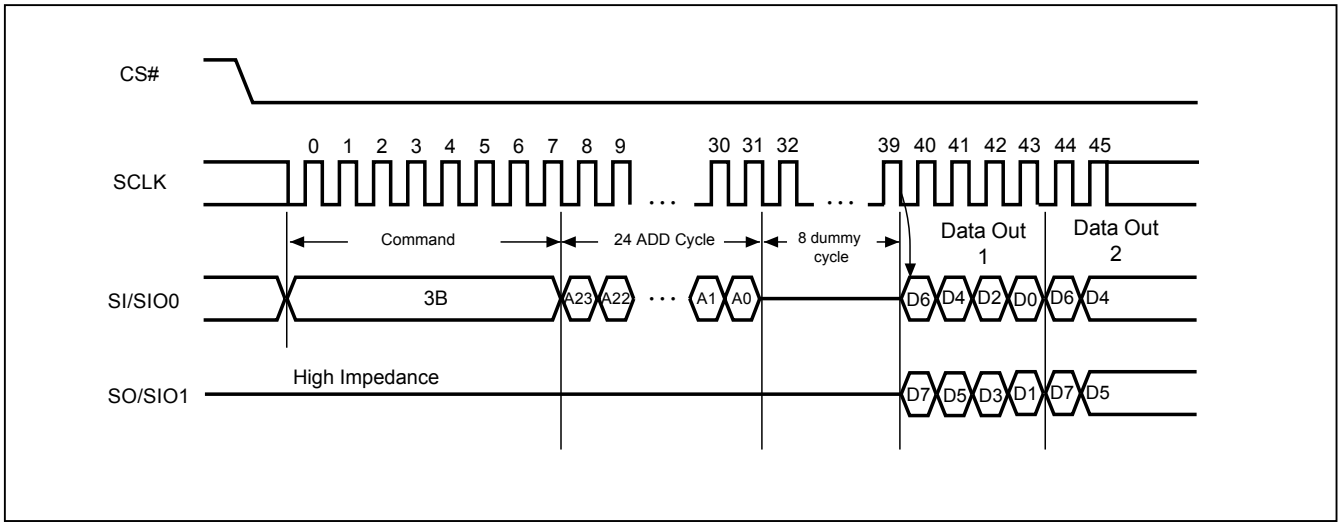
9-12. Dual Read Mode (DREAD)

The DREAD instruction enable double throughput of Serial NOR Flash in read mode. The address is latched on rising edge of SCLK, and data of every two bits (interleave on 2 I/O pins) shift out on the falling edge of SCLK at a maximum frequency fT. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single DREAD instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing DREAD instruction, the following data out will perform as 2-bit instead of previous 1-bit.

The sequence of issuing DREAD instruction is: CS# goes low → sending DREAD instruction → 3-byte address on SI → 8-bit dummy cycle → data out interleave on SIO1 & SIO0 → to end DREAD operation can use CS# to high at any time during data out.

While Program/Erase/Write Status Register cycle is in progress, DREAD instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

Figure 17. Dual Read Mode Sequence (Command 3Bh)



9-13. Sector Erase (SE)

The Sector Erase (SE) instruction is for erasing the data of the chosen sector to be "1". The instruction is used for any 4K-byte sector. A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Sector Erase (SE). Any address of the sector (see *"Table 3. Memory Organization"*) is a valid address for Sector Erase (SE) instruction. The CS# must go high exactly at the byte boundary (the latest eighth of address byte been latched-in); otherwise, the instruction will be rejected and not executed.

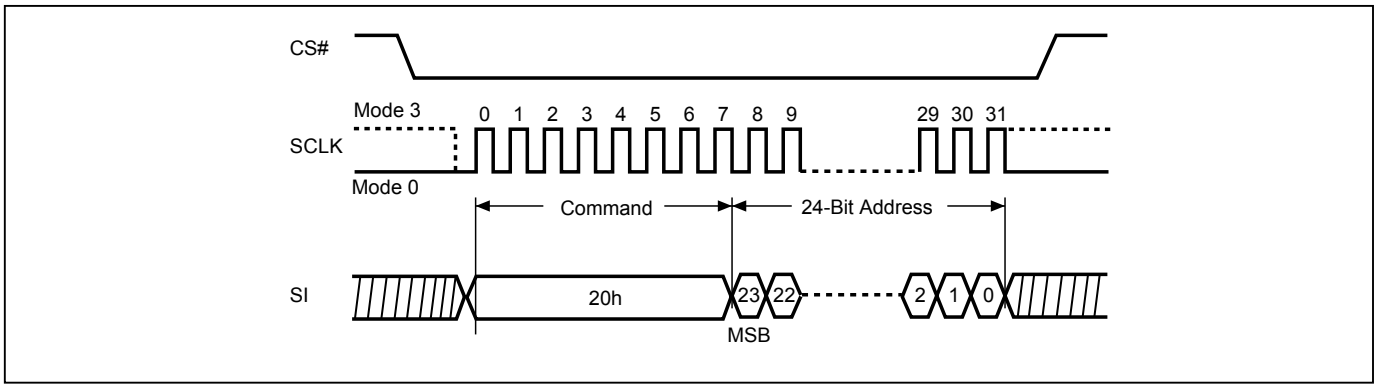
Address bits [Am-A12] (Am is the most significant address) select the sector address.

The sequence of issuing SE instruction is: CS# goes low→ sending SE instruction code→ 3-byte address on SI→ CS# goes high.

The SIO[3:1] are "don't care".

The self-timed Sector Erase Cycle time (tSE) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked during the Sector Erase cycle is in progress. The WIP sets 1 during the tSE timing, and sets 0 when Sector Erase Cycle is completed, and the Write Enable Latch (WEL) bit is reset. If the sector is protected by BP3, BP2, BP1, BP0 bits, the Sector Erase (SE) instruction will not be executed on the sector.

Figure 18. Sector Erase (SE) Sequence



9-14. Block Erase (BE32K)

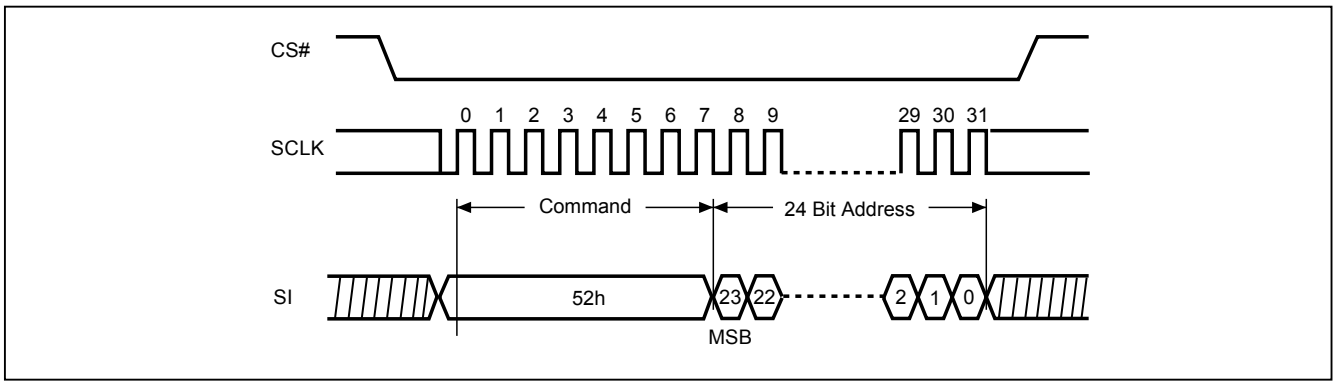
The Block Erase (BE32K) instruction is for erasing the data of the chosen block to be "1". The instruction is used for 32K-byte block erase operation. A Write Enable (WREN) instruction must be executed to set the Write Enable Latch (WEL) bit before sending the Block Erase (BE32K). Any address of the block (see *"Table 3. Memory Organization"*) is a valid address for Block Erase (BE32K) instruction. The CS# must go high exactly at the byte boundary (the least significant bit of address byte has been latched-in); otherwise, the instruction will be rejected and not executed.

The sequence of issuing BE32K instruction is: CS# goes low → sending BE32K instruction code → 3-byte address on SI → CS# goes high.

The SIO[3:1] are don't care.

The self-timed Block Erase Cycle time (tBE32K) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked while the Block Erase cycle is in progress. The WIP sets during the tBE32K timing, and clears when Block Erase Cycle is completed, and the Write Enable Latch (WEL) bit is cleared. If the block is protected by BP3-0, the array data will be protected (no change) and the WEL bit still be reset.

Figure 19. Block Erase 32KB (BE32K) Sequence (Command 52)



9-15. Block Erase (BE)

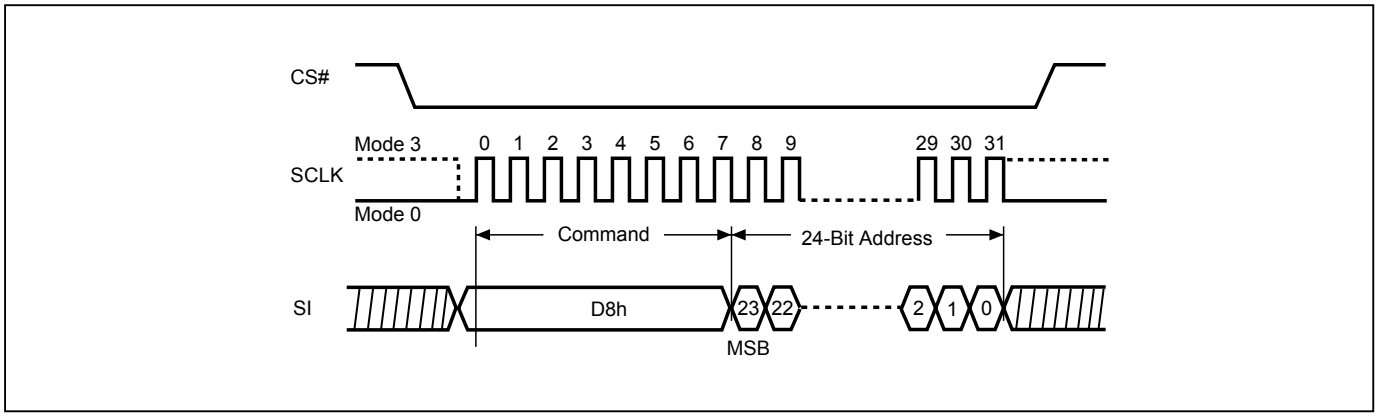
The Block Erase (BE) instruction is for erasing the data of the chosen block to be "1". The instruction is used for 64K-byte block erase operation. A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Block Erase (BE). Any address of the block (Please refer to *"Table 3. Memory Organization"*) is a valid address for Block Erase (BE) instruction. The CS# must go high exactly at the byte boundary (the latest eighth of address byte been latched-in); otherwise, the instruction will be rejected and not executed.

The sequence of issuing BE instruction is: CS# goes low→ sending BE instruction code→ 3-byte address on SI→ CS# goes high.

The SIO[3:1] are "don't care".

The self-timed Block Erase Cycle time (tBE) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked during the Block Erase cycle is in progress. The WIP sets 1 during the tBE timing, and sets 0 when Block Erase Cycle is completed, and the Write Enable Latch (WEL) bit is reset. If the block is protected by BP3, BP2, BP1, BP0 bits, the Block Erase (BE) instruction will not be executed on the block.

Figure 20. Block Erase (BE) Sequence



9-16. Chip Erase (CE)

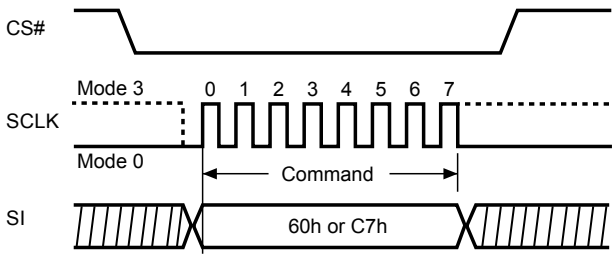
The Chip Erase (CE) instruction is for erasing the data of the whole chip to be "1". A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Chip Erase (CE). The CS# must go high exactly at the byte boundary, otherwise the instruction will be rejected and not executed.

The sequence of issuing CE instruction is: CS# goes low→sending CE instruction code→CS# goes high.

The SIO[3:1] are "don't care".

The self-timed Chip Erase Cycle time (tCE) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked during the Chip Erase cycle is in progress. The WIP sets 1 during the tCE timing, and sets 0 when Chip Erase Cycle is completed, and the Write Enable Latch (WEL) bit is reset. If the chip is protected by BP3, BP2, BP1, BP0 bits, the Chip Erase (CE) instruction will not be executed. It will be only executed when BP3, BP2, BP1, BP0 all set to "0".

Figure 21. Chip Erase (CE) Sequence



9-17. Page Program (PP)

The Page Program (PP) instruction is for programming the memory to be "0". A Write Enable (WREN) instruction must be executed to set the Write Enable Latch (WEL) bit before sending the Page Program (PP). The device programs only the last 256 data bytes sent to the device. The last address byte (the 8 least significant address bits, A7-A0) should be set to 0 for 256 bytes page program. If A7-A0 are not all zero, transmitted data that exceed page length are programmed from the starting address (24-bit address that last 8 bit are all 0) of currently selected page. If the data bytes sent to the device exceeds 256, the last 256 data byte is programmed at the request page and previous data will be disregarded. If the data bytes sent to the device has not exceeded 256, the data will be programmed at the request address of the page. There will be no effort on the other data bytes of the same page.

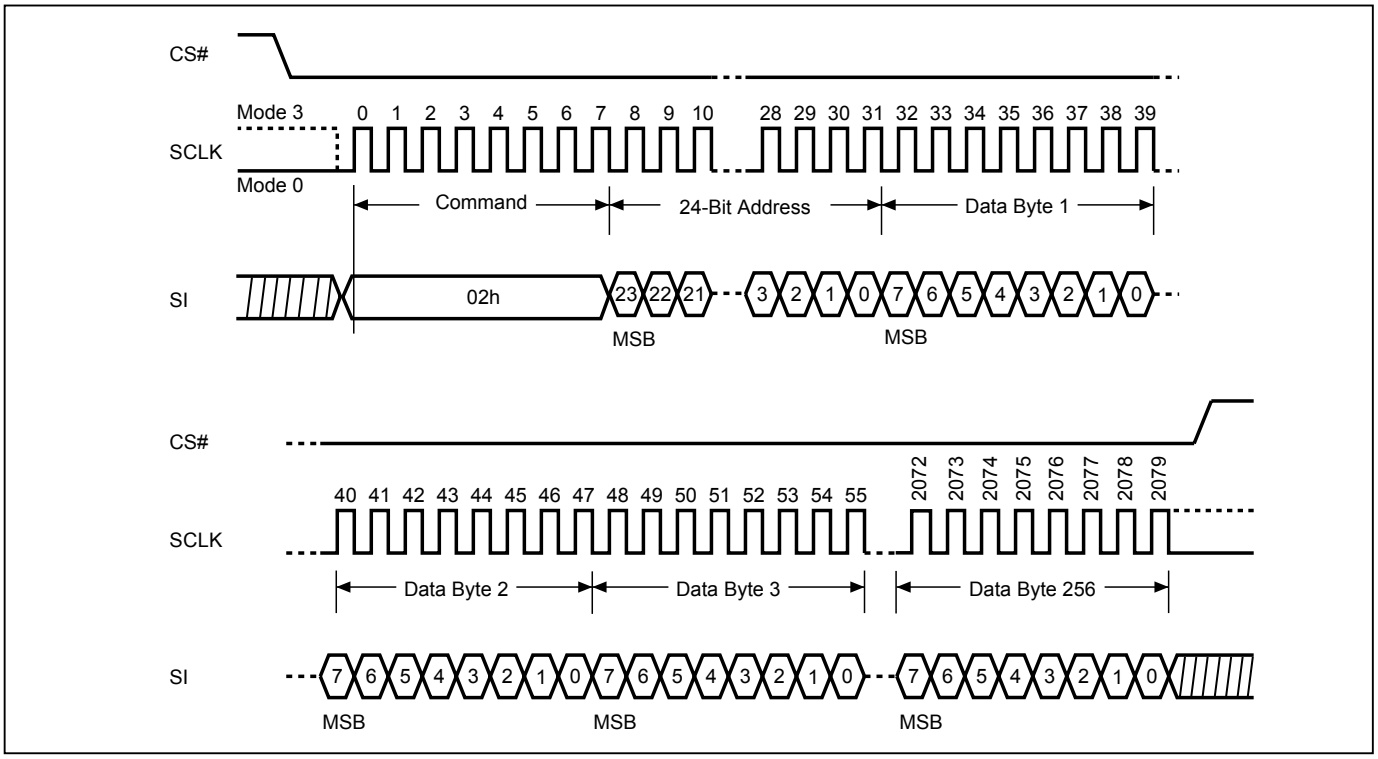
The sequence of issuing PP instruction is: CS# goes low→ sending PP instruction code→ 3-byte address on SI→ at least 1-byte on data on SI→ CS# goes high.

The CS# must be kept low during the whole Page Program cycle; The CS# must go high exactly at the byte boundary (the latest eighth bit of data being latched in), otherwise the instruction will be rejected and will not be executed.

The self-timed Page Program Cycle time (tPP) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked during the Page Program cycle is in progress. The WIP sets 1 during the tPP timing, and sets 0 when Page Program Cycle is completed, and the Write Enable Latch (WEL) bit is reset. If the page is protected by BP3, BP2, BP1, BP0 bits, the Page Program (PP) instruction will not be executed.

The SIO[3:1] are "don't care".

Figure 22. Page Program (PP) Sequence



9-18. Deep Power-down (DP)

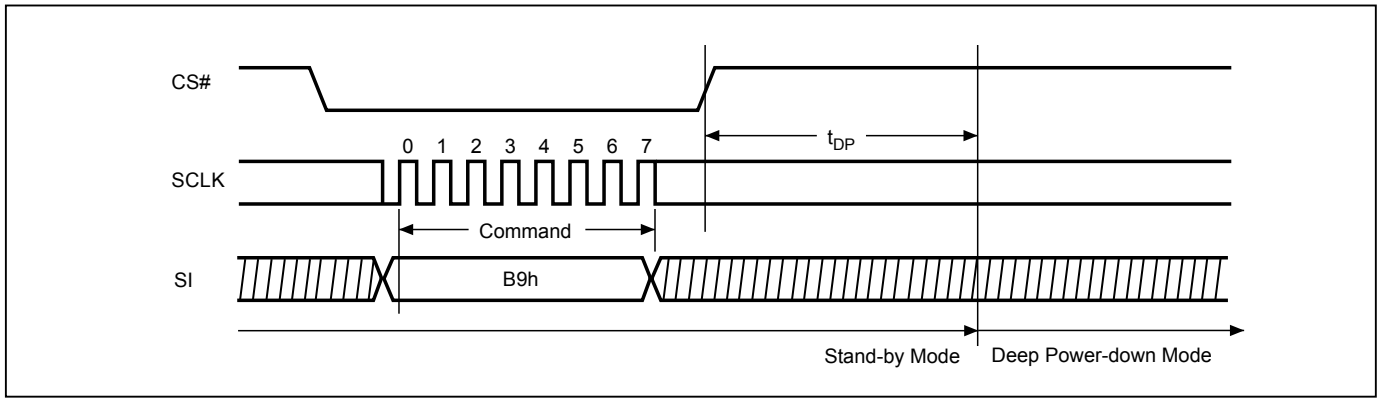
The Deep Power-down (DP) instruction places the device into a minimum power consumption state, Deep Power-down mode, in which the quiescent current is reduced from ISB1 to ISB2.

The sequence of issuing DP instruction: CS# goes low→ send DP instruction code→ CS# goes high. The CS# must go high at the byte boundary (after exactly eighth bits of the instruction code have been latched-in); otherwise the instruction will not be executed. SIO[3:1] are "don't care".

After CS# goes high there is a delay of tDP before the device transitions from Stand-by mode to Deep Powerdown mode and before the current reduces from ISB1 to ISB2. Once in Deep Power-down mode, all instructions will be ignored except Release from Deep Power-down (RDP).

The device exits Deep Power-down mode and returns to Stand-by mode if it receives a Release from Deep Power-down (RDP) instruction, power-cycle. Please refer to *"Figure 25. Release from Deep Power-down (RDP) Sequence"*.

Figure 23. Deep Power-down (DP) Sequence



9-19. Release from Deep Power-down (RDP), Read Electronic Signature (RES)

The Release from Deep Power-down (RDP) instruction is completed by driving Chip Select (CS#) High. When Chip Select (CS#) is driven High, the device is put in the standby Power mode. If the device was not previously in the Deep Power-down mode, the transition to the standby Power mode is immediate. If the device was previously in the Deep Power-down mode, though, the transition to the standby Power mode is delayed by tRES1, and Chip Select (CS#) must remain High for at least tRES1(max). Once in the standby mode, the device waits to be selected, so that it can receive, decode and execute instructions.

RES instruction is for reading out the old style of 8-bit Electronic Signature, whose values are shown as *"Table 5. ID Definitions"*. This is not the same as RDID instruction. It is not recommended to use for new design. For new design, please use RDID instruction. Even in Deep power-down mode, the RDP and RES are also allowed to be executed, only except the device is in progress of program/erase/write cycles; there's no effect on the current program/erase/write cycles in progress.

The SIO[1:0] are don't care when during this mode.

The RES instruction is ended by CS# goes high after the ID been read out at least once. The ID outputs repeatedly if continuously send the additional clock cycles on SCLK while CS# is at low. If the device was not previously in Deep Power-down mode, the device transition to standby mode is immediate. If the device was previously in Deep Power-down mode, there's a delay of tRES2 to transit to standby mode, and CS# must remain to high at least tRES2(max). Once in the standby mode, the device waits to be selected, so it can receive, decode, and execute instruction.

The RDP instruction is for releasing from Deep Power-down Mode.

Figure 24. Read Electronic Signature (RES) Sequence

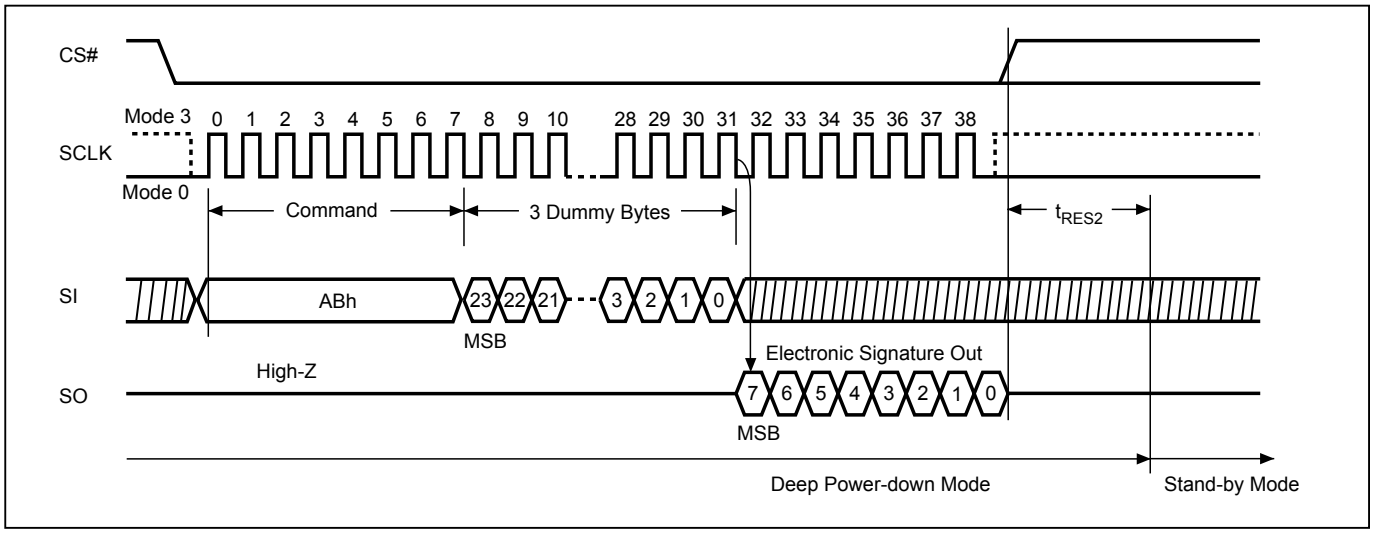
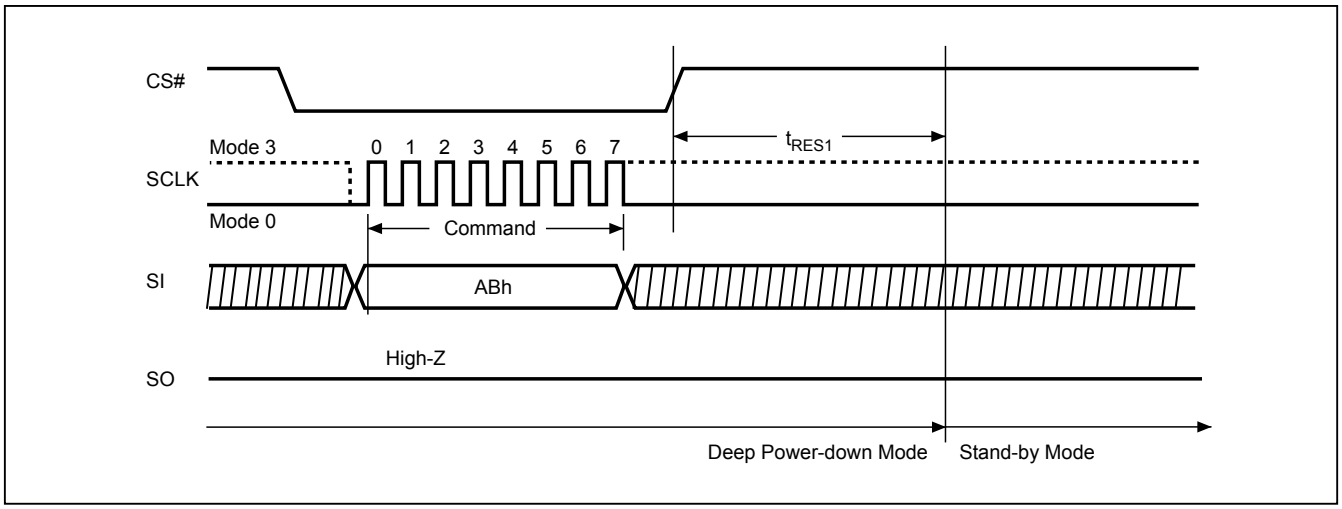


Figure 25. Release from Deep Power-down (RDP) Sequence



9-20. Software Reset (Reset-Enable (RSTEN) and Reset (RST))

The Software Reset operation combines two instructions: Reset-Enable (RSTEN) command and Reset (RST) command. It returns the device to a standby mode. All the volatile bits and settings will be cleared then, which makes the device return to the default status as power on.

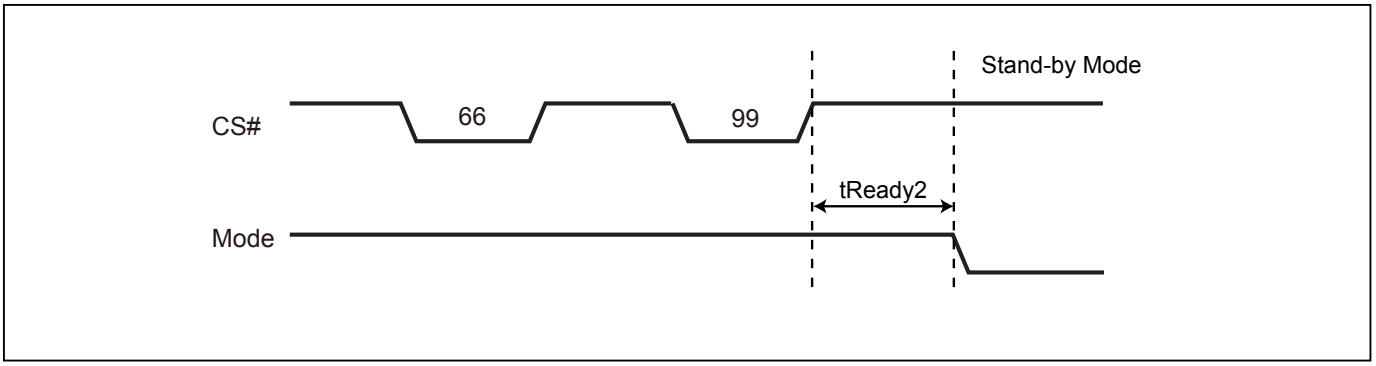
To execute Reset command (RST), the Reset-Enable (RSTEN) command must be executed first to perform the Reset operation. If there is any other command to interrupt after the Reset-Enable command, the Reset-Enable will be invalid.

The SIO[3:1] are "don't care".

If the Reset command is executed during program or erase operation, the operation will be disabled, the data under processing could be damaged or lost.

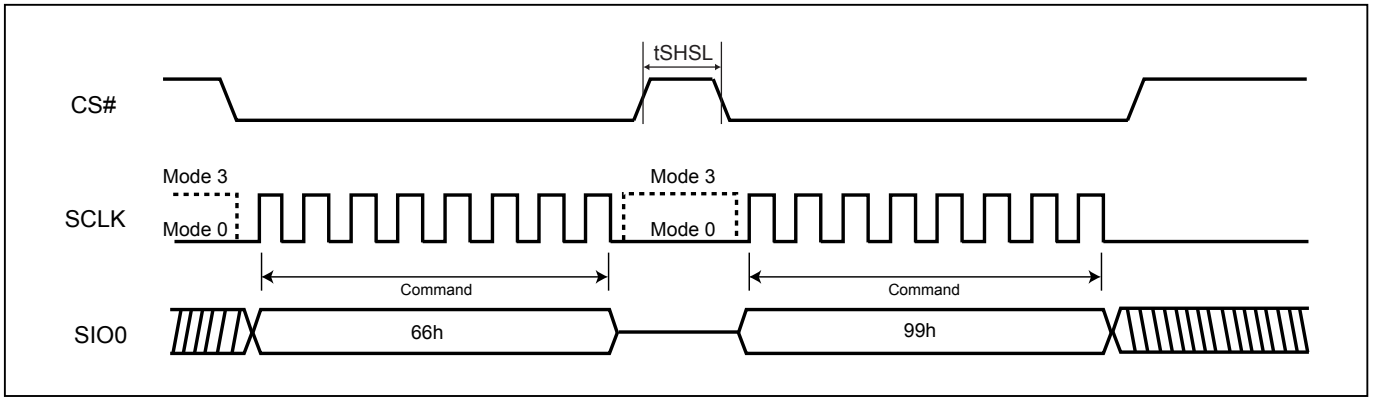
The reset time is different depending on the last operation. Longer latency time is required to recover from a program operation than from other operations.

Figure 26. Software Reset Recovery



Note: Refer to **Table 11. AC Characteristics** for tREADY2 data.

Figure 27. Reset Sequence



9-21. Read SFDP Mode (RDSFDP)

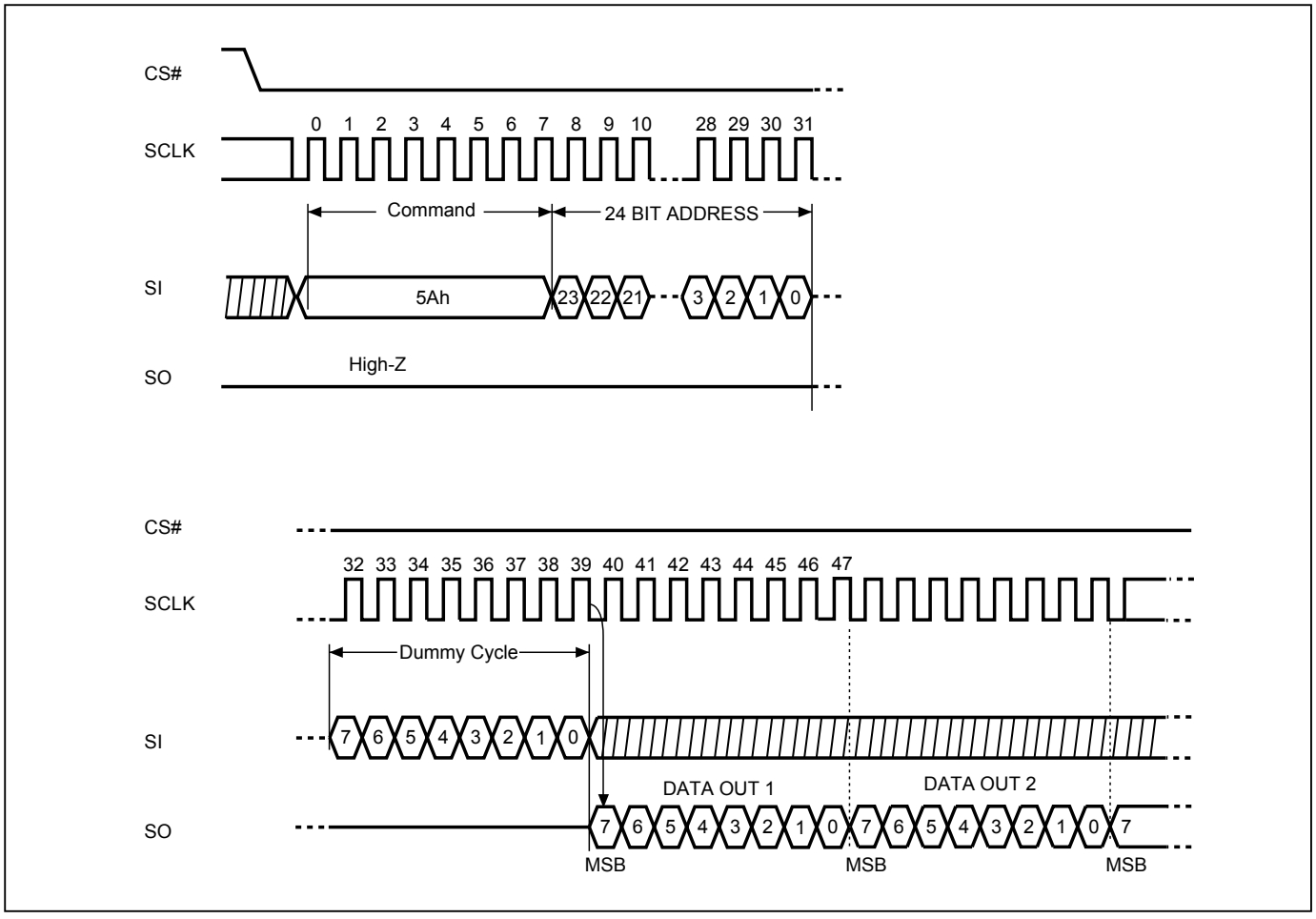
The Serial Flash Discoverable Parameter (SFDP) standard provides a consistent method of describing the functional and feature capabilities of serial flash devices in a standard set of internal parameter tables. These parameter tables can be interrogated by host system software to enable adjustments needed to accommodate divergent features from multiple vendors. The concept is similar to the one found in the Introduction of JEDEC Standard, JESD68 on CFI.

The sequence of issuing RDSFDP instruction is same as FAST_READ: CS# goes low→send RDSFDP instruction (5Ah)→send 3 address bytes on SI pin→send 1 dummy byte on SI pin→read SFDP code on SO→to end RDSFDP operation can use CS# to high at any time during data out.

SFDP is a JEDEC Standard, JESD216.

For SFDP register values detail, please contact local Macronix sales channel for Application Note.

Figure 28. Read Serial Flash Discoverable Parameter (RDSFDP) Sequence



9-22. Factory Mode Sector Erase

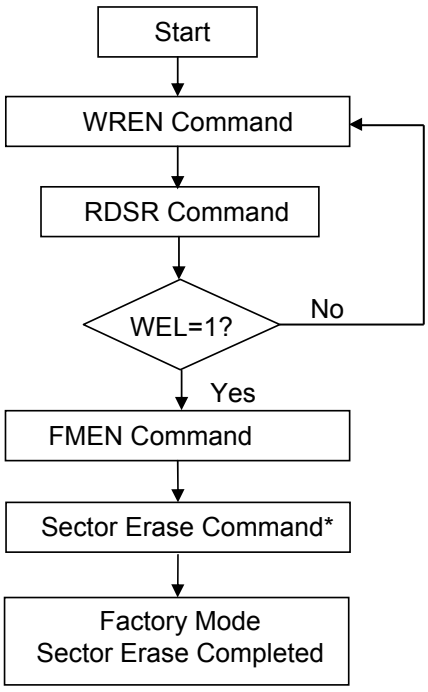
To apply Factory Mode Sector Erase, customers need to follow the operation below:

Factory Mode Enable (FMEN): The Factory Mode Enable (FMEN) instruction is for enhancing Sector Erase performance, which increase factory production throughput. The FMEN instruction will need to be combined with the SE instruction when user intends to change the device content.

A valid factory mode operation need to include three sequences: WREN instruction → FMEN instruction→ Sector Erase instruction. The sequence of issuing FMEN instruction is: CS# goes low→send FMEN instruction code→ CS# goes high.

The FMEN will be reset in following situations: Power-up, Sector Erase command completion.

Figure 29. Factory Mode Sector Erase Flow



***Note:** * Please reference Program/Erase flow chart in datasheet.*

9-23. Factory Mode 32KB Block Erase

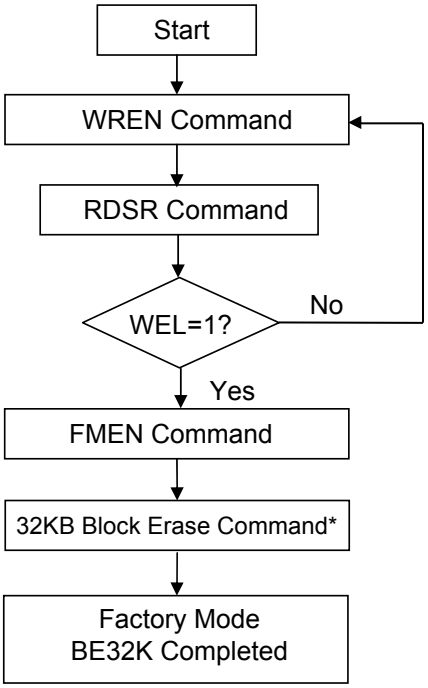
To apply Factory Mode 32KB Block Erase, customers need to follow the operation below:

Factory Mode Enable (FMEN): The Factory Mode Enable (FMEN) instruction is for enhancing 32KB Block Erase performance, which increase factory production throughput. The FMEN instruction will need to be combined with the BE32K instruction when user intends to change the device content.

A valid factory mode operation need to include three sequences: WREN instruction → FMEN instruction→ BE32K instruction. The sequence of issuing FMEN instruction is: CS# goes low→send FMEN instruction code→ CS# goes high.

The FMEN will be reset in following situations: Power-up, BE32K command completion.

Figure 30. Factory Mode 32KB Block Erase Flow



***Note:** * Please reference Program/Erase flow chart in datasheet.*

9-24. Factory Mode 64KB Block Erase

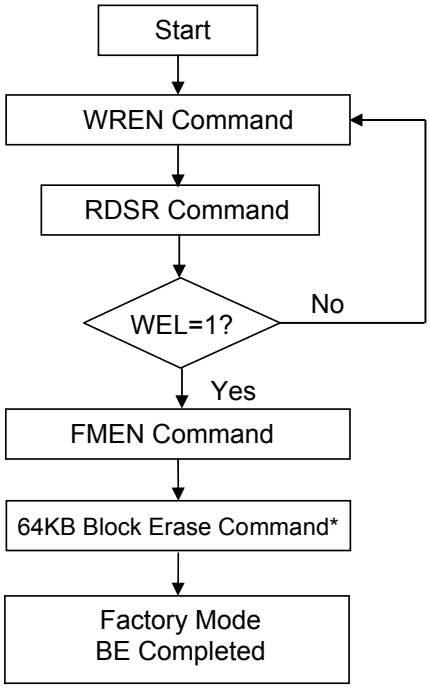
To apply Factory Mode 64KB Block Erase, customers need to follow the operation below:

Factory Mode Enable (FMEN): The Factory Mode Enable (FMEN) instruction is for enhancing 64KB Block Erase performance, which increase factory production throughput. The FMEN instruction will need to be combined with the BE instruction when user intends to change the device content.

A valid factory mode operation need to include three sequences: WREN instruction → FMEN instruction→ BE instruction. The sequence of issuing FMEN instruction is: CS# goes low→send FMEN instruction code→ CS# goes high.

The FMEN will be reset in following situations: Power-up, BE command completion.

Figure 31. Factory Mode Block Erase Flow



***Note:** * Please reference Program/Erase flow chart in datasheet.*

9-25. Factory Mode Chip Erase

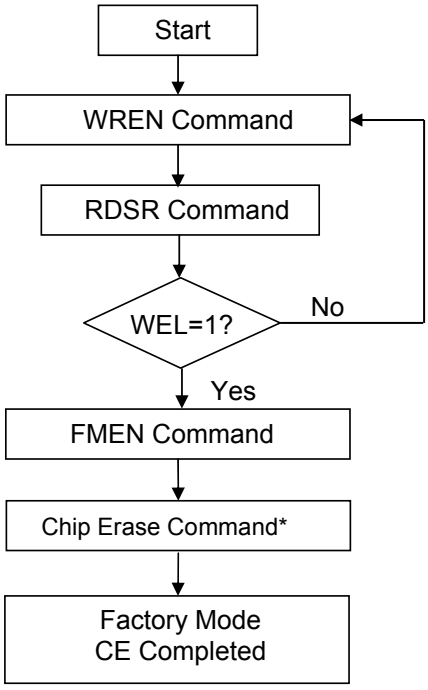
To apply Factory Mode Chip Erase, customers need to follow the operation below:

Factory Mode Enable (FMEN): The Factory Mode Enable (FMEN) instruction is for enhancing Chip Erase performance, which increase factory production throughput. The FMEN instruction will need to be combined with the CE instruction when user intends to change the device content.

A valid factory mode operation need to include three sequences: WREN instruction → FMEN instruction→ CE instruction. The sequence of issuing FMEN instruction is: CS# goes low→send FMEN instruction code→ CS# goes high.

The FMEN will be reset in following situations: Power-up, CE command completion.

Figure 32. Factory Mode Chip Erase Flow



***Note:** * Please reference Program/Erase flow chart in datasheet.*

10. POWER-ON STATE

The device is at the following states when power-up:
- Standby mode (please note it is not deep power-down mode)
- Write Enable Latch (WEL) bit is reset

The device must not be selected during power-up and power-down stage until the VCC reaches the following levels:
- VCC minimum at power-up stage and then after a delay of tVSL
- GND at power-down

Please note that a pull-up resistor on CS# may ensure a safe and proper power-up/down level.

An internal power-on reset (POR) circuit may protect the device from data corruption and inadvertent data change during power up state. When VCC is lower than VWI (POR threshold voltage value), the internal logic is reset and the flash device has no response to any command.

For further protection on the device, if the VCC does not reach the VCC minimum level, the correct operation is not guaranteed. The write, erase, and program command should be sent after the below time delay:
- tVSL after VCC reached VCC minimum level

The device can accept read command after VCC reached VCC minimum and a time delay of tVSL.
Please refer to the *"Figure 40. Power-up Timing"*.

Note:
- To stabilize the VCC level, the VCC rail decoupled by a suitable capacitor close to package pins is recommended. (generally around 0.1uF)
- At power-down stage, the VCC drops below VWI level, all operations are disable and device has no response to any command. The data corruption might occur during this stage if a write, program, erase cycle is in progress.

11. ELECTRICAL SPECIFICATIONS

Table 8. Absolute Maximum Ratings

Rating		Value
Ambient Operating Temperature	Industrial grade	-40°C to 85°C
Storage Temperature		-65°C to 150°C
Applied Input Voltage		-0.5V to VCC+0.5V
Applied Output Voltage		-0.5V to VCC+0.5V
VCC to Ground Potential		-0.5V to 4.0V

NOTICE:
1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is stress rating only and functional operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.
2. Specifications contained within the following tables are subject to change.
3. During voltage transitions, all pins may overshoot to VCC+1.0V or -1.0V for period up to 20ns.

Figure 33. Maximum Negative Overshoot Waveform

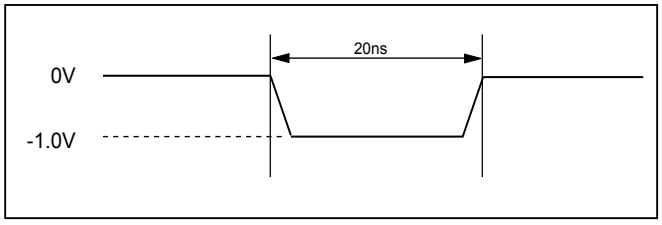


Figure 34. Maximum Positive Overshoot Waveform

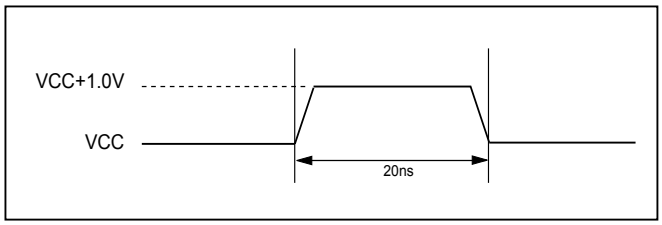
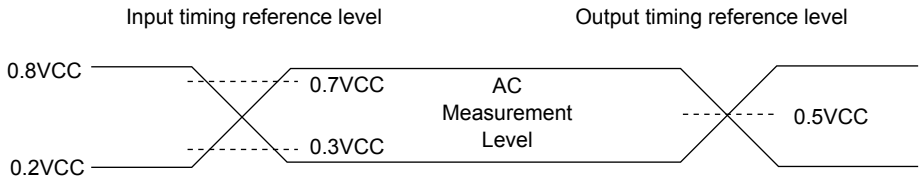


Table 9. Capacitance

TA = 25°C, f = 1.0 MHz

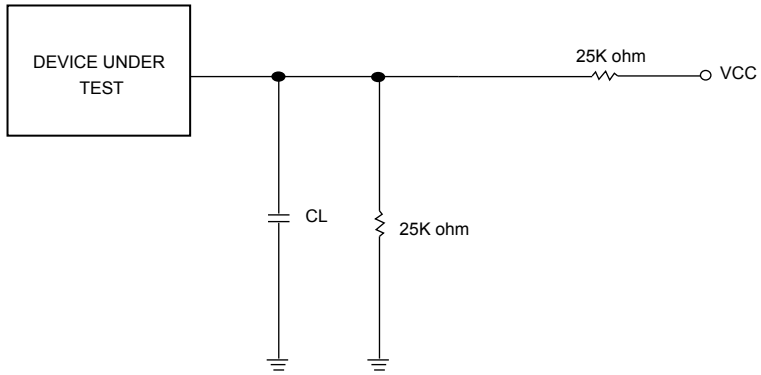
Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
CIN	Input Capacitance			6	pF	VIN = 0V
COUT	Output Capacitance			8	pF	VOUT = 0V

Figure 35. Data Input Test Waveforms and Measurement Level



Note: Input pulse rise and fall time are <5ns

Figure 36. Output Loading



CL=15/30pF Including jig capacitance

Figure 37. SCLK TIMING DEFINITION

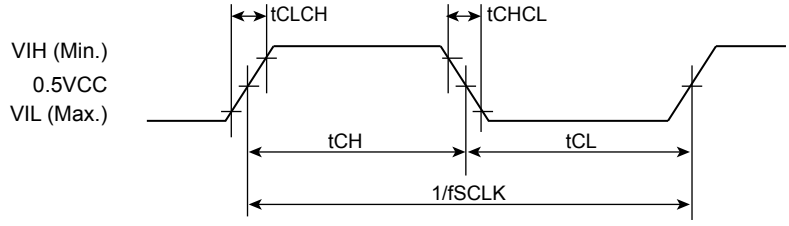


Table 10. DC Characteristics

Symbol	Parameter	Notes	Min.	Typ.	Max.	Units	Test Conditions
ILI	Input Load Current	1			±2	uA	VCC = VCC Max, VIN = VCC or GND
ILO	Output Leakage Current	1			±2	uA	VCC = VCC Max, VOUT = VCC or GND
ISB1	VCC Standby Current	1		2	20	uA	VIN = VCC or GND, CS# = VCC
ISB2	Deep Power-down Current			2	20	uA	VIN = VCC or GND, CS# = VCC
ICC1	VCC Read	1			6	mA	f=50MHz SCLK=0.1VCC/0.9VCC, SO=Open
				4	6	mA	f=80MHz (2x I/O) SCLK=0.1VCC/0.9VCC, SO=Open
ICC2	VCC Program Current (PP)	1		5	15	mA	Program in Progress, CS# = VCC
ICC3	VCC Write Status Register (WRSR) Current			5	15	mA	Program status register in progress, CS#=VCC
ICC4	VCC Sector/Block (64K) Erase Current (SE/BE)	1		5	15	mA	Erase in Progress, CS#=VCC
ICC5	VCC Chip Erase Current (CE)	1		4.5	15	mA	Erase in Progress, CS#=VCC
VIL	Input Low Voltage		-0.5		0.3VCC	V	
VIH	Input High Voltage		0.7VCC		VCC+0.4	V	
VOL	Output Low Voltage				0.2	V	IOL = 100uA
VOH	Output High Voltage		VCC-0.2			V	IOH = -100uA

Notes :
1. Device operation range: 2.3V-3.6V, Typical values at VCC = 3.0V, T = 25°C. These currents are valid for all product versions (package and speeds).
2. Typical value is calculated by simulation.

Table 11. AC Characteristics

Symbol	Alt.	Parameter			Min.	Typ.(2)	Max.	Unit
fSCLK	fC	Clock Frequency for the following instructions: FAST_READ, RDSFDP, PP, SE, BE32K, BE, CE, DP, RES, WREN, WRDI, RDID, RDSR, WRSR		VCC: 2.3V-2.7V	D.C.		50	MHz
				VCC: 2.7V-3.6V	D.C.		80	MHz
fRSCLK	fR	Clock Frequency for READ instructions		VCC: 2.3V-2.7V			33	MHz
				VCC: 2.7V-3.6V			50	MHz
fTSCLK	fT	Clock Frequency for DREAD instructions		VCC: 2.3V-2.7V			50	MHz
				VCC: 2.7V-3.6V			80	MHz
tCH(1)	tCLH	Clock High Time	Others (fSCLK)		45%x (1/fSCLK)			ns
			Normal Read (fRSCLK)		13			ns
tCL(1)	tCLL	Clock Low Time	Others (fSCLK)		45%x (1/fSCLK)			ns
			Normal Read (fRSCLK)		13			ns
tCLCH(4)		Clock Rise Time (peak to peak)			0.1			V/ns
tCHCL(4)		Clock Fall Time (peak to peak)			0.1			V/ns
tSLCH	tCSS	CS# Active Setup Time (relative to SCLK)			7			ns
tCHSL		CS# Not Active Hold Time (relative to SCLK)			7			ns
tDVCH	tDSU	Data In Setup Time			3			ns
tCHDX	tDH	Data In Hold Time			5			ns
tCHSH		CS# Active Hold Time (relative to SCLK)			7			ns
tSHCH		CS# Not Active Setup Time (relative to SCLK)			7			ns
tSHSL	tCSH	CS# Deselect Time	From Read to next Read		20			ns
			From Write/Erase/Program to Read Status Register		40			ns
tSHQZ(4)	tDIS	Output Disable Time					6	ns
tCLQV	tV	Clock Low to Output Valid Loading: 30pF/15pF	Loading: 30pF				8	ns
			Loading: 15pF				6	ns
tCLQX	tHO	Output Hold Time			0			ns
tWHSL(3)		Write Protect Setup Time			20			ns
tSHWL(3)		Write Protect Hold Time			100			ns
tDP		CS# High to Deep Power-down Mode					10	us
tRES1		CS# High to Standby Mode without Electronic Signature Read					8.8	us
tRES2		CS# High to Standby Mode with Electronic Signature Read					8.8	us
tW		Write Status Register Cycle Time				5	40	ms

AC Characteristics - continued

Symbol	Alt.	Parameter		Min.	Typ.(2)	Max.	Unit
tBP		Byte-Program	VCC: 2.3V-2.7V		43	200	us
			VCC: 2.7V-3.6V		30	180	us
tPP		Page Program Cycle Time	VCC: 2.3V-2.7V		0.82	5	ms
			VCC: 2.7V-3.6V		0.73	4	ms
tSE		Sector Erase Cycle Time	VCC: 2.3V-2.7V		75	750	ms
			VCC: 2.7V-3.6V		73	500	ms
tBE32K		Block Erase (32KB) Cycle Time	VCC: 2.3V-2.7V		0.35	4.95	s
			VCC: 2.7V-3.6V		0.34	3.8	s
tBE		Block Erase (64KB) Cycle Time	VCC: 2.3V-2.7V		0.65	5.3	s
			VCC: 2.7V-3.6V		0.62	4	s
tCE		Chip Erase Cycle Time	VCC: 2.3V-2.7V		7.5	28	s
			VCC: 2.7V-3.6V		7	22.5	s
tREADY2		Reset Recovery time (During instruction decoding)	VCC: 2.3V-3.6V	30			us
		Reset Recovery time (for read operation)	VCC: 2.3V-3.6V	30			us
		Reset Recovery time (for program operation)	VCC: 2.3V-3.6V	80			us
		Reset Recovery time(for SE4KB operation)	VCC: 2.3V-3.6V	12			ms
		Reset Recovery time (for BE32K/64K operation)	VCC: 2.3V-3.6V	25			ms
		Reset Recovery time (for Chip Erase operation)	VCC: 2.3V-3.6V	25			ms
		Reset Recovery time (for WRSR operation)	VCC: 2.3V-3.6V	0.1			ms

Notes:

1. tCH + tCL must be greater than or equal to 1/ Frequency.
2. Typical values given for TA=25°C. Not 100% tested.
3. Only applicable as a constraint for a WRSR instruction when SRWD is set at 1.
4. The value guaranteed by characterization, not 100% tested in production.
5. Test condition is shown as *"Figure 35. Data Input Test Waveforms and Measurement Level", "Figure 36. Output Loading".*

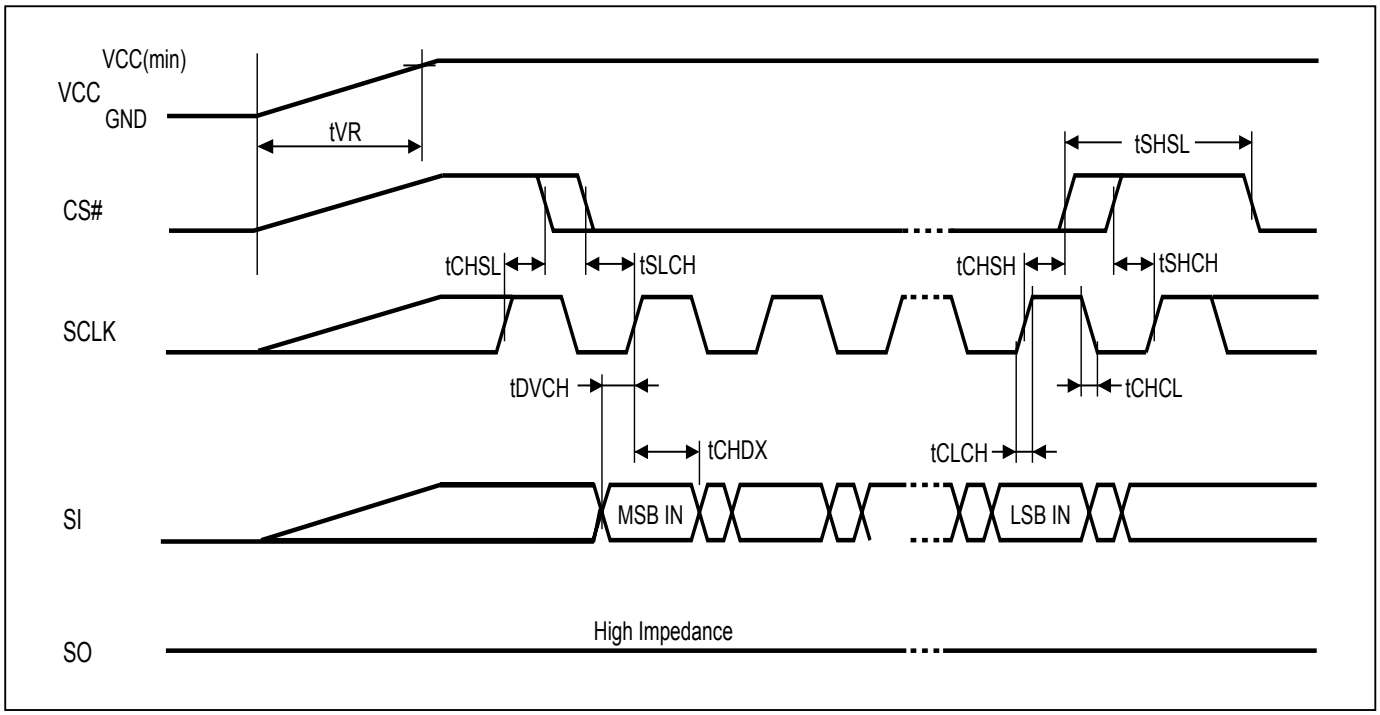
12. OPERATING CONDITIONS

At Device Power-Up and Power-Down

AC timing illustrated in *"Figure 38. AC Timing at Device Power-Up"* and *"Figure 39. Power-Down Sequence"* are for the supply voltages and the control signals at device power-up and power-down. If the timing in the figures is ignored, the device will not operate correctly.

During power-up and power-down, CS# needs to follow the voltage applied on VCC to keep the device not to be selected. The CS# can be driven low when VCC reach Vcc(min.) and wait a period of tVSL.

Figure 38. AC Timing at Device Power-Up



Symbol	Parameter	Notes	Min.	Max.	Unit
tVR	VCC Rise Time	1		500000	us/V

Notes :
1. Sampled, not 100% tested.
2. For AC spec tCHSL, tSLCH, tDVCH, tCHDX, tSHSL, tCHSH, tSHCH, tCHCL, tCLCH in the figure, please refer to *"Table 11. AC Characteristics"*.

Figure 39. Power-Down Sequence

During power-down, CS# needs to follow the voltage drop on VCC to avoid mis-operation.

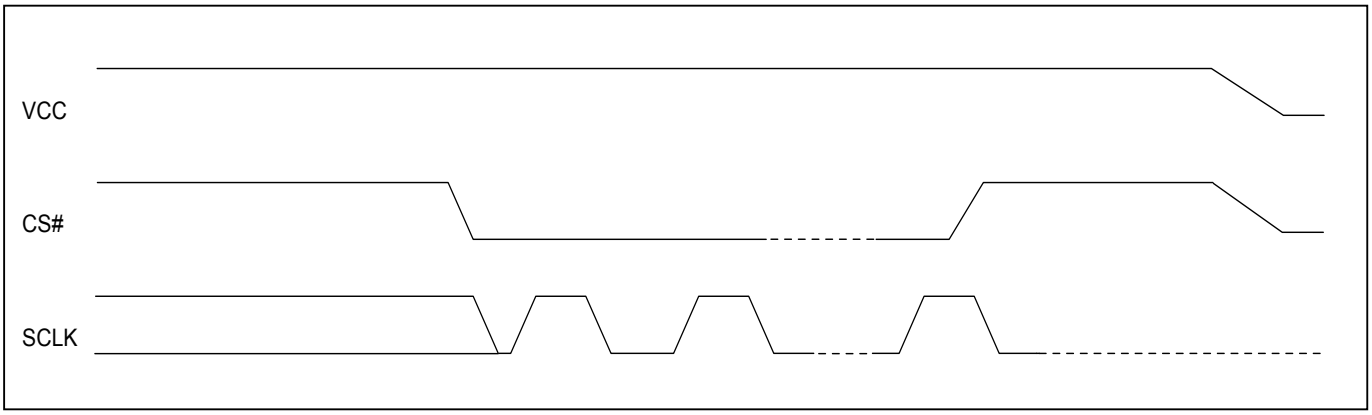


Figure 40. Power-up Timing

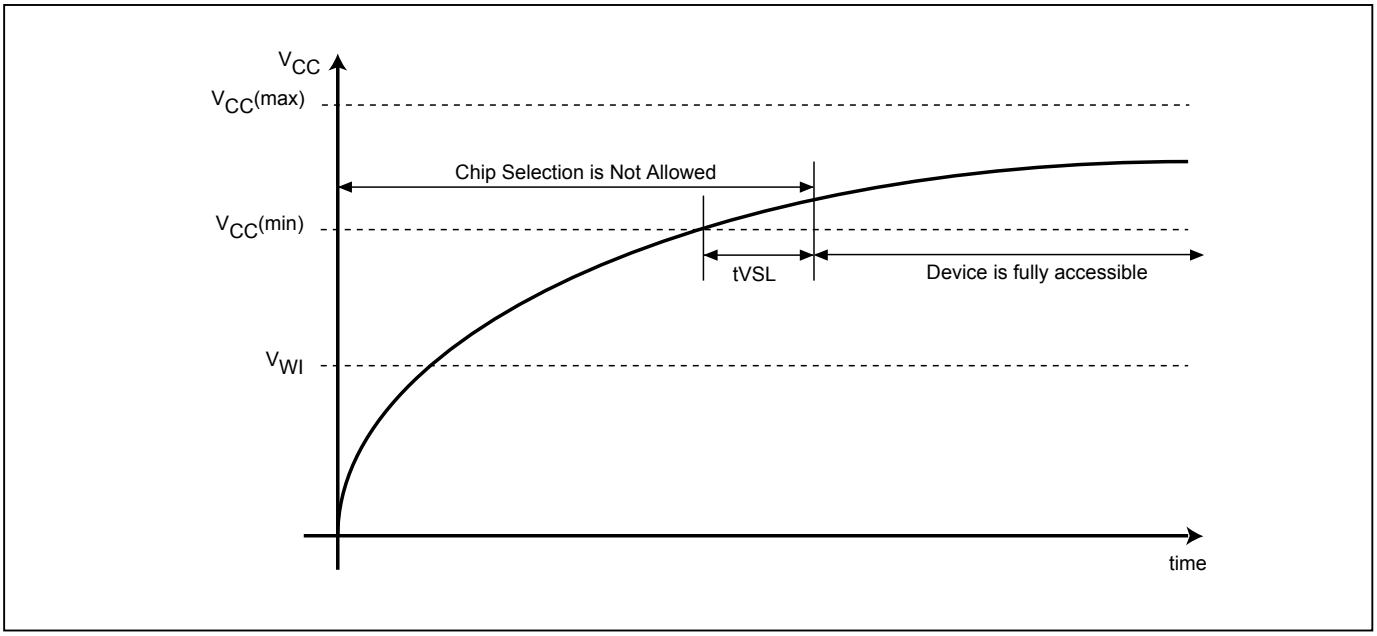


Figure 41. Power Up/Down and Voltage Drop

When powering down the device, VCC must drop below V_{PWD} for at least tPWD to ensure the device will initialize correctly during power up. Please refer to *"Figure 41. Power Up/Down and Voltage Drop"* and *"Table 12. Power-Up/Down Voltage and Timing"* below for more details.

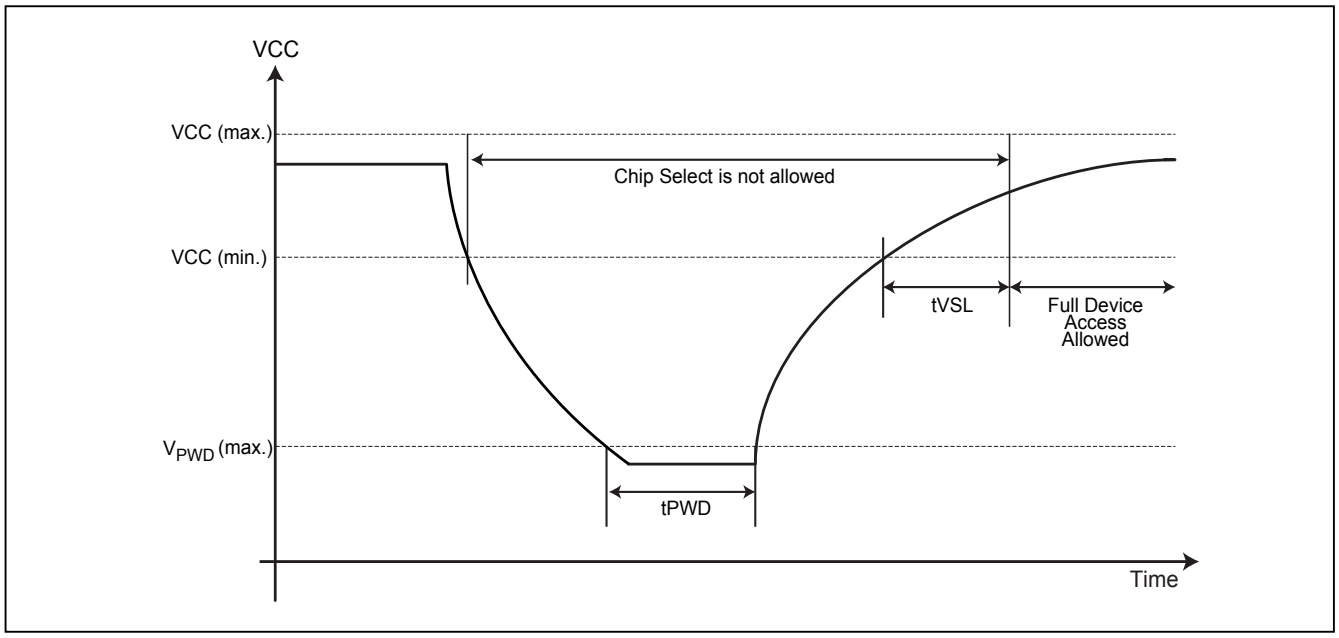


Table 12. Power-Up/Down Voltage and Timing

Symbol	Parameter	Min.	Max.	Unit
tVSL	VCC(min.) to device operation	500		us
VWI	Write Inhibit Voltage	1.5	2.1	V
V_{PWD}	VCC voltage needed to below V_{PWD} for ensuring initialization will occur		0.9	V
tPWD	The minimum duration for ensuring initialization will occur	300		us

Note: These parameters are characterized only.

12-1. Initial Delivery State

The device is delivered with the memory array erased: all bits are set to 1 (each byte contains FFh). The Status Register contains 00h (all Status Register bits are 0).

13. ERASE AND PROGRAMMING PERFORMANCE

PARAMETER		Min.	Typ.(1)	Max.(2)	Unit
Write Status Register Cycle Time			5	40	ms
Sector Erase Cycle Time (4KB)	VCC: 2.3V-2.7V		75	750	ms
	VCC: 2.7V-3.6V		73	500	ms
Block Erase Cycle Time (32KB)	VCC: 2.3V-2.7V		0.35	4.95	s
	VCC: 2.7V-3.6V		0.34	3.8	s
Block Erase Cycle Time (64KB)	VCC: 2.3V-2.7V		0.65	5.3	s
	VCC: 2.7V-3.6V		0.62	4	s
Chip Erase Cycle Time	VCC: 2.3V-2.7V		7.5	28	s
	VCC: 2.7V-3.6V		7	22.5	s
Byte Program Time	VCC: 2.3V-2.7V		43	200	us
	VCC: 2.7V-3.6V		30	180	us
Page Program Time	VCC: 2.3V-2.7V		0.82(4)	5	ms
	VCC: 2.7V-3.6V		0.73(4)	4	ms
Erase/Program Cycle			100,000		cycles

Notes:
1. Typical erase assumes the following conditions: 25°C, typical operation voltage and all zero pattern.
2. Under worst conditions of 85°C and minimum operation voltage.
3. System-level overhead is the time required to execute the first-bus-cycle sequence for the programming command.
4. Typical program assumes the following conditions: 25°C, typical VCC, and checkerboard pattern.

14. ERASE AND PROGRAMMING PERFORMANCE (Factory Mode)

Parameter	Min.	Typ.	Max.	Unit
Sector Erase Cycle Time (4KB)		24		ms
Block Erase Cycle Time (32KB)		0.16		s
Block Erase Cycle Time (64KB)		0.32		s
Chip Erase Cycle Time		6		s
Page Program Time		0.54		ms
Erase/Program Cycle			50	cycles

Notes:
1. Factory Mode must be operated in 20°C to 45°C and VCC 3.0V-3.6V.
2. In Factory mode, the Erase/Program operation should not exceed 50 cycles, and "ERASE AND PROGRAMMING PERFORMANCE" 100k cycles will not be affected.

15. LATCH-UP CHARACTERISTICS

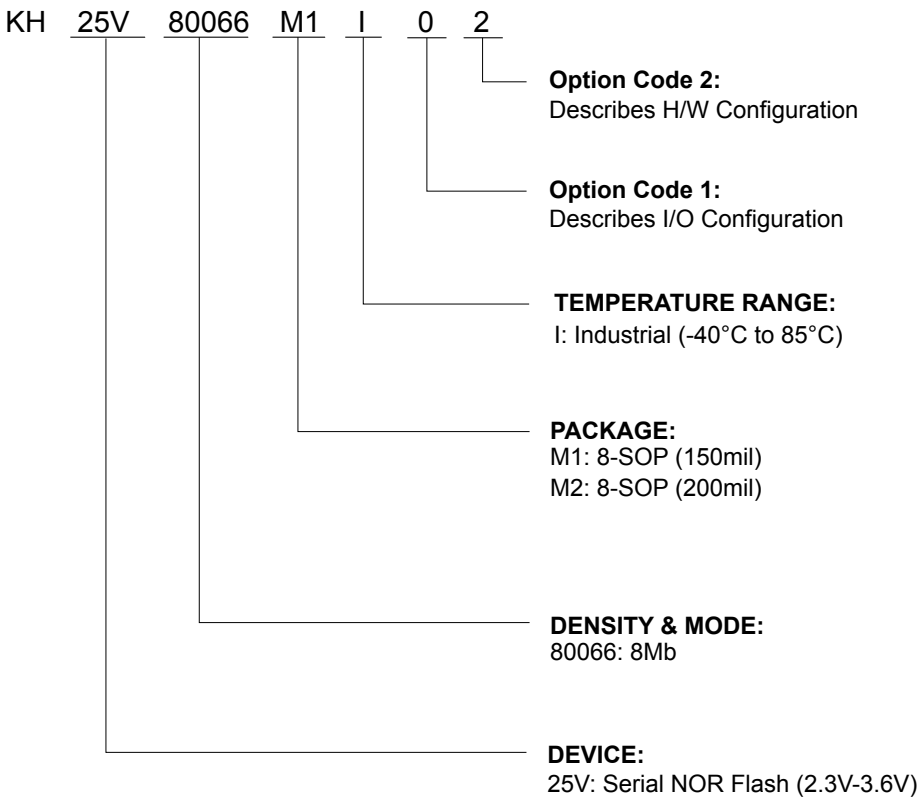
	Min.	Max.
Input Voltage with respect to GND on all power pins		1.5 VCCmax
Input Current on all non-power pins	-100mA	+100mA
Test conditions: VCC = VCCmax, one pin at a time (compliant to JEDEC JESD78 standard).		

16. ORDERING INFORMATION

Please contact Macronix regional sales for the latest product selection and available form factors.

PART NO.	Package	Temp.	I/O Configuration		H/W Configuration	Remark
			Default I/O	Dummy Cycle	Addressing	
KH25V80066M1I02	8-SOP (150mil)	-40°C to 85°C	Standard	Standard	Standard	
KH25V80066M2I02	8-SOP (200mil)	-40°C to 85°C	Standard	Standard	Standard	

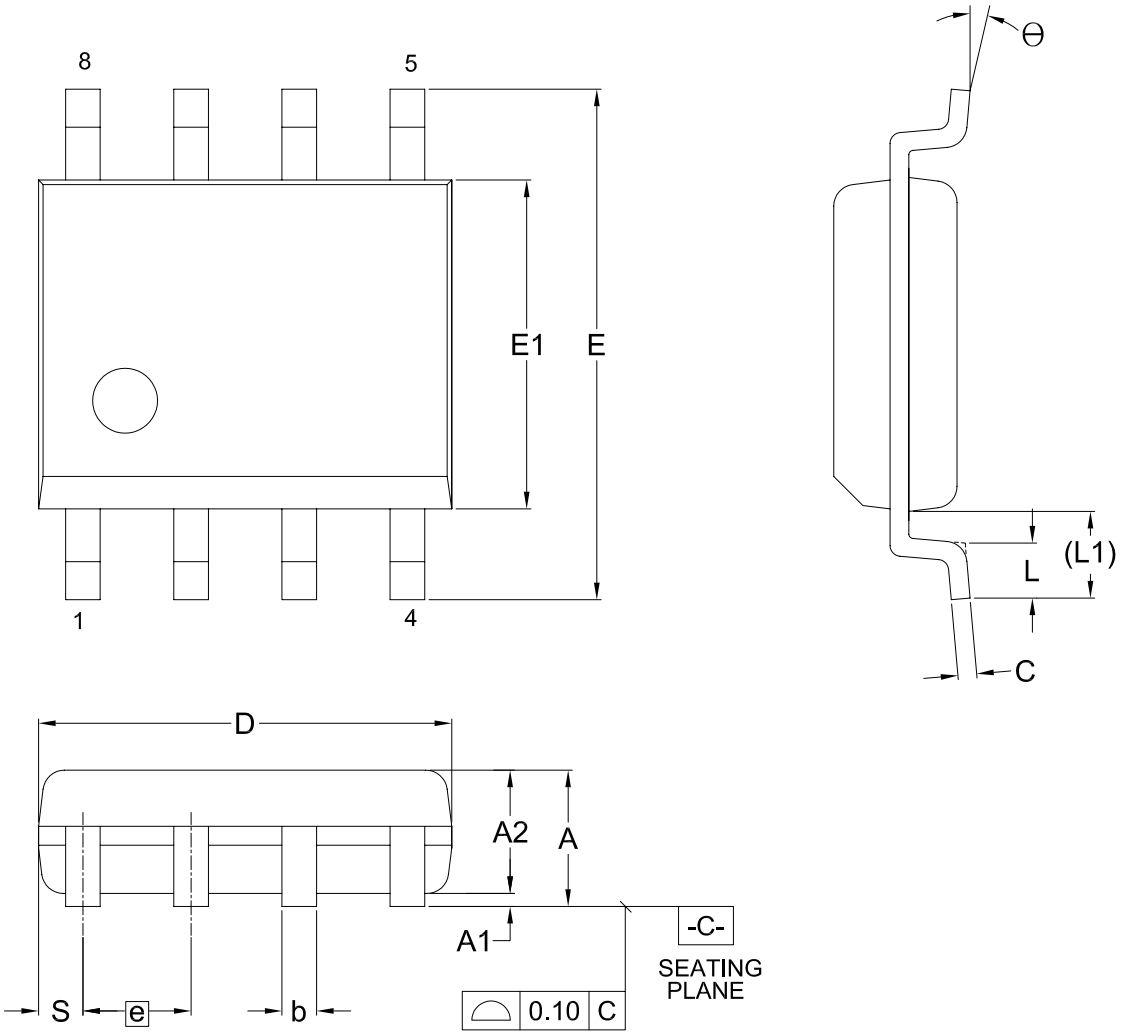
17. PART NAME DESCRIPTION



18. PACKAGE INFORMATION

18-1. 8-pin SOP (150mil)

Doe. Title: Package Outline for SOP 8L (150MIL)

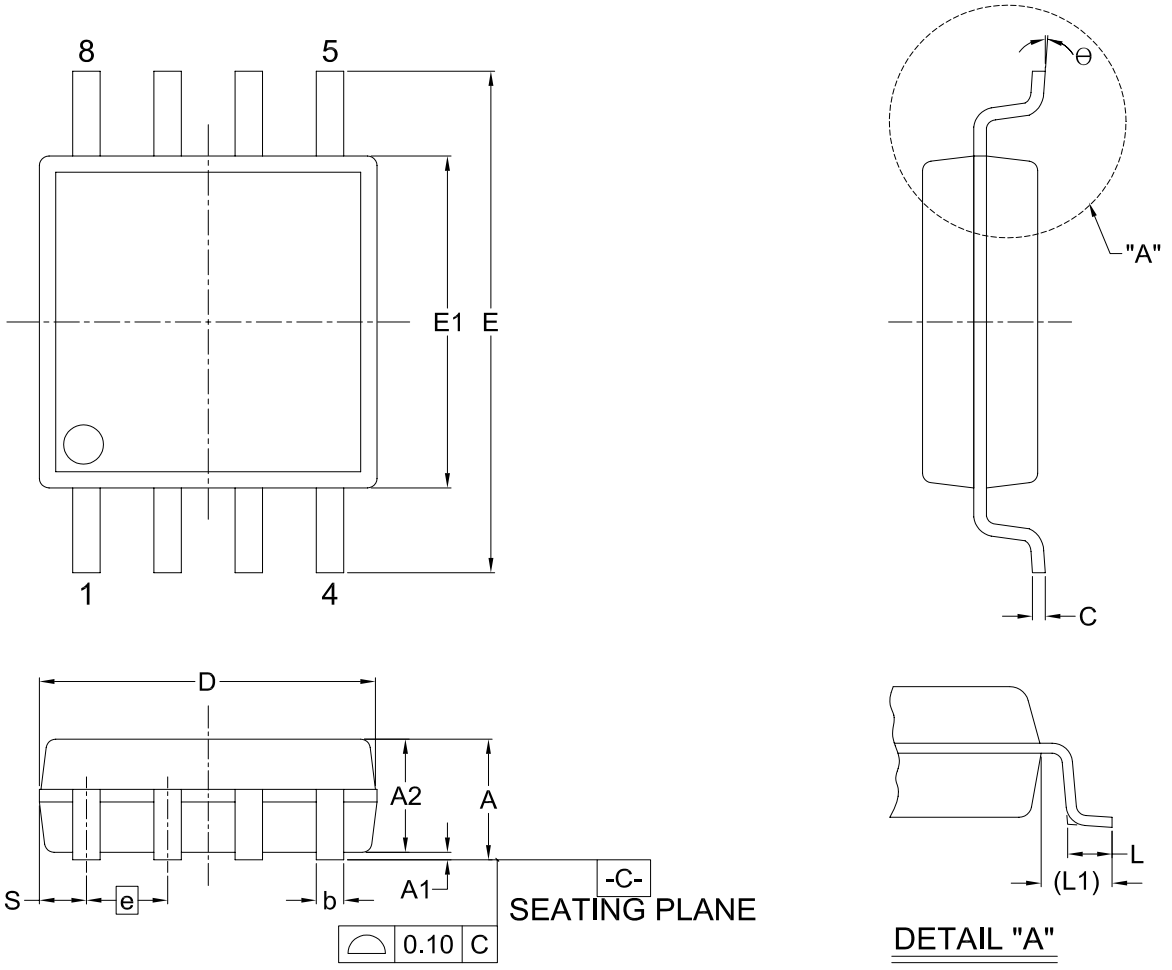


Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	C	D	E	E1	e	L	L1	S	θ
mm	Min.	---	0.10	1.35	0.36	0.15	4.77	5.80	3.80	—	0.46	0.85	0.41	0°
	Nom.	---	0.15	1.45	0.41	0.20	4.90	5.99	3.90	1.27	0.66	1.05	0.54	5°
	Max.	1.75	0.20	1.55	0.51	0.25	5.03	6.20	4.00	—	0.86	1.25	0.67	8°
Inch	Min.	---	0.004	0.053	0.014	0.006	0.188	0.228	0.150	—	0.018	0.033	0.016	0°
	Nom.	—	0.006	0.057	0.016	0.008	0.193	0.236	0.154	0.050	0.026	0.041	0.021	5°
	Max.	0.069	0.008	0.061	0.020	0.010	0.198	0.244	0.158	—	0.034	0.049	0.026	8°

18-2. 8-pin SOP (200mil)

Doc. Title: Package Outline for SOP 8L 200MIL



Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	C	D	E	E1	e	L	L1	S	θ
mm	Min.	1.75	0.05	1.70	0.36	0.19	5.13	7.70	5.18	—	0.50	1.21	0.62	0°
	Nom.	1.95	0.15	1.80	0.41	0.20	5.23	7.90	5.28	1.27	0.65	1.31	0.74	5°
	Max.	2.16	0.20	1.91	0.51	0.25	5.33	8.10	5.38	—	0.80	1.41	0.88	8°
Inch	Min.	0.069	0.002	0.067	0.014	0.007	0.202	0.303	0.204	—	0.020	0.048	0.024	0°
	Nom.	0.077	0.006	0.071	0.016	0.008	0.206	0.311	0.208	0.050	0.026	0.052	0.029	5°
	Max.	0.085	0.008	0.075	0.020	0.010	0.210	0.319	0.212	—	0.031	0.056	0.035	8°

19. REVISION HISTORY

Revision	Descriptions	Page
November 19, 2019		
0.00	Initial Release	ALL
November 27, 2019		
0.01	Part Number changed to KH25V80066M1I02/M2I02 (Option Code 2 = 2)	P56-57
January 09, 2020		
0.02	1. Modified Dummy Cycle for Table 4. Command Set - Read SFDP command	P13
	2. Modified VCC to 2.3-3.6 for Block Erase Cycle Time (32KB) in ERASE AND PROGRAMMING PERFORMANCE table	P54
June 24, 2020		
1.0	1. Removed "Advanced Information" to align with the product status	ALL
	2. Modified ISB1, ISB2, tDVCH, tBP, tPP, tSE, tBE32K, tBE and tCE values	P48,49,50,54
	3. Corrected "Read Electronic Signature (RES) Sequence"	P37
November 04, 2020		
1.1	1. Corrected Serial Input Timing & Read Electronic Signature (RES) Sequence	P12,17
	2. Content correction	P4
	3. Corrected VCC range of tREADY2	P50
February 03, 2021		
1.2	1. Modified Byte Program Time (Max.) values	P50,54
September 30, 2021		
1.3	1. Modified WRSR description and *"Figure 12. Write Status Register (WRSR) Sequence"*	P24
	2. Added "Support Unique ID" description	P4

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