

Features

- Input Voltage Range: 2.5 V to 5.5 V
- Output Voltage Options:
 - ◆ Fixed Voltage: 1.2 V, 1.5V, 1.8 V, 2.5 V, 2.8 V, 3 V, and 3.3 V
 - ◆ Adjustable Voltage: 0.8 V to 5 V
- $\pm 2\%$ Output Accuracy Through Operating Conditions
- Maximum Output Current: 500 mA
- Low Dropout Voltage: 500 mV Max at 500 mA
- Low Quiescent Current and Shutdown Current
- Foldback Current Limit and Thermal Protection
- Stable with 2.2 μF Ceramic Capacitor
- Soft-start Limits Input Current Surge During Enable
- Thermal Shutdown Protection
- Junction Temperature Range: -40°C to $+125^{\circ}\text{C}$
- SOT23-5 Package

Applications

- Handheld Devices with Battery Power Supply
- Video Surveillance
- Wireless and IoT modules

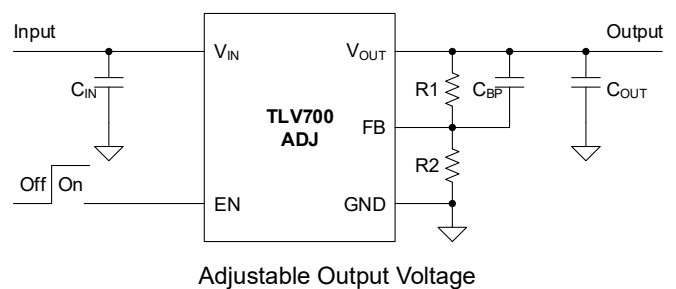
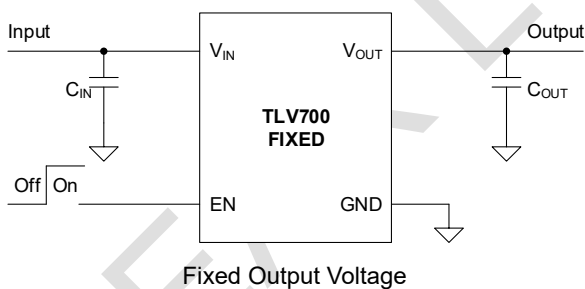
Description

The TLV700 series products are high performance and low dropout linear regulators. The TLV700 series products support maximum 500 mA output current with low quiescent current and high PSRR. The TLV700 series products is stable with ceramic output capacitor from 2.2 μF to 10 μF .

The TLV700 series products have a high PSRR with 60 dB at 1 KHz. This feature makes TLV700 series products very suitable for power-sensitive applications with high noise from previous stage power supply. As low as 50 μA quiescent current and shutdown current makes the TLV700 series products ideal choices for portable devices with battery power supply. Current-limit foldback and thermal overload protection circuits improves the reliability under heavy load conditions.

The TLV700 series products provide several output voltage version options including fixed version and adjustable version with $\pm 2\%$ output voltage accuracy over operating conditions. The TLV700 series products are guaranteed over operating temperature range from -40°C to $+85^{\circ}\text{C}$.

Typical Application Schematic



Product Family Table

Part Number	Output Voltage	Order Number	Package	Transport Media, Quantity	MSL	Marking Information
TLV700ADJ	Adjustable (0.8 V ~ 5 V)	TLV700ADJ-C5TR	SOT23-5	Tape and Reel, 3,000	L3	L6A
TLV700F12	Fixed 1.2 V	TLV700F12-C5TR	SOT23-5	Tape and Reel, 3,000	L3	L6D
TLV700F15	Fixed 1.5 V	TLV700F15-C5TR	SOT23-5	Tape and Reel, 3,000	L3	L6K
TLV700F18	Fixed 1.8 V	TLV700F18-C5TR	SOT23-5	Tape and Reel, 3,000	L3	L6F
TLV700F25	Fixed 2.5 V	TLV700F25-C5TR	SOT23-5	Tape and Reel, 3,000	L3	L6G
TLV700F28	Fixed 2.8 V	TLV700F28-C5TR	SOT23-5	Tape and Reel, 3,000	L3	L6H
TLV700F30	Fixed 3.0 V	TLV700F30-C5TR	SOT23-5	Tape and Reel, 3,000	L3	L6I
TLV700F33	Fixed 3.3 V	TLV700F33-C5TR	SOT23-5	Tape and Reel, 3,000	L3	L6J

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Revision History

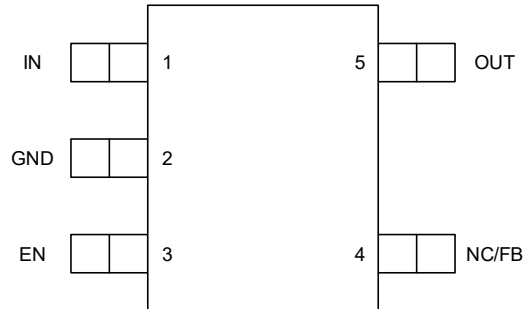
Date	Revision	Notes
2019/01/01	Rev.A.0	Initial Release
2019/06/30	Rev.A.1	Added 1.5 V output voltage option
2020/08/15	Rev.A.2	Added description of "Short-Circuit Protection"
2023/04/15	Rev.A.3	Upgraded Output Current to 500 mA

Pin Configuration and Functions

TLV700 Series

5-Pin SOT23 Package

Top View



Pin Functions

Name	Pin Number	I/O	Description
IN	1	I	Input voltage pin. Bypass IN to GND with a 1 μ F or greater capacitor.
OUT	5	O	Regulated output voltage pin. Bypass OUT to GND with a 2.2 μ F or greater capacitor.
EN	3	I	Regulator enable pin. Drive EN high to turn on the regulator; drive EN low to turn off the regulator. For automatic startup, connect EN to IN directly.
GND	2	–	Ground reference pin. Connect GND pin to PCB ground plane directly.
NC	4	–	No connection.
FB	4	I	Output feedback pin (Adjustable version only). Connect to a resistor divider to adjust the output voltage.

Note: Thermal pad must be connected to PCB ground plane to maximum the thermal performance.

Specifications

Absolute Maximum Ratings

Parameters		Min	Max	Unit
V_{IN}, V_{EN}	Input Voltage	-0.3	6	V
V_{OUT}	Output Voltage	-0.3	6	V
V_{FB}	Feedback Voltage (Adjustable version only)	-0.3	6	V
T_J	Junction Temperature Range	-40	150	°C
T_{STG}	Storage Temperature Range	-65	150	°C
T_L	Lead Temperature (Soldering 10 sec)		260	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

(2) All voltage values are with respect to GND.

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001	±8	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002	±2	kV

Recommended Operating Conditions

Parameters		Min	Max	Unit
V_{IN}	Input Voltage	2.5	5.5	V
V_{EN}	Enable Voltage	0	V_{IN}	V
V_{OUT}	Output Voltage	0	5	V
V_{FB}	Feedback Voltage (Adjustable version only)	0	V_{OUT}	V
I_{OUT}	Output Current	0	500	mA
T_J	Junction Temperature Range	-40	125	°C

Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
SOT23-5	280	62	°C/W

Electrical Characteristics

All test condition: $V_{IN} = V_{OUT(NOM)} + 0.5V$ or $2.5V$, whichever is greater; $C_{OUT} = 2.2\mu F$, $T_A = +25^\circ C$, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply Input Voltage and Current						
V _{IN}	Input voltage range		2.5		5.5	V
I _{GND}	Ground pin current	I _{OUT} = 0 mA		50		μA
I _{SHDN}	Shutdown current	EN = GND		1		μA
UVLO	V _{IN} under-voltage lock-out	V _{IN} rising		2		V
		Hysteresis		0.2		V
Enable Input Voltage and Current						
V _{IH(EN)}	EN logic-input high level (enable)		1.2		V _{IN}	V
V _{IL(EN)}	EN logic-input low level (disable)		0		0.4	V
I _{EN}	EN pin leakage current	EN = 5V		1		μA
Regulated Output Voltage and Current						
V _{OUT}	Output voltage accuracy		−2%		2%	
V _{FB}	Feedback pin voltage	ADJ version only		0.8		V
ΔV _{OUT}	Line regulation	V _{IN} = V _{OUT(NOM)} + 0.5 V or 2.5V to 5.5 V, I _{OUT} = 1 mA		4	10	mV
	Load regulation	I _{OUT} = 1 mA to 500 mA		25		mV
V _{DO} ⁽¹⁾	Dropout voltage	V _{IN} = 0.98 × V _{OUT(NOM)} , I _{OUT} = 100 mA		80		mV
		V _{IN} = 0.98 × V _{OUT(NOM)} , I _{OUT} = 300 mA		240	300	mV
		V _{IN} = 0.98 × V _{OUT(NOM)} , I _{OUT} = 500 mA		400	500	mV
I _{OUT}	Output current	V _{OUT} in regulation	0		500	mA
I _{CL}	Output current limit	V _{OUT} = 0.9 × V _{OUT(NOM)}	550		1200	mA
PSRR	Power supply rejection ratio	I _{OUT} = 100 mA, f = 1 kHz		60		dB
		I _{OUT} = 100 mA, f = 1 MHz		40		dB
V _N	Output noise voltage	I _{OUT} = 100 mA, BW = 100Hz to 80 kHz		150		μV _{RMS}
t _{STR} ⁽²⁾	Start-up time	I _{OUT} = 500 mA, C _{OUT} = 2.2 μF		150		μs
		I _{OUT} = 500 mA, C _{OUT} = 2.2 μF, C _{BP} = 100 nF		15		ms
Temperature Range						
T _{SD}	Thermal shutdown temperature			170		°C
	Thermal shutdown hysteresis			30		°C

(1) Dropout voltage is the minimum input to output voltage differential needed to maintain regulation at a specified output current. In dropout, the output voltage will be equal to: $V_{IN} - V_{DROPOUT}$.

(2) Start-up time from EN assertion to $0.98 \times V_{OUT(NOM)}$.

Typical Performance Characteristics

All test condition: $V_{IN} = V_{OUT(NOM)} + 0.5V$ or $2.5V$, whichever is greater; $C_{OUT} = 2.2\mu F$, $T_A = +25^\circ C$, unless otherwise noted.

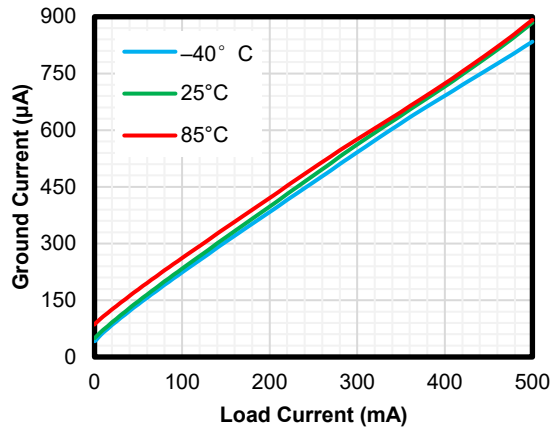


Figure 1 Quiescent Current vs Output Current

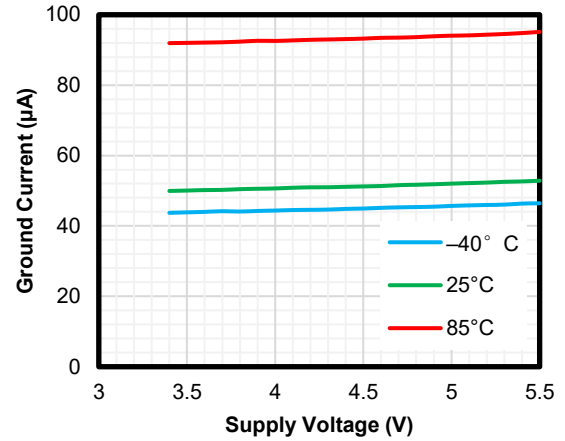


Figure 2 Quiescent Current vs Supply Voltage

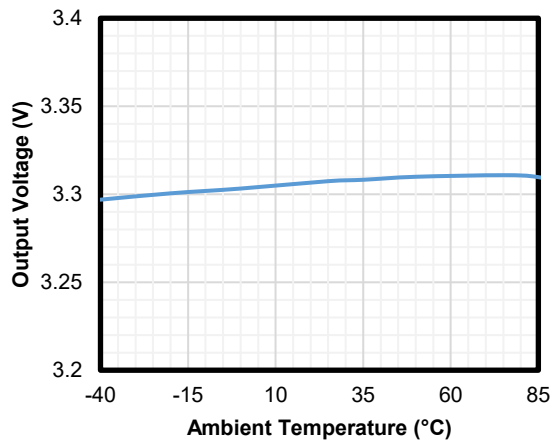


Figure 3 Output Accuracy vs Ambient Temperature

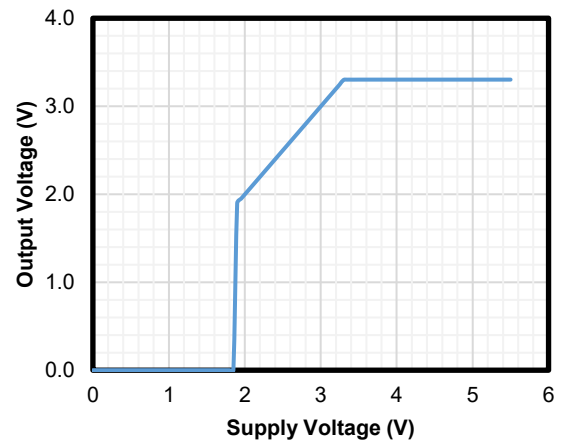


Figure 4 Output Voltage vs Supply Voltage

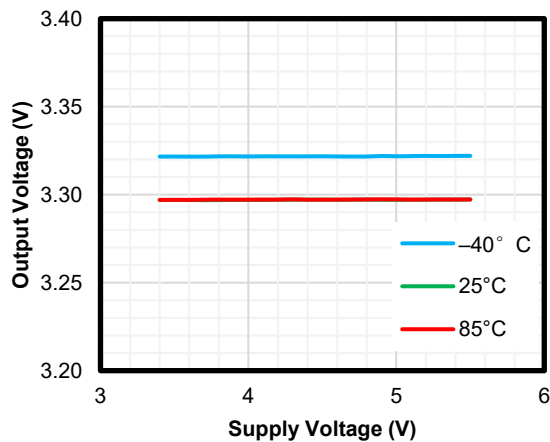


Figure 5. Line Regulation

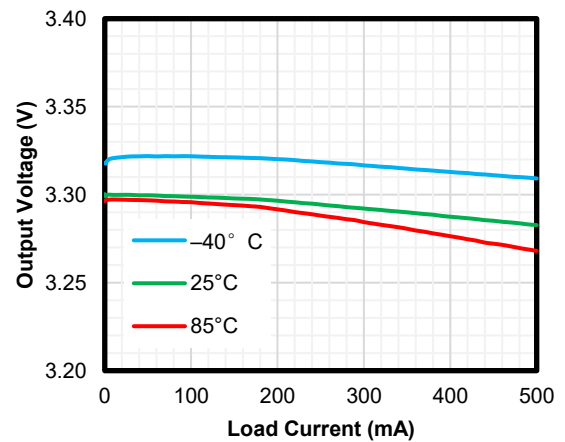


Figure 6. Load Regulation

Typical Performance Characteristics (continued)

Test condition: $V_{IN} = V_{OUT(NOM)} + 0.5V$ or $2.5V$, whichever is greater; $C_{OUT} = 2.2\mu F$, $T_A = +25^\circ C$, unless otherwise noted.

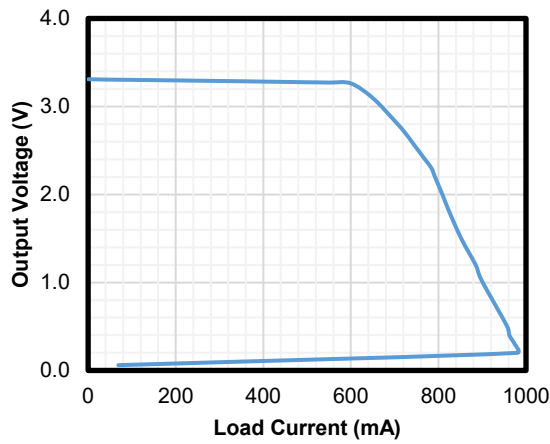


Figure 7. Current Limit

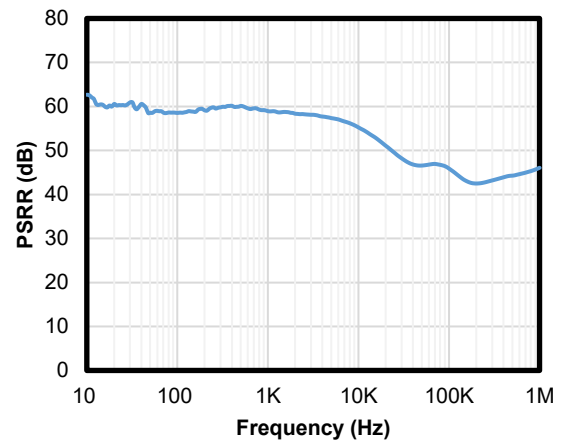


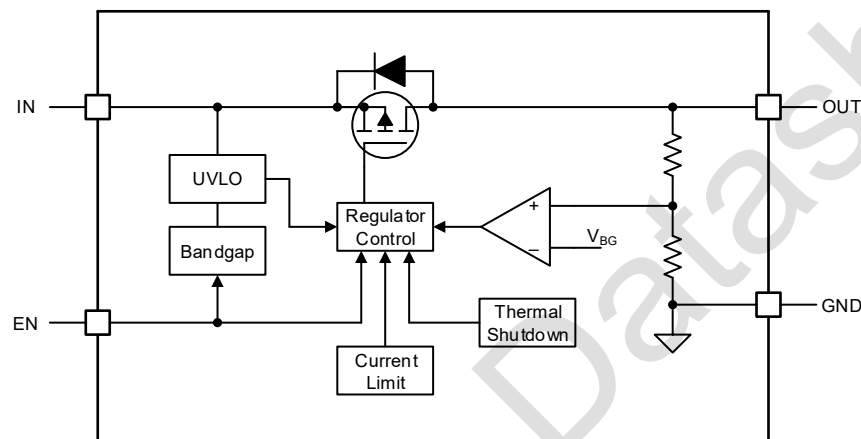
Figure 8. PSRR

Detailed Description

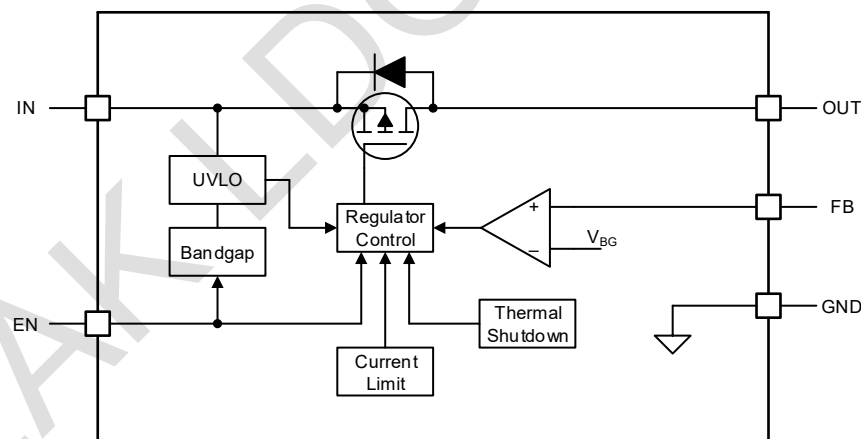
Overview

The TLV700 devices products are 500 mA high PSRR, low-dropout linear regulators with very low quiescent current. These voltage regulators operate from 2.5 V to 5.5 V and consume 50 μ A of quiescent current at no load. The TLV700 series are available in fixed voltage versions of 1.2 V, 1.5 V, 1.8 V, 2.5 V, 2.8 V, 3 V and 3.3 V, and also adjustable voltage version of 0.8 V to 5 V with $\pm 2\%$ output voltage accuracy over operating conditions.

Functional Block Diagram



TLV700 Series Fixed Output Version



TLV700 Series Adjustable Output Version

Feature Description

Enable

The enable pin (EN) is active high. Connect this pin to the GPIO of an external processor or digital logic control circuit to enable and disable the device. Or connect this pin to the IN pin for self-bias applications.

Under-voltage Lockout (UVLO)

The TLV700 series use an under-voltage lockout circuit (UVLO = 2 V) to keep the output shut off until the internal circuitry operates properly.

Regulated Output Voltage

The TLV700 series are available in fixed voltage versions of 1.2 V, 1.5V, 1.8 V, 2.5 V, 2.8 V, 3 V and 3.3 V. When the input voltage is higher than $V_{OUT(NOM)} + V_{DO}$ or 2.5V, output pin is the regulated output based on the selected voltage version. When the input voltage falls below $V_{OUT(NOM)} + V_{DO}$ or 2.5V, output pin tracks the input voltage minus the dropout voltage based on the load current. When the input voltage drops below UVLO threshold, the output keeps shut off.

Adjustable Output Voltage

The TLV700 series are also available in adjustable voltage versions of 0.8 V to 5 V by selecting suitable external resistor dividers. Use [Equation 1](#) to calculate the output voltage ($V_{FB} = 0.8$ V). Suggest select resistor value of ($R1 + R2$) between 10 k Ω and 100 k Ω .

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R1}{R2} \right) \quad (1)$$

Current Limit

The TLV700 series integrate an internal foldback current limit that helps to protect the regulator during fault conditions. Output voltage is not regulated when the device is in current limit mode, and V_{OUT} equals to $I_{CL} \times R_{LOAD}$.

Short-Circuit Protection

The TLV700 series integrate a short-circuit protection. When the output pin is shorted to ground or forced to a voltage below 0.2V, the output current of the TLV700 series is limited to a typical value of 150 mA.

Thermal Shutdown

During normal operation, LDO junction temperature should not exceed 125°C. When the junction temperature exceeds the thermal shutdown threshold, the LDO shut down the output immediately. Until when the junction temperature falls below the thermal shutdown threshold minus thermal shutdown hysteresis, the output turns on again.

Application and Implementation

NOTE

Information in the following applications sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

The TLV700 devices are a series of 500 mA high PSRR, low-dropout linear regulator with low quiescent current. The following application schematic shows a typical usage of the TLV700 series.

Typical Application

Figure 9 and Figure 10 show the typical application schematic of the TLV700 series.

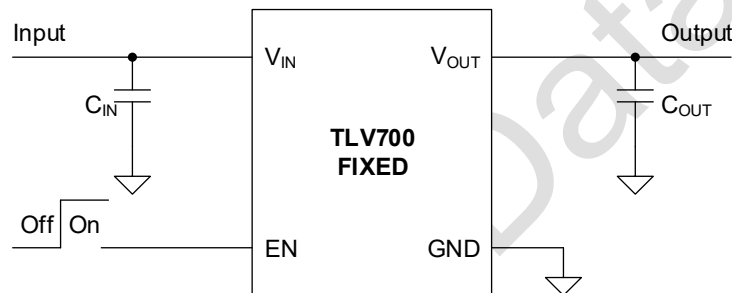


Figure 9 TLV700 Fixed Output Voltage

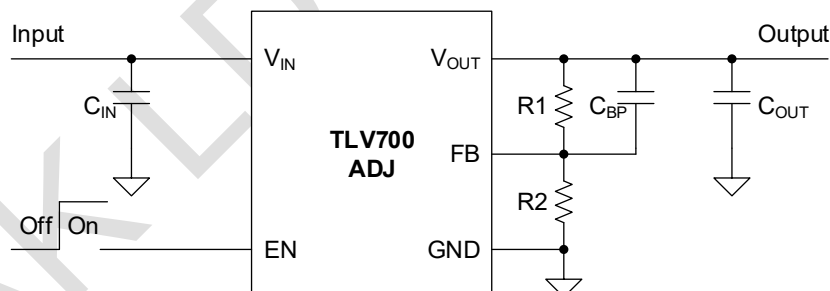


Figure 10 TLV700 Adjustable Output Voltage

Input Capacitor and Output Capacitor

3PEAK recommends adding a 1 μF or greater capacitor with a 0.1 μF bypass capacitor in parallel at IN pin to keep the input voltage stable. The voltage rating of the capacitors must be greater than the maximum input voltage.

To ensure loop stability, the TLV700 series requires an output capacitor with a minimum effective capacitance value of 2.2 μF . 3PEAK recommends selecting a X5R- or X7R-type ceramic capacitor with low ESR over temperature.

Both input capacitors and output capacitors must be placed as close to the device pins as possible.

Power Dissipation

During normal operation, LDO junction temperature should not exceed 125°C. Using below equations to calculate the power dissipation and estimate the junction temperature.

The power dissipation can be calculated using [Equation 2](#).

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_{GND} \quad (2)$$

The junction temperature can be estimated using [Equation 3](#). θ_{JA} is the junction-to-ambient thermal resistance (See Section [Thermal Information](#)).

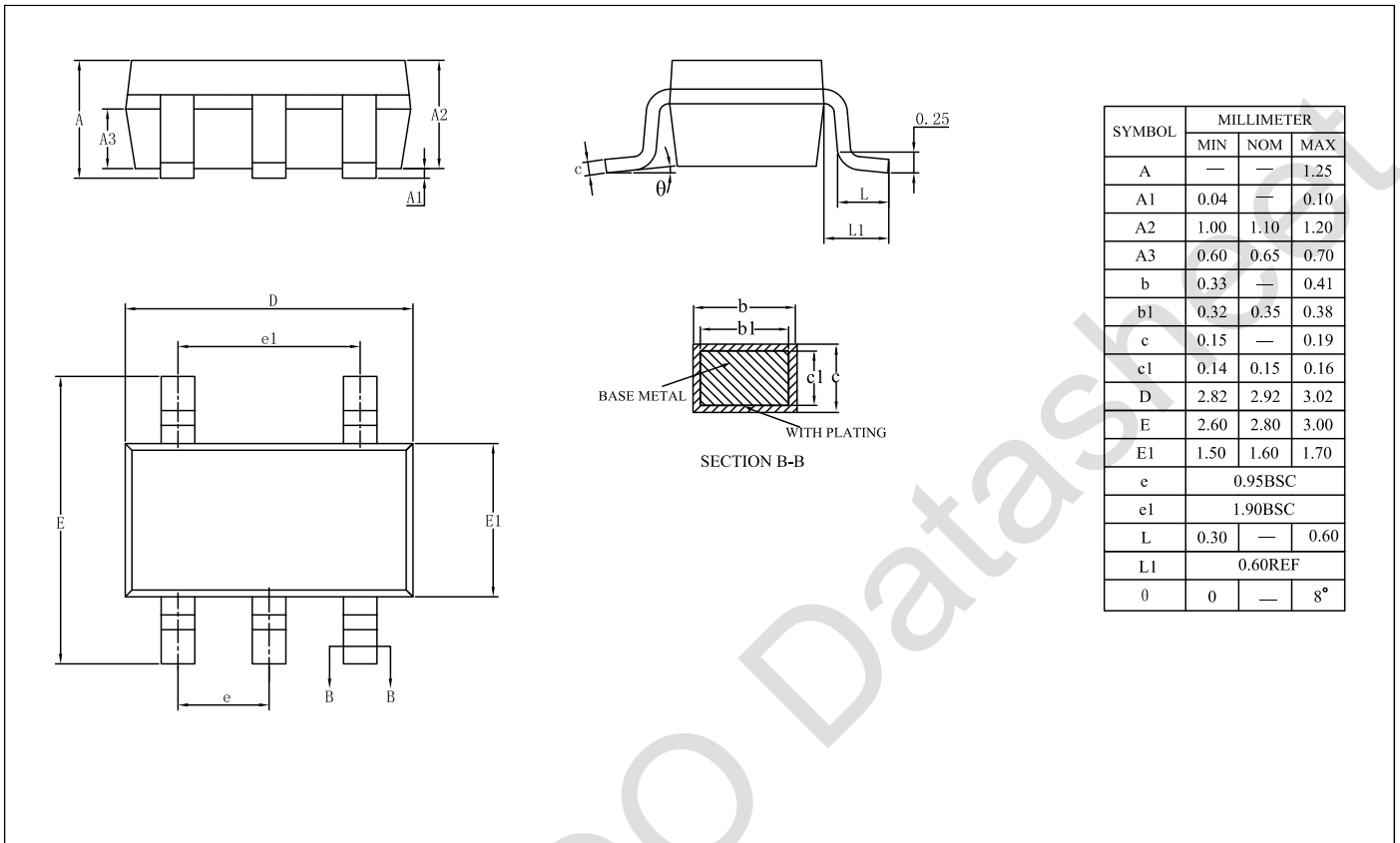
$$T_J = T_A + P_D \times \theta_{JA} \quad (3)$$

Layout Requirements

- Both input capacitors and output capacitors must be placed as close to the device pins as possible.
- It is recommended to bypass the input pin to ground with a 0.1 μ F bypass capacitor. The loop area formed by the bypass capacitor connection, IN pin and the GND pin of the system must be as small as possible.
- It is recommended to use wide trace lengths or thick copper weight to minimize $I \times R$ drop and heat dissipation.

Package Outline Dimensions

SOT23-5



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