Intel® 3D NAND Gen 4 (Q4128A) Flash Memory Die

Datasheet

Features

- Open NAND Flash Interface (ONFI) 4.1-compliant
- ONFI 4.1 I/O performance[1]
  - Up to ONFI 4.0 timing mode 12
  - Clock rate: 1.67ns
  - Read/write throughput per pin: 1.2GT/s
- Operating Voltage Range
  - V_{CC}: 2.35–3.6V
  - V_{CCQ}: 1.14–1.26V
- Command set: ONFI NAND Flash Protocol
- Advanced command set:
  - Page cache program
  - Read cache (Random, Sequential, End)
  - Read unique ID
  - Multi-LUN operations
  - Multi-plane commands
- First 4 blocks are valid when shipped from factory.
- RESET(FFh) required as first command after power-on
- Operation status byte provides software method for detecting
  - Operation completion
  - Pass/fail condition
  - Write-protect status
- Data strobe (DQS) signals provide a hardware method for synchronizing data DQ in the synchronous interface
- On-die Termination (ODT)
- Operating temperature: 0°C to +70°C

Physical Specifications

- Die size (stepping distance): 10.936mm x 7.404mm
- Maximum die per wafer: 779
- Bond pad location and identification: see Table 2 on page 15 and Table 3 on page 17
- Passivation openings (min): 50 µm x 65 µm
- Wafer diameter: 300 mm
- Nominal wafer thickness: 775 µm ± 10 µm (wafer form only)
- Typical bond-pad metal thickness: 7 kÅ
- Typical topside passivation: 35 kÅ polyimide over 8 kÅ nitride over 10 kÅ of TEOS oxide
- Metallization composition: 7kÅ AlCu, 99.5% Al 0.5% Cu alloy

1. ONFI 4.1 functionality is only available with 1.2V V_{CCQ}.

Ordering Information

For devices or wafers not listed in this table, contact your local Intel representative.

I/O Voltage (V)	Product Technology, Wafer	Litho	MM#	Part Number
3.3/1.2	1024 Gb QLC 300 mm wafer	3D Gen 4	99A3FW	X29F01T0T3AQK1 S LNLB
3.3/1.2	1024 Gb QLC 300 mm wafer	3D Gen 4	99A3FT	X29F01T0R3AQK1 S LNL9
3.3/1.2	1024 Gb QLC 300 mm wafer	3D Gen 4	99A67X	X29F01T0W3AQK1 S LNPT
3.3/1.2	1024 Gb QLC 300 mm wafer	3D Gen 4	99AF5Z	X29F01T0C3AQK1 S LNW5
3.3/1.2	1024 Gb QLC 300 mm wafer	3D Gen 4	99AF5L	X29F01T0U3AQK1 S LNVW
3.3/1.2	1024 Gb QLC 300 mm wafer	3D Gen 4	99AF5M	X29F01T0D3AQK1 S LNVX

Table 1: Revision Table

Revision Number	Description	Date
001	Initial documentation.	March 2020
002	Updated Part Number.	August 2020
003	Updated Part Number. Added TLC Device ID.	February 2021

Contents

Figures

Tables

1 Functional Specifications

The specifications in this die datasheet are provided for reference only. For functional and parametric specifications, see the packaged product datasheet for the Intel® 3D NAND Gen 4 (Q4128A) NAND Flash Memory device. This datasheet is available to customers under non-disclosure agreement (NDA). To obtain a copy, contact your local Intel field representative.

2 Die Testing Procedures

Intel die products are tested at a standard wafer test level. Wafer probe is performed at an elevated temperature to ensure product functionality in Intel standard packages. The package environment is not within the control of Intel; therefore, the user must determine the necessary heat sink requirements to ensure that the die junction temperature remains within specified limits.

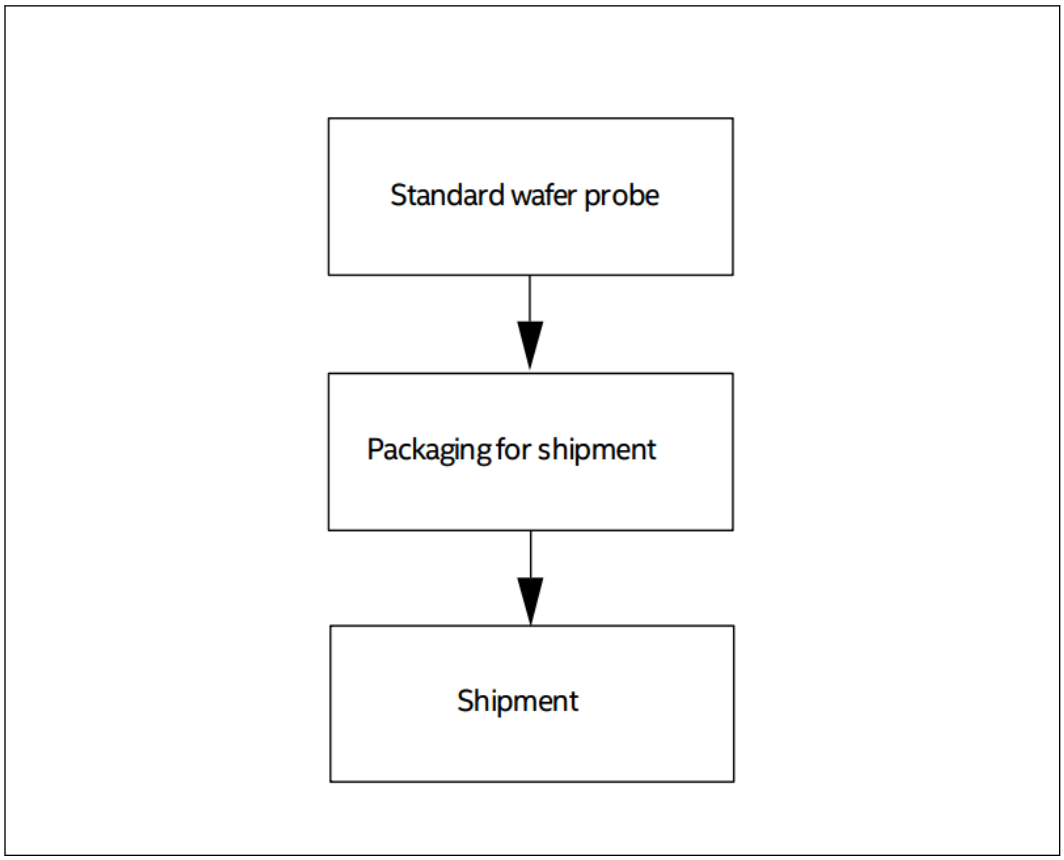
3 Wafer-Level Testing

The standard probe flow is the same probe flow used for Intel packaged products. The following list provides an example of a standard probe test performed at wafer-level for Intel wafer sales products:

- Opens/shorts
- Input/output leakage tests
- I_{CC} standby
- Voltage regulator performance
- Nominal V_{CC} functional
- Memory array algorithmic patterns
- High voltage stress
- PROGRAM performance
- ERASE performance
- Bad block marking

Repairs are implemented at each repair test. Repairable die are processed through repair algorithms based on the repair solutions defined during the tests described above. Post-repair testing is conducted with appropriate guard bands to ensure a consistently high quality level.

Figure 1: Standard Probe Flow



Intel retains a wafer map of each wafer as part of the probe records, along with a lot summary of wafer yields for each lot probed.

Intel reserves the right to change the probe program at any time to improve the reliability, packaged device yield, or performance of the product. Die users might experience differences in performance relative to Intel datasheet specifications due to differences in package capacitance, inductance, resistance, and trace length.

4 Bonding Instructions

The Intel® 3D NAND Gen 4 (Q4128A) Flash Memory Die has 61 bond pads. See Die Bond Pad Location from Pad 1 Center for Synchronous Operations for a complete list of bond pads and coordinates from bond pad 1 center, and Bond Pad Location from Die Center for Synchronous Operations for bond pad locations from center of die.

The back side of the die is at Vss potential. For improved thermal performance, Intel recommends that the die be connected to the ground plane. It is also possible to leave the back side of the die unconnected.

5 Wafer-Level Processing

Intel provides full-thickness wafers to accommodate post-processing, which might include adding extra passivation or metal layers or bumping bond pads.

6 Storage Requirements

Intel® 3D NAND Gen 4 (Q4128A) Flash Memory devices are packaged for shipping in a clean room environment. Upon receipt, the customer should transfer the die or wafers to a similar environment for storage.

Intel also recommends that the die or wafers be maintained in a filtered nitrogen atmosphere until removed for assembly. The moisture content of the storage facility should be maintained at 30 percent relative humidity (±10 percent). Precautions for avoiding ESD damage are necessary during handling. The die must be in an ESD-protected environment for inspection and assembly at all times.

WARNING: Intel advises customers to avoid exposing flash die devices to ultraviolet light, or processing them at temperatures greater than 250°C for more than five minutes. Failure to adhere to these handling instructions will result in irreparable damage to the devices.

7 Product Reliability Monitors

The Intel Quality Department continually samples product families for reliability studies. These samples are subjected to a battery of tests known as “accelerated life and environmental stress tests.” During these tests, devices are stressed for many hours under conditions designed to simulate years of normal field use. A summary of these product-family evaluations is published on a regular basis and is available upon request.

8 Die-Level Reliability and Screening

Extensive Intel qualification of both the die and its manufacturing process shows that production burn-in is not required to ensure a high level of reliability on flash products. Additional information is available upon request.

9 Bond Pad Locations and Identification

Bond pad locations are provided from the center of pad 1, located in the upper left corner of the die, and from the center of the die.

Table 2: Die Bond Pad Location from Pad 1 Center for Synchronous Operations

Pad #	Pad Name	Coordinates from Center of Pad 1 (0,0)		Notes
		X (µm)[1]	Y (µm)[1]	
1	V_{SS}	0	0	
2	V_{SS}	8121.1260	0	
3	WP#	8013.6260	0	
4	ALE	7874.8760	0	
5	Dummy	7784.8760	0	
6	CLE	7694.8760	0	
7	Dummy	7604.8760	0	
8	V_{CC}	7514.8760	0	
9	V_{SS}	7206.8760	0	
10	V_{CCQ}	6989.3310	0	
11	V_{SS}	6871.7685	0	
12	DQ0	6744.5960	0	
13	DQ1	6522.9410	0	
14	V_{CCQ}	6395.7685	0	
15	V_{SS}	6235.7685	0	
16	DQ2	6108.5960	0	
17	DQ3	5886.9410	0	
18	V_{CCQ}	5759.7685	0	
19	V_{SS}	5667.2670	0	
20	DQS_c	5540.0945	0	
21	DQS (DQS_t)	5318.4395	0	
22	V_{CCQ}	5191.2670	0	
23	RE_c	5064.0960	0	
24	RE# (RE_t)	4842.4410	0	
25	V_{SS}	4715.2685	0	
26	V_{CCQ}	4622.7685	0	
27	DQ4	4495.5960	0	

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Pad #	Pad Name	Coordinates from Center of Pad 1 (0,0)		Notes
		X (µm)[1]	Y (µm)[1]	
28	DQ5	4273.9410	0	
29	V_{SS}	4146.7685	0	
30	V_{CCQ}	3986.8070	0	
31	DQ6	3859.6345	0	
32	DQ7	3637.9795	0	
33	V_{SS}	3510.8070	0	
34	V_{CCQ}	3381.0250	0	
35	Dummy	3283.5250	0	
36	WE#	3193.5250	0	
37	Dummy	3103.5250	0	
38	CE#	3013.5250	0	
39	Dummy	2923.5250	0	
40	Dummy	2833.5250	0	
41	Dummy	2743.5250	0	
42	RB#	2636.0250	0	
43	V_{CC}	2510.7500	0	
44	V_{SS}	2172.5000	0	
45	V_{CCQ}	2082.5000	0	
46	V_{REFQ}	1970.0000	0	
47	V_{SS}	1847.4990	0	
48	ZQ	1687.5000	0	
49	V_{CCQ}	1517.5000	0	
50	ENi	1427.5000	0	
51	ENo	1332.5000	0	
52	MDS0	1237.5000	0	3
53	MDS1	1142.5000	0	3
54	MDS2	1047.5000	0	3
55	MDS3	952.5000	0	3
56	V_{SS}	855.0000	0	
57	DNU	725.0000	0	2
58	DNU	574.7750	0	2
59	V_{PP}	372.5000	0	
60	DNU	228.7500	0	2
61	DNU	105.0000	0	2

Notes:

1. Reference is to the center of each bond pad from the center of Pad 1.
2. DNU = do not use.
3. See Multi-Die Stack Configuration per CE# for bonding configuration.

Table 3: Bond Pad Location from Die Center for Synchronous Operations

Pad #	Pad Name	Coordinates from Center of Die Center (0,0)		Notes
		X (µm)[1]	Y (µm)[1]	
1	V_{SS}	-5319.4995	-3555.9375	
2	V_{SS}	2801.6265	-3555.9375	
3	WP#	2694.1265	-3555.9375	
4	ALE	2555.3765	-3555.9375	
5	Dummy	2465.3765	-3555.9375	
6	CLE	2375.3765	-3555.9375	
7	Dummy	2285.3765	-3555.9375	
8	V_{CC}	2195.3765	-3555.9375	
9	V_{SS}	1887.3765	-3555.9375	
10	V_{CCQ}	1669.8315	-3555.9375	
11	V_{SS}	1552.2690	-3555.9375	
12	DQ0	1425.0965	-3555.9375	
13	DQ1	1203.4415	-3555.9375	
14	V_{CCQ}	1076.2690	-3555.9375	
15	V_{SS}	916.2690	-3555.9375	
16	DQ2	789.0965	-3555.9375	
17	DQ3	567.4415	-3555.9375	
18	V_{CCQ}	440.2690	-3555.9375	
19	V_{SS}	347.7675	-3555.9375	
20	DQS_c	220.5950	-3555.9375	
21	DQS (DQS_t)	-1.0600	-3555.9375	
22	V_{CCQ}	-128.2325	-3555.9375	
23	RE_c	-255.4035	-3555.9375	
24	RE# (RE_t)	-477.0585	-3555.9375	
25	V_{SS}	-604.2310	-3555.9375	
26	V_{CCQ}	-696.7310	-3555.9375	
27	DQ4	-823.9035	-3555.9375	
28	DQ5	-1045.5585	-3555.9375	
29	V_{SS}	-1172.7310	-3555.9375	

continued...

Pad #	Pad Name	Coordinates from Center of Die Center (0,0)		Notes
		X (µm)[1]	Y (µm)[1]	
30	V_{CCQ}	-1332.6925	-3555.9375	
31	DQ6	-1459.8650	-3555.9375	
32	DQ7	-1681.5200	-3555.9375	
33	V_{SS}	-1808.6925	-3555.9375	
34	V_{CCQ}	-1938.4745	-3555.9375	
35	Dummy	-2035.9745	-3555.9375	
36	WE#	-2125.9745	-3555.9375	
37	Dummy	-2215.9745	-3555.9375	
38	CE#	-2305.9745	-3555.9375	
39	Dummy	-2395.9745	-3555.9375	
40	Dummy	-2485.9745	-3555.9375	
41	Dummy	-2575.9745	-3555.9375	
42	RB#	-2683.4745	-3555.9375	
43	V_{CC}	-2808.7495	-3555.9375	
44	V_{SS}	-3146.9995	-3555.9375	
45	V_{CCQ}	-3236.9995	-3555.9375	
46	V_{REFQ}	-3349.4995	-3555.9375	
47	V_{SS}	-3472.0005	-3555.9375	
48	ZQ	-3631.9995	-3555.9375	
49	V_{CCQ}	-3801.9995	-3555.9375	
50	ENi	-3891.9995	-3555.9375	
51	ENo	-3986.9995	-3555.9375	
52	MDS0	-4081.9995	-3555.9375	3
53	MDS1	-4176.9995	-3555.9375	3
54	MDS2	-4271.9995	-3555.9375	3
55	MDS3	-4366.9995	-3555.9375	3
56	V_{SS}	-4464.4995	-3555.9375	
57	DNU	-4594.4995	-3555.9375	2
58	DNU	-4744.7245	-3555.9375	2
59	V_{PP}	-4946.9995	-3555.9375	
60	DNU	-5090.7495	-3555.9375	2
61	DNU	-5214.4995	-3555.9375	2

Notes:

1. Reference is to the center of each bond pad from the center of die.
2. DNU = do not use.
3. See Multi-Die Stack Configuration per CE# for bonding configuration.

10 Multi-Die Stack Configuration per CE#

This Intel product supports a multi-die stack (MDS) configuration for customers building high-density, high-performance devices. For each CE# in an MDS configuration, some of the MDS pads must be bonded to Vss and the LA2, LA1, and LA0 address bits must be used during the address cycle of commands. See the following table for details.

Table 4: MDS Bonding Configurations

Number of Die		CE#	MDS3	MDS2	MDS1	MDS0	LA2	LA1	LA0
Single	Die0	CE#	NU	NU	NU	NU	-	-	-
Dual_A	Die0	CE#	NU	NU	NU	NU	-	-	-
	Die1	CE#2	NU	NU	NU	NU	-	-	-
Dual_B	Die0	CE#	NU	Vss	NU	NU	-	-	-
	Die1	CE#	NU	Vss	NU	Vss	-	-	1
Quad_A	Die0	CE#	NU	Vss	NU	NU	-	-	0
	Die1	CE#	NU	Vss	NU	Vss	-	-	1
	Die2	CE#2	NU	Vss	NU	NU	-	-	0
	Die3	CE#2	NU	Vss	NU	Vss	-	-	1
Quad_B	Die0	CE#	NU	NU	Vss	NU	-	0	0
	Die1	CE#	NU	NU	Vss	Vss	-	0	1
	Die2	CE#	NU	Vss	Vss	NU	-	1	0
	Die3	CE#	NU	Vss	Vss	Vss	-	1	1
Eight_A	Die0	CE#	NU	NU	NU	NU	0	0	0
	Die1	CE#	NU	NU	NU	Vss	0	0	1
	Die2	CE#	NU	NU	Vss	NU	0	1	0
	Die3	CE#	NU	NU	Vss	Vss	0	1	1
	Die4	CE#	NU	Vss	NU	NU	1	0	0
	Die5	CE#	NU	Vss	NU	Vss	1	0	1
	Die6	CE#	NU	Vss	Vss	NU	1	1	0
	Die7	CE#	NU	Vss	Vss	Vss	1	1	1
Eight_B	Die0	CE#	Vss	Vss	NU	Vss	-	0	0
	Die1	CE#	Vss	Vss	NU	NU	-	0	1
	Die2	CE#	Vss	NU	NU	Vss	-	1	0
	Die3	CE#	Vss	NU	NU	NU	-	1	1
	Die4	CE#2	Vss	Vss	NU	Vss	-	0	0

continued...

Number of Die		CE#	MDS3	MDS2	MDS1	MDS0	LA2	LA1	LA0
	Die5	CE#2	Vss	Vss	NU	NU	-	0	1
	Die6	CE#2	Vss	NU	NU	Vss	-	1	0
	Die7	CE#2	Vss	NU	NU	NU	-	1	1

Note: NU = "Not Used"

11 READ ID for Multi-Die Stack Configurations

The READ ID (90h) command with 00h address reads identifier codes programmed into the device. The following table shows the READ ID parameters for the MDS bonding configurations.

Table 5: READ ID Parameters for Address 00h

DIE per CE	QLC Device ID	TLC Device ID
1	89h, D3h, ACh, 32h, C6h, 00h, 00h, 00h	89h, CBh, 98h, 32h, C6h, 00h, 00h, 00h
2	89h, E3h, ADh, 32h, C6h, 00h, 00h, 00h	89h, DBh, 99h, 32h, C6h, 00h, 00h, 00h
4	89h, F3h, AEh, 32h, C6h, 00h, 00h, 00h	89h, EBh, 9Ah, 32h, C6h, 00h, 00h, 00h
8	89h, 2Bh, AFh, 32h, C6h, 00h, 00h, 00h	89h, FBh, 9Bh, 32h, C6h, 00h, 00h, 00h

Note: h = hexadecimal

12 Bus Configuration for Multi-CE# Systems

When multiple CE#s are used in a system, there are three possible bus configurations (see Single Channel Configuration with Shared R/B#, Single Channel Configuration with Separate R/B# and Multi-Channel Configuration for details).

Each CE# unit can be configured with a single die or multiple die. When using multiple die (see CE# Unit), some MDS pads must be bonded to Vss, as shown in MDS Bonding Configurations.

Figure 2: Single Channel Configuration with Shared R/B#

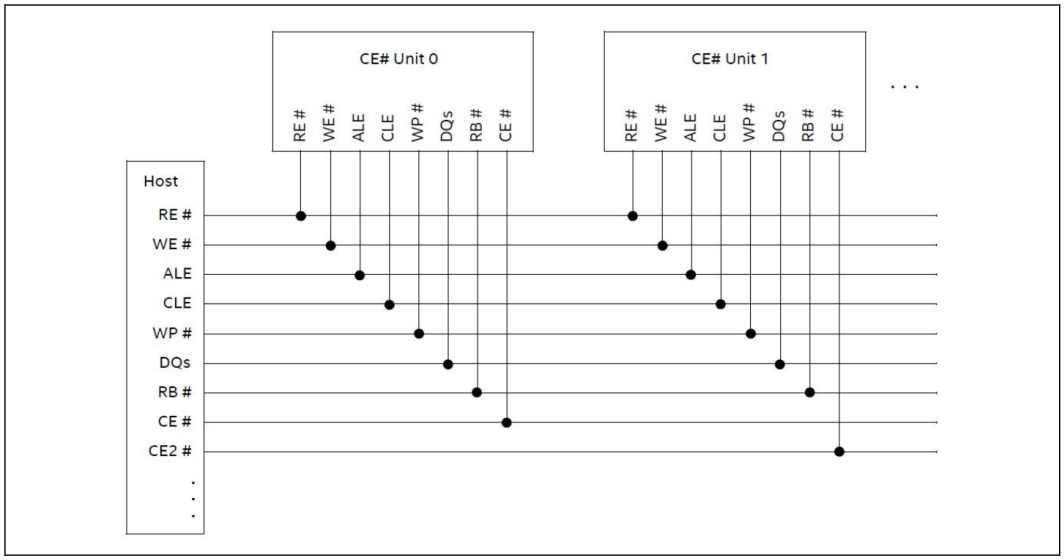


Figure 3: Single Channel Configuration with Separate R/B#

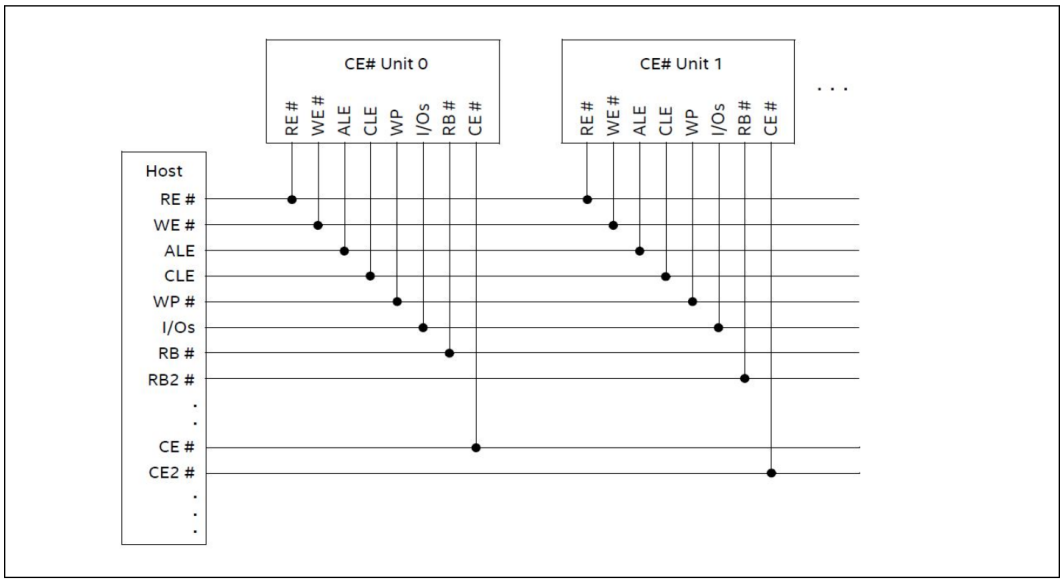


Figure 4: Multi-Channel Configuration

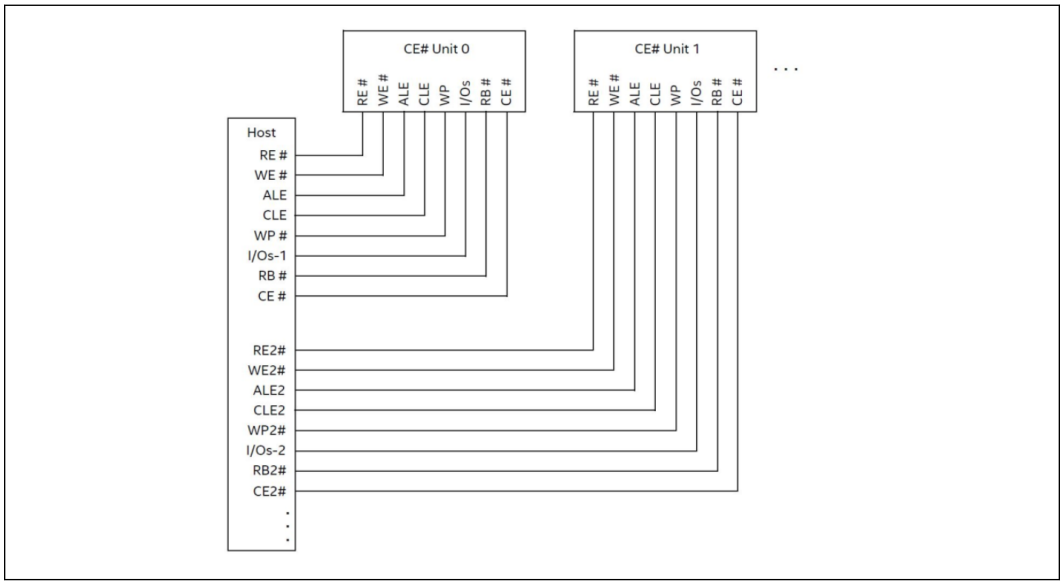
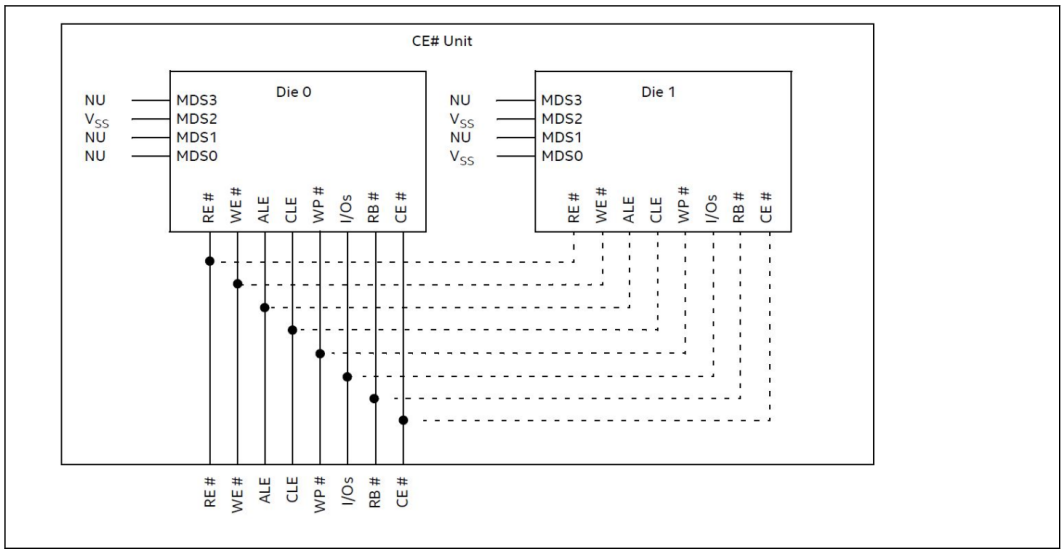


Figure 5: CE# Unit



13 Die Features and Physical Specifications

Table 6: Die Dimensions

Characteristic	Dimensions
Wafer diameter	300 mm
Wafer thickness	775 µm ± 10 µm
Die size (stepping interval)	10.936 mm x 7.404 mm
Street width along X-axis (dsw_X)	90.00 µm
Street width along Y-axis (dsw_Y)	90.00 µm
Bond pad passivation openings (MIN)	50 µm x 65 µm
Minimum bond pad pitch	100 µm