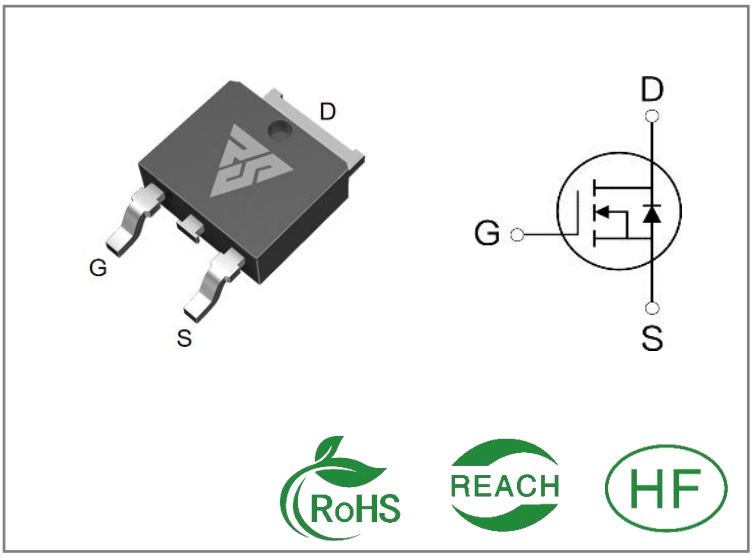
ID	R_{DS}(ON)(Typ)	VDSS
2A	3.8Ω	650V



Applications:

- Switch Mode Power Supply(SMPS)
- Adapter & Charger
- AC-DC Switching Power Supply

Features:

- Fast switching speed
- 100% avalanche tested
- Improved dv/dt capability

Ordering Information

Part Number	Package	Marking	Packing	Qty.
RS2N65D	T0-252	RS2N65D	Tape&reel	2500 PCS

Absolute Maximun Ratings Tc= 2 5℃ unless otherwise specified

Symbol	Parameter	RS2N65D	Units
VDSS	Drain-to-Source Voltage	650	V
ID	Continuous Drain Current TC=25℃	2	A
ID	Continuous Drain Current TC=100℃	1.45	
IDM	Pulsed Drain Current (Note*1)	8	
PD	Power Dissipation	35	W
VGS	Gate- to- Source Voltage	±30	V
EAS	Single Pulse Avalanche Engergy L = 30mH, IAS=2.52A,VDD = 145V, RG = 25 Ω	68	mJ
TL TPKG	Maximum Temperature for Soldering	300	℃
	Leads at 0.063in(1.6mm)from Case for 10 seconds Package Body for 10 seconds	260	
TJ and TSTG	Operating Junction and Storage Temperature Range	-55 to 150	

* Drain Current Limited by Maximum Junction Temperature

Caution: Stresses greater than those listed in the“ Absolute Maximum Ratings” Table may cause permanent damage to the device.

Thermal Resistance

Symbol	Parameter	RS2N65D	Units	Test Conditions
RθJC	Junction-to-Case	3.75	℃/ W	Drain lead soldered to water cooled heatsink, PD adjusted for a peak junction temperature of + 1 5 0 ℃
RθJA	Junction-to-Ambient	62		1 cubic foot chamber,free air.

OFF Characteristics TJ= 25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BVDSS	Drain- to- source Breakdown Voltage	650	--	--	V	VGS=0V,ID=250μA
IDSS	Drain- to- Source Leakage Current	--	--	1	μA	VDS=650V,VGS=0 V
IGSS	Gate- to- Source Forward Leakage	--	--	100	nA	VGS=30V ,VDS=0V
	Gate- to- Source Reverse Leakage	--	--	-100		VGS=-30V ,VDS=0 V

ON Characteristics TJ=25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
RDS(on)	Static Drain- to- Source On-Resistance(Note*2)	--	3.8	4.5	Ω	VGS=10V,ID=1A
VGS(TH)	Gate Threshold Voltage	2	--	4	V	VGS=VDS,ID=250μA

Resistive Switching Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
td(ON)	Turn- on Delay Time	--	7.8	--	nS	VDS=325V ID=2A RG=9.1Ω
trise	Rise Time	--	6	--		
td(OFF)	Turn- OFF Delay Time	--	30	--		
tfall	Fall Time	--	11	--		

Dynamic Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
Ciss	Input Capacitance	--	290	--	pF	VGS=0V VDS=25V f=1.0MHz
Coss	Output Capacitance	--	31	--		
Crss	Reverse Transfer Capacitance	--	6	--		
Qg	Total Gate Charge	--	9	--	nC	VDS=325V ID=2A VGS=10V
Qgs	Gate- to- Source Charge	--	1.5	--		
Qgd	Gate-to-Drain(" Miller") Charge	--	4	--		

Source- Drain Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
IS	Continuous Source Current	--	--	2	A	Integral pn- diode in MOSFET
ISM	Maximum Pulsed Current	--	--	8	A	
VSD	Diode Forward Voltage	--	--	1.5	V	IS=2A,VGS=0V
trr	Reverse Recovery Time	--	425	--	nS	VGS=0V IS=2A,di/dt=100A/μs
Qrr	Reverse Recovery Charge	--	1.2	--	μC	

Notes:

* 1. Repetitive rating, pulse width limited by maximum junction temperature.
* 2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 1%

Typical Feature Curve

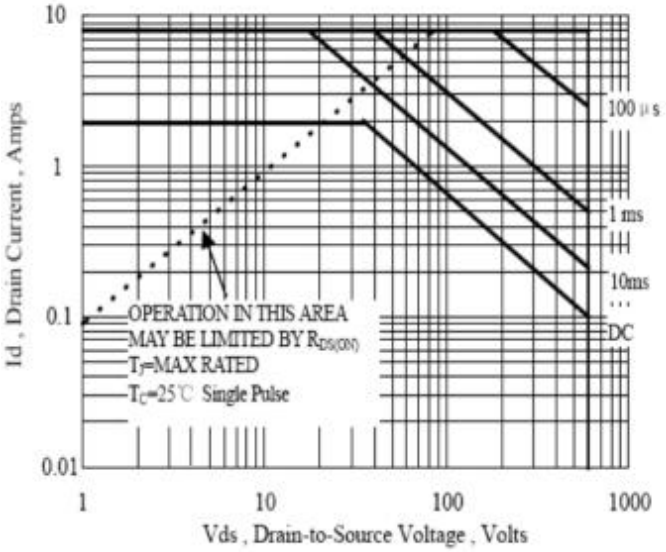


Figure 1 Maximum Forward Bias Safe Operating Area

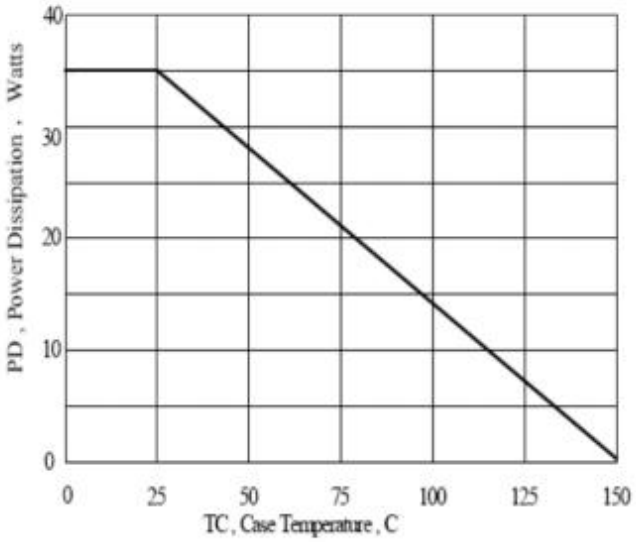


Figure 2 Maximum Power Dissipation vs Case Temperature

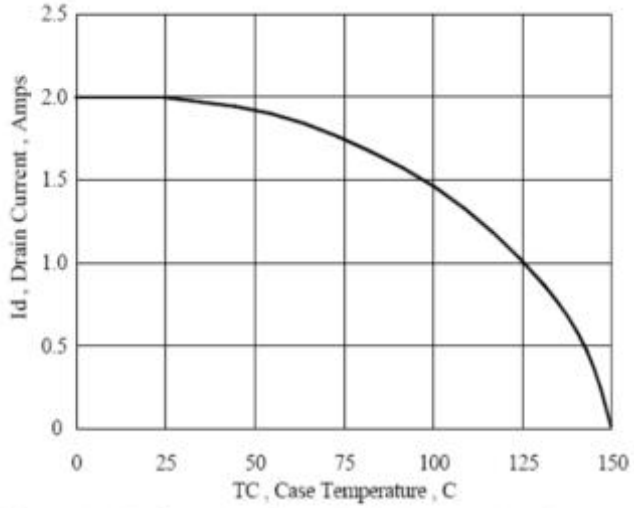


Figure 3 Maximum Continuous Drain Current vs Case Temperature

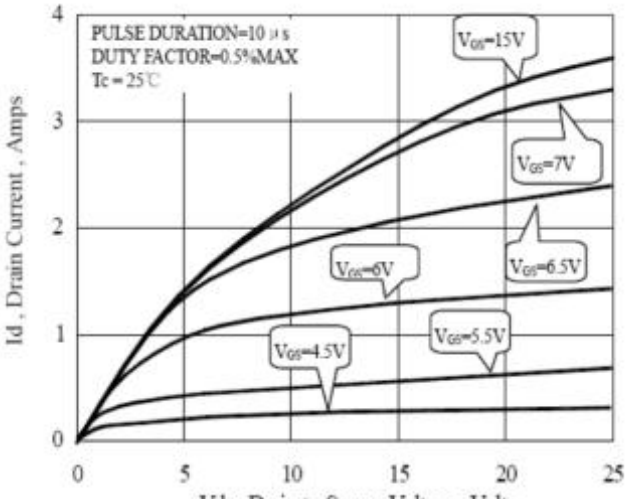


Figure 4 Typical Output Characteristics

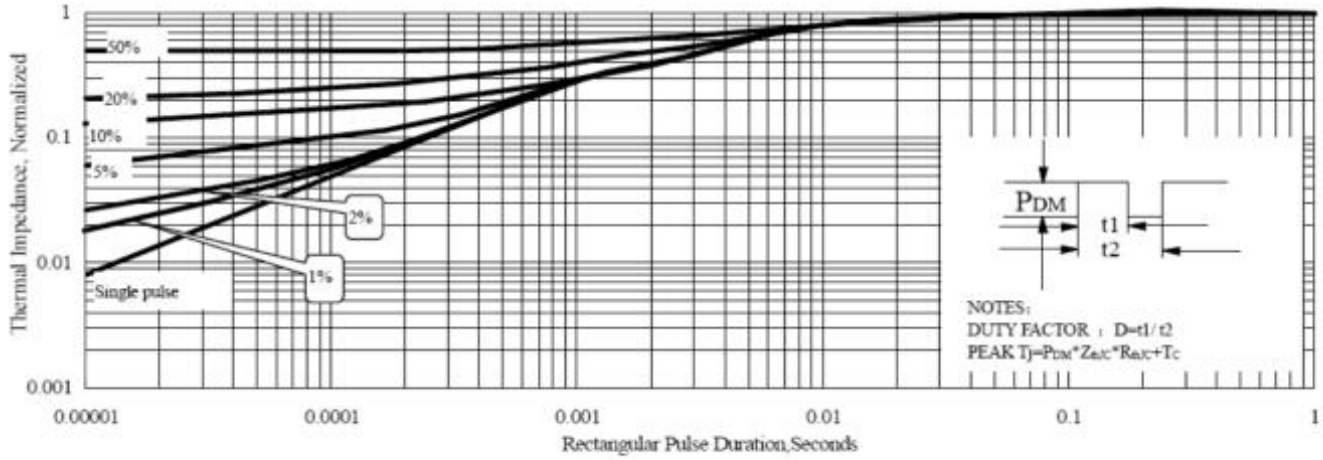


Figure 5 Maximum Effective Thermal Impendance , Junction to Case

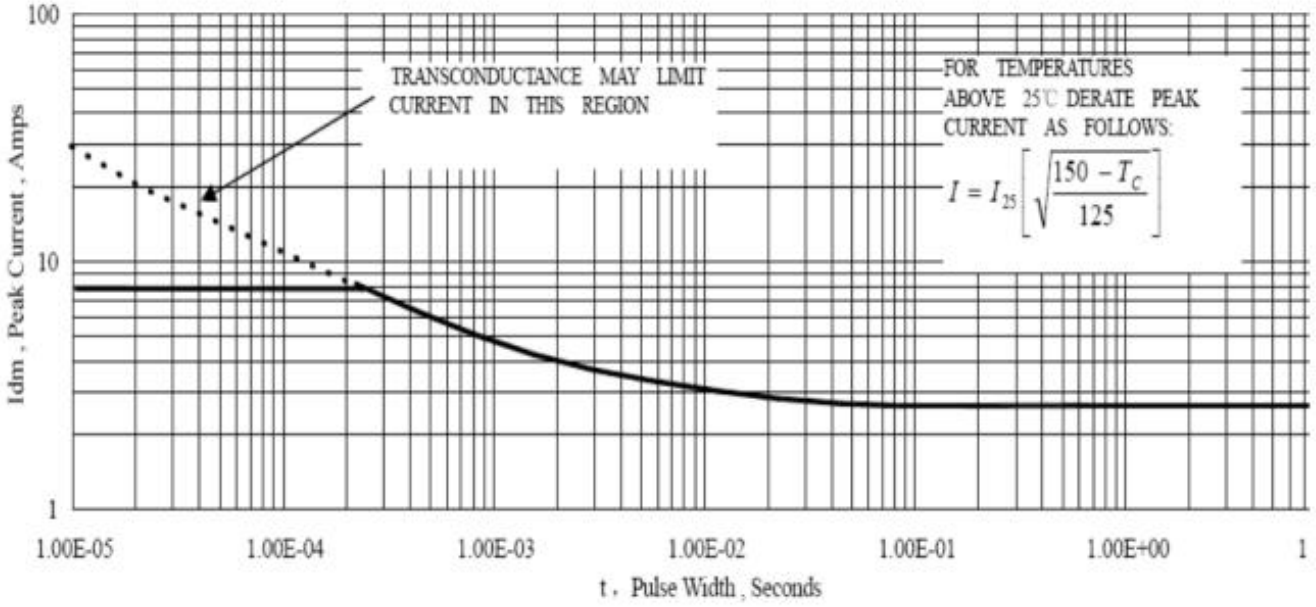


Figure 6 Maximum Peak Current Capability

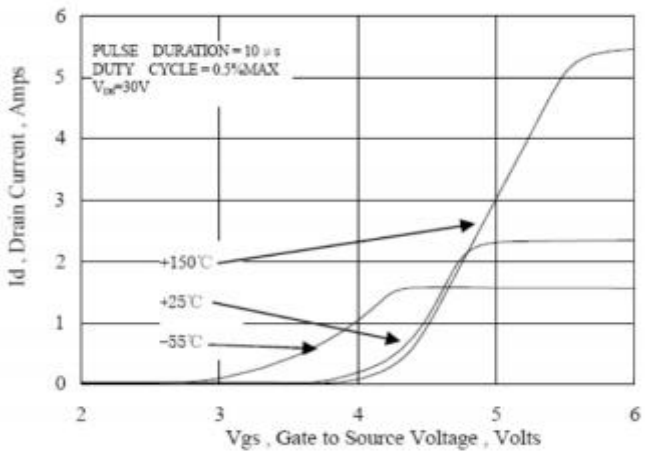


Figure 7 Typical Transfer Characteristics

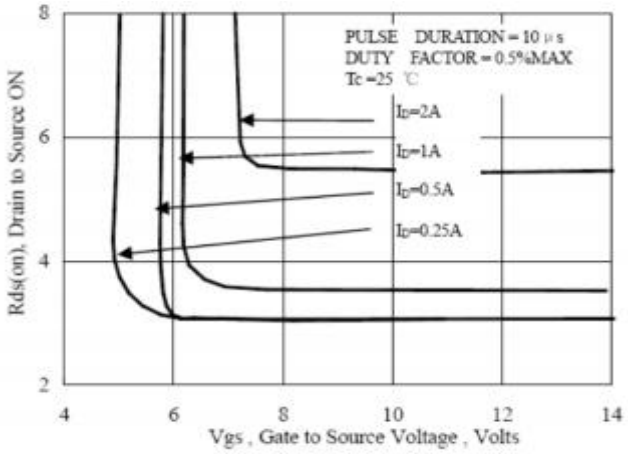


Figure 8 Typical Drain to Source ON Resistance vs Gate Voltage and Drain Current

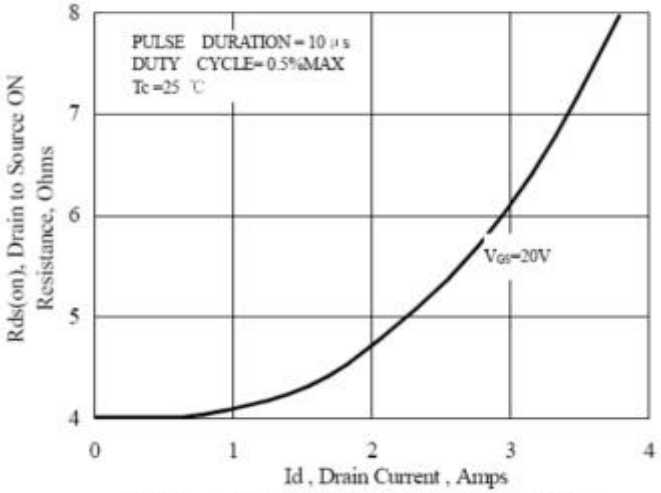


Figure 9 Typical Drain to Source ON Resistance vs Drain Current

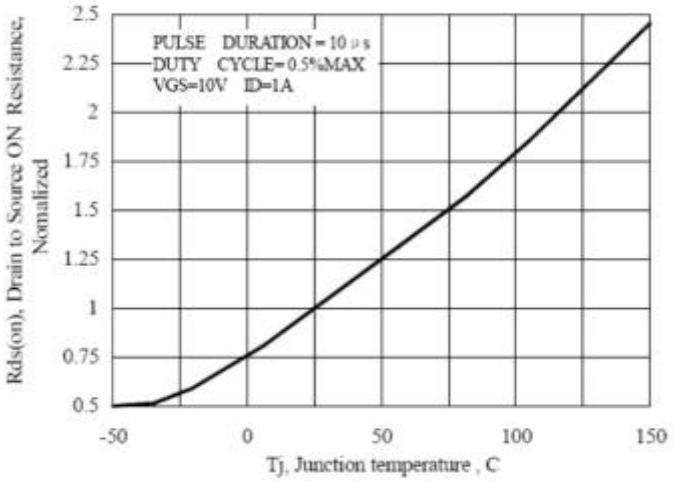


Figure 10 Typical Drian to Source on Resistance vs Junction Temperature

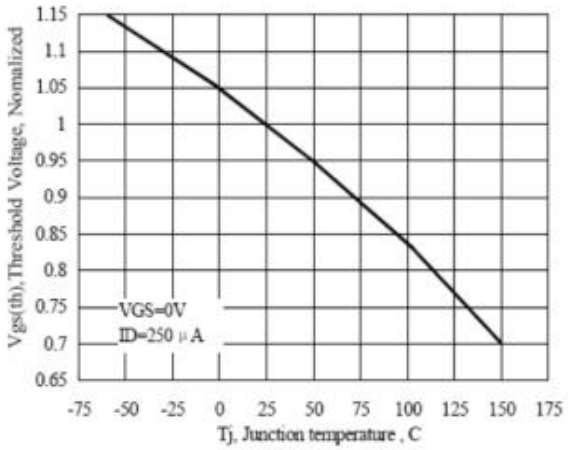


Figure 11 Typical Theshold Voltage vs Junction Temperature

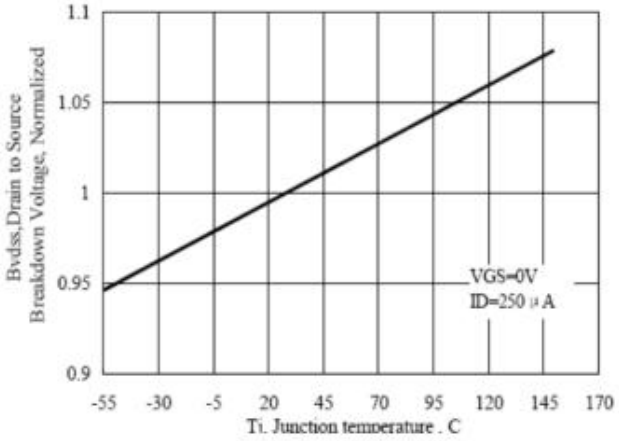


Figure 12 Typical Breakdown Voltage vs Junction Temperature

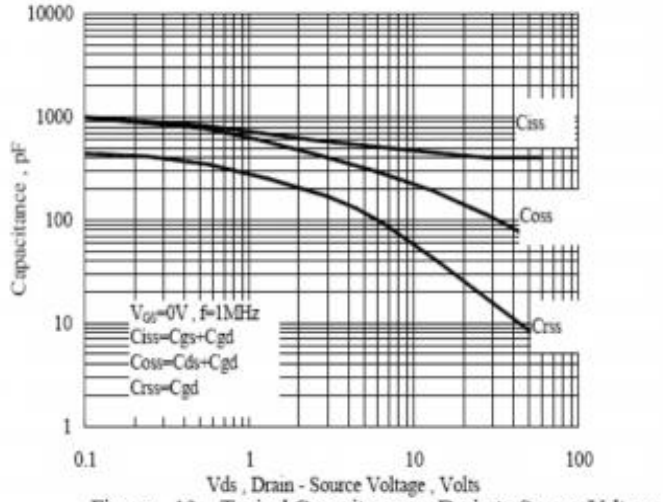


Figure 13 Typical Capacitance vs Drain to Source Voltage

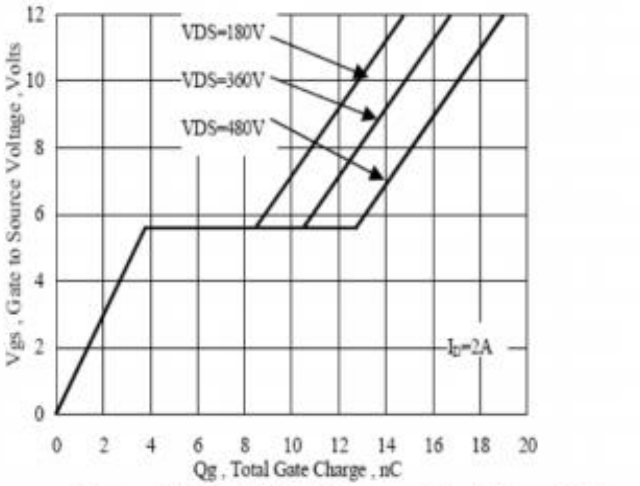


Figure 14 Typical Gate Charge vs Gate to Source Voltage

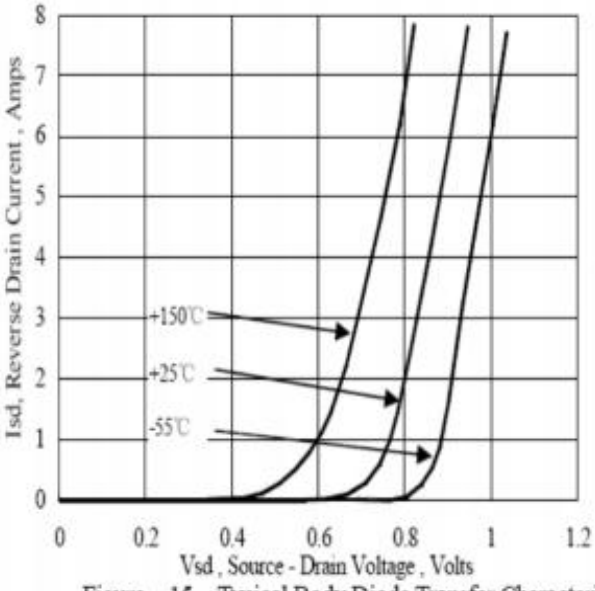


Figure 15 Typical Body Diode Transfer Characteristics

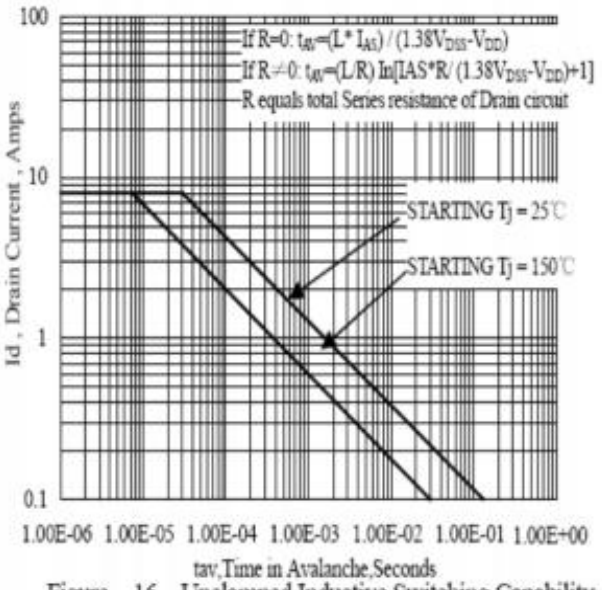


Figure 16 Unclamped Inductive Switching Capability

Test Circuits and Waveforms

Figure A: Gate Charge Test Circuit and Waveform

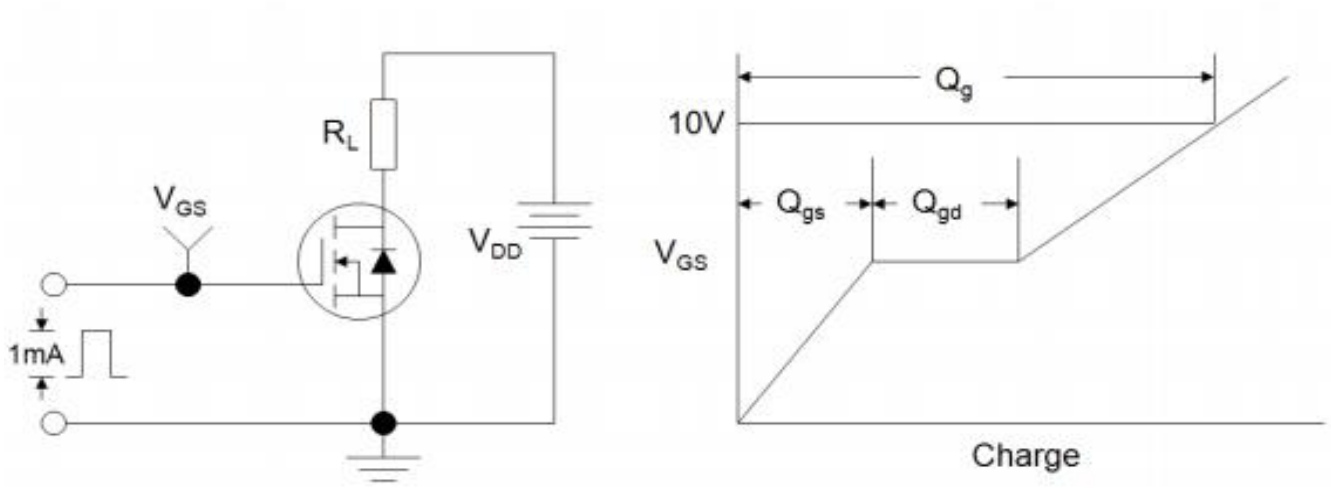


Figure B: Resistive Switching Test Circuit and Waveform

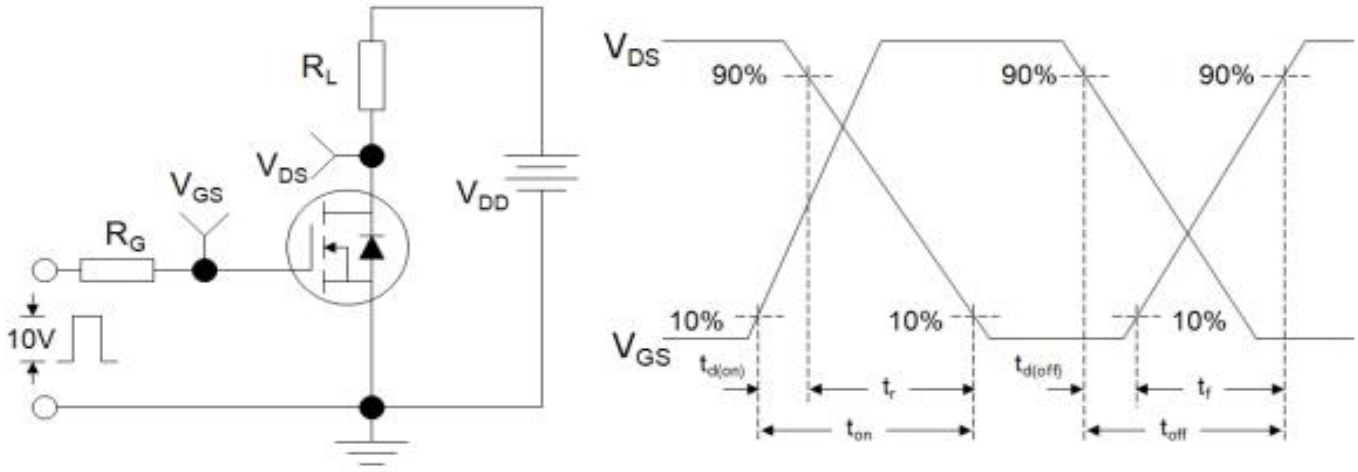
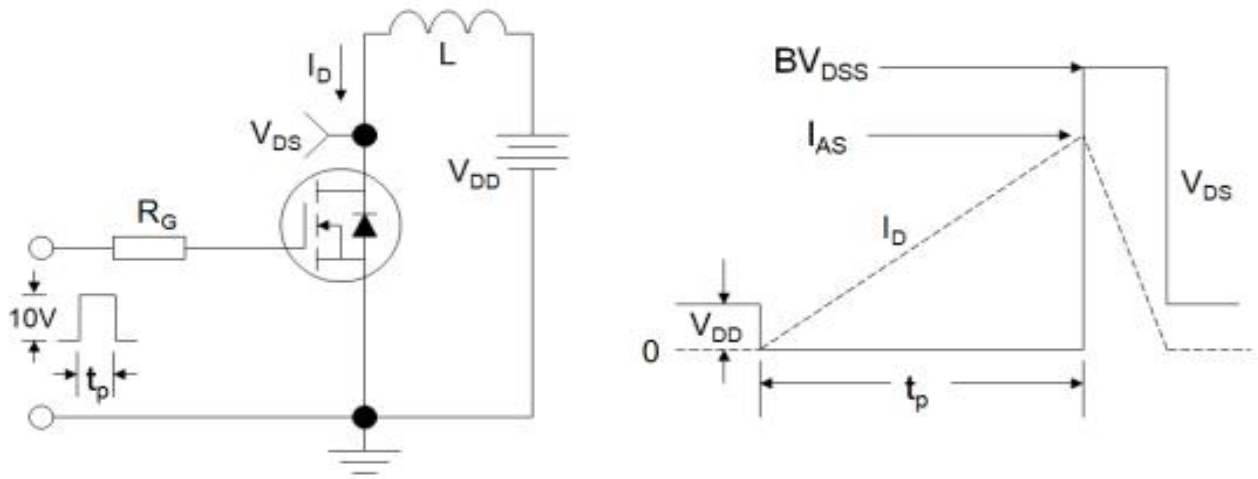
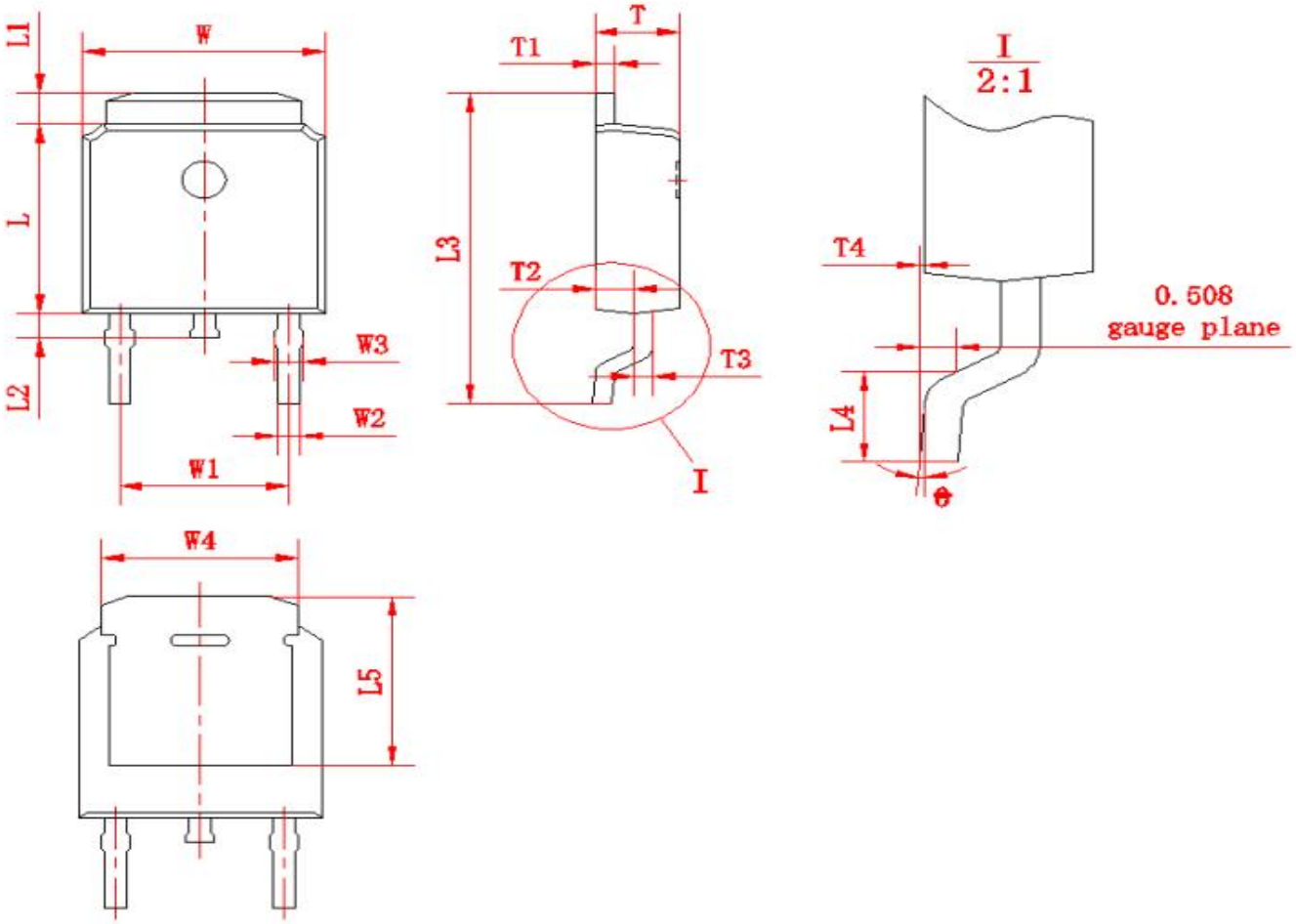


Figure C: Unclamped Inductive Switching Test Circuit and Waveform



Package outline drawing(TO-252 Unit: mm)



符号	尺寸		符号	尺寸		符号	尺寸	
	Min	Max		Min	Max		Min	Max
W	6.50	6.70	L1	0.80	1.20	T1	0.48	0.58
W1	(4.572)		L2	0.60	1.00	T2	0.95	1.15
W2	0.6	0.8	L3	9.70	10.30	T3	0.48	0.58
W3	0.68	0.88	L4	1.30	1.70	T4	0.00	0.12
W4	(5.3)		L5	(5.20)		0	0	8
L	6.00	6.20	T	2.20	2.40			

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