

## FDS4935A-NL-VB Datasheet

## Dual P-Channel 30-V (D-S) MOSFET

## PRODUCT SUMMARY

$V_{DS}$ (V)	$R_{DS(on)}$ ( $\Omega$ )	$I_D$ (A) <sup>d, e</sup>	$Q_g$ (Typ.)
- 30	0.021 at $V_{GS} = - 10$ V	- 8.0	15 nC
	0.028 at $V_{GS} = - 4.5$ V	- 7.0	

## FEATURES

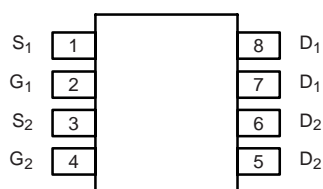
- Halogen-free
- TrenchFET<sup>®</sup> Power MOSFET
- 100 % UIS Tested

## APPLICATIONS

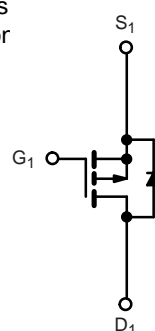
- Load Switches
- Notebook PCs
- Desktop PCs
- Game Station


**RoHS**  
 COMPLIANT

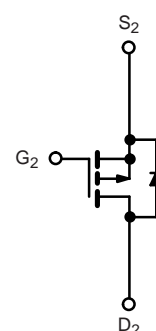
SO-8



Top View



P-Channel MOSFET



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS  $T_A = 25$  °C, unless otherwise noted

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	- 30	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	
Continuous Drain Current ( $T_J = 150$ °C)	$T_C = 25$ °C	- 9.5 <sup>e</sup>	A
	$T_C = 70$ °C	- 8.0 <sup>e</sup>	
	$T_A = 25$ °C	- 8.3 <sup>a, b</sup>	
	$T_A = 70$ °C	- 7.9 <sup>a, b</sup>	
Pulsed Drain Current	$I_{DM}$	- 32 <sup>e</sup>	
Continuous Source-Drain Diode Current	$T_C = 25$ °C	- 4.1	
	$T_A = 25$ °C	- 2.0 <sup>a, b</sup>	
Avalanche Current	$L = 0.1$ mH	$I_{AS}$	- 20
Single-Pulse Avalanche Energy		$E_{AS}$	20
Maximum Power Dissipation	$T_C = 25$ °C	$P_D$	5.0
	$T_C = 70$ °C		3.2
	$T_A = 25$ °C		2.5 <sup>a, b</sup>
	$T_A = 70$ °C		1.6 <sup>a, b</sup>
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	- 55 to 150	°C

## THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient <sup>a, c</sup>	$R_{thJA}$	38	50	°C/W
Maximum Junction-to-Foot	$R_{thJF}$	20	25	

Notes:

a. Surface mounted on 1" x 1" FR4 board.

b.  $t = 10$  s.

c. Maximum under Steady State conditions is 85 °C/W.

d. Based on  $T_C = 25$  °C.

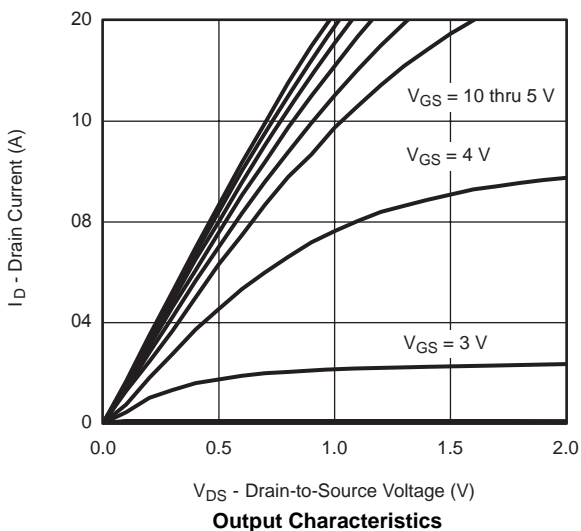
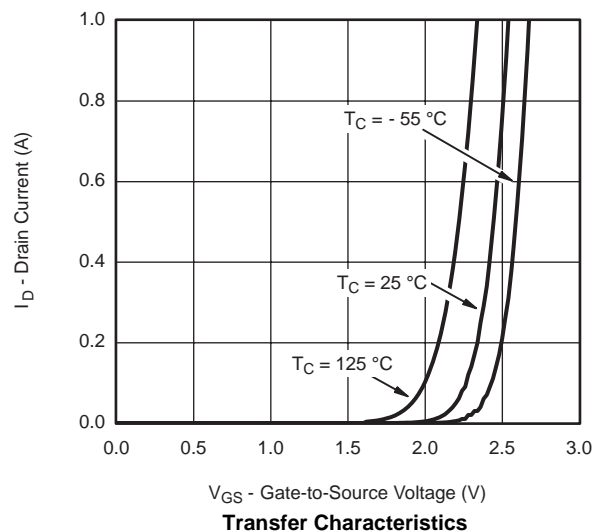
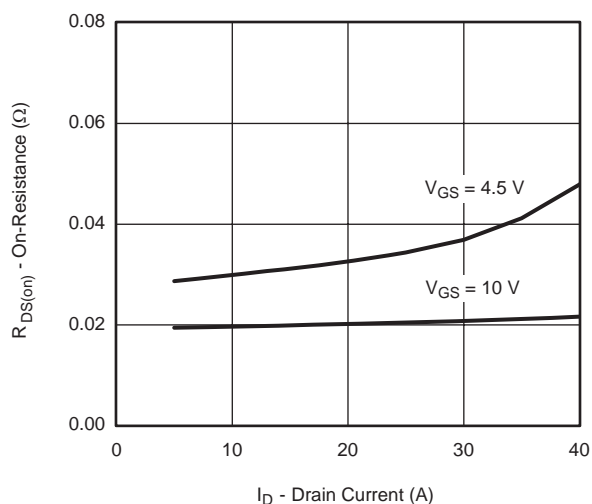
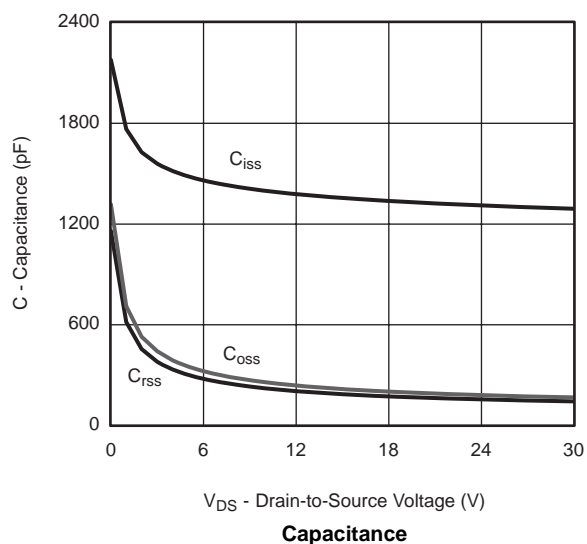
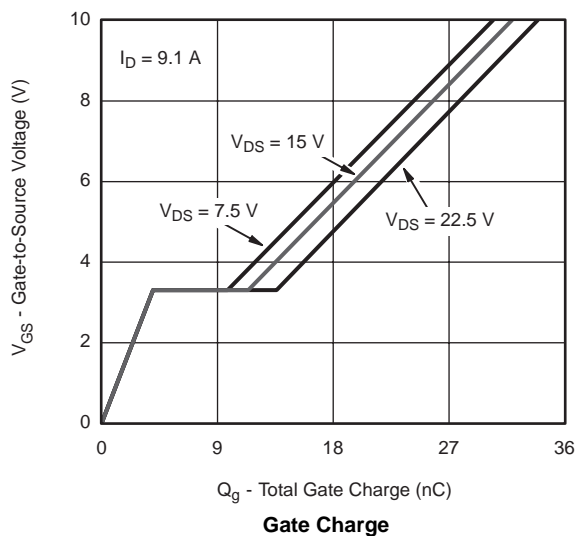
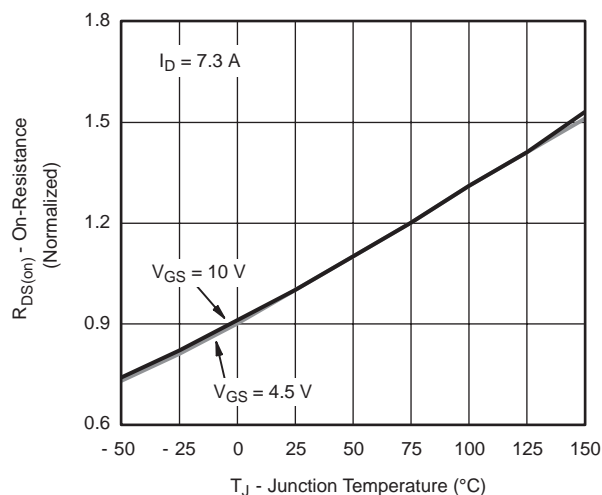
e. Limited by package.

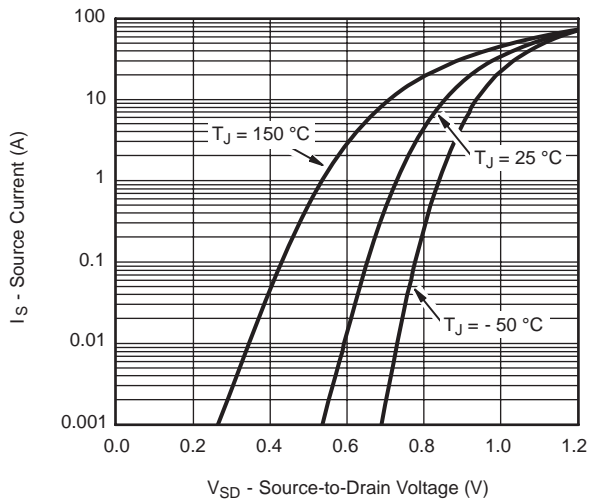
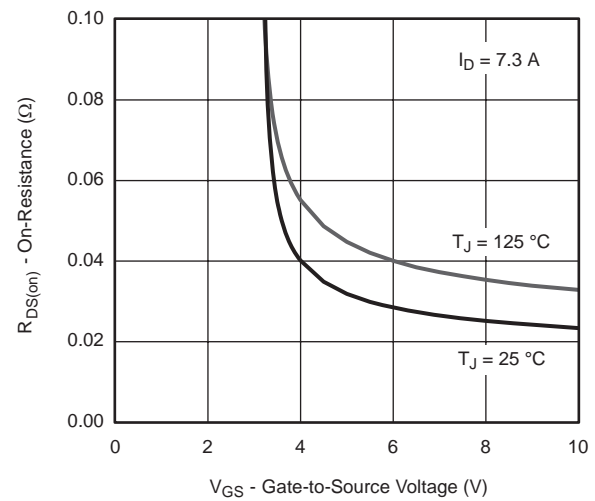
SPECIFICATIONS T <sub>J</sub> = 25 °C, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = - 250 μA	- 30			V
V <sub>DS</sub> Temperature Coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>	I <sub>D</sub> = - 250 μA		- 31		mV/°C
V <sub>GS(th)</sub> Temperature Coefficient	ΔV <sub>GS(th)</sub> /T <sub>J</sub>			4.5		
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = - 250 μA	- 1.0		- 3.0	V
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = - 30 V, V <sub>GS</sub> = 0 V			- 1	μA
		V <sub>DS</sub> = - 30 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55 °C			- 5	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> ≥ - 10 V, V <sub>GS</sub> = - 10 V	- 30			A
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = - 10 V, I <sub>D</sub> = - 7.3 A		0.021		Ω
		V <sub>GS</sub> = - 4.5 V, I <sub>D</sub> = - 6.2 A		0.028		
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = - 10 V, I <sub>D</sub> = - 9.1 A		23		S
Dynamic <sup>b</sup>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = - 15 V, V <sub>GS</sub> = 0 V, f = 1 MHz		1350		pF
Output Capacitance	C <sub>oss</sub>			215		
Reverse Transfer Capacitance	C <sub>rss</sub>			185		
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> = - 15 V, V <sub>GS</sub> = - 10 V, I <sub>D</sub> = - 9.1 A		32	50	nC
Gate-Source Charge	Q <sub>gs</sub>	V <sub>DS</sub> = - 15 V, V <sub>GS</sub> = - 4.5 V, I <sub>D</sub> = - 9.1 A		15	25	
Gate-Drain Charge	Q <sub>gd</sub>			4		
Gate Resistance	R <sub>g</sub>			7.5		
Gate Resistance	R <sub>g</sub>	f = 1 MHz		5.8		Ω
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = - 15 V, R <sub>L</sub> = 15 Ω I <sub>D</sub> ≡ - 1 A, V <sub>GEN</sub> = - 10 V, R <sub>g</sub> = 1 Ω		10	15	ns
Rise Time	t <sub>r</sub>			8	15	
Turn-Off DelayTime	t <sub>d(off)</sub>			45	70	
Fall Time	t <sub>f</sub>			12	25	
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = - 15 V, R <sub>L</sub> = 15 Ω I <sub>D</sub> ≡ - 1 A, V <sub>GEN</sub> = - 4.5 V, R <sub>g</sub> = 1 Ω		42	70	
Rise Time	t <sub>r</sub>			35	60	
Turn-Off DelayTime	t <sub>d(off)</sub>			40	70	
Fall Time	t <sub>f</sub>			16	30	
Drain-Source Body Diode Characteristics						
Continous Source-Drain Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25 °C			- 4.1	A
Pulse Diode Forward Current	I <sub>SM</sub>				- 32	
Body Diode Voltage	V <sub>SD</sub>	I <sub>S</sub> = - 2 A, V <sub>GS</sub> = 0 V		- 0.75	- 1.2	V
Body Diode Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = - 2 A, dI/dt = 100 A/μs, T <sub>J</sub> = 25 °C		34	60	ns
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>			22	40	nC
Reverse Recovery Fall Time	t <sub>a</sub>			11		ns
Reverse Recovery Rise Time	t <sub>b</sub>			23		

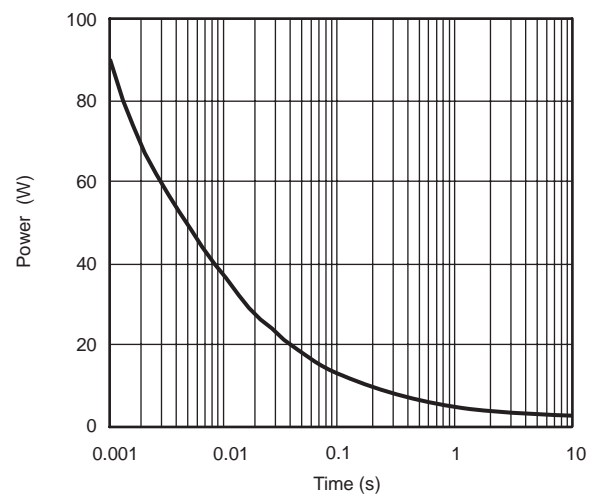
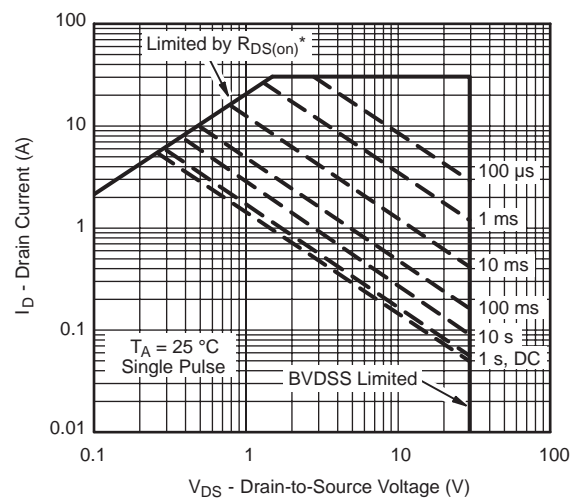
Notes:

- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .  
 b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

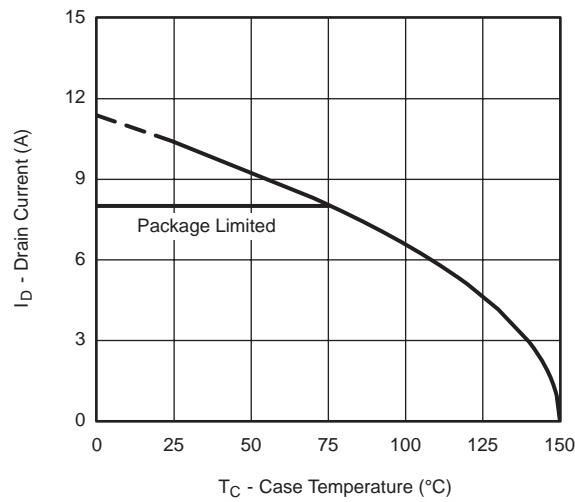
**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted

**Output Characteristics**

**Transfer Characteristics**

**On-Resistance vs. Drain Current**

**Capacitance**

**Gate Charge**

**On-Resistance vs. Junction Temperature**

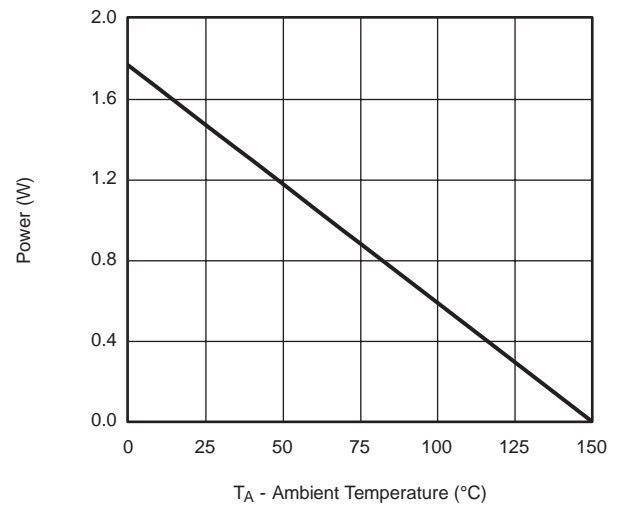
**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted

**Source-Drain Diode Forward Voltage**

**On-Resistance vs. Gate-to-Source Voltage**

**Threshold Voltage**

**Single Pulse Power, Junction-to-Ambient**


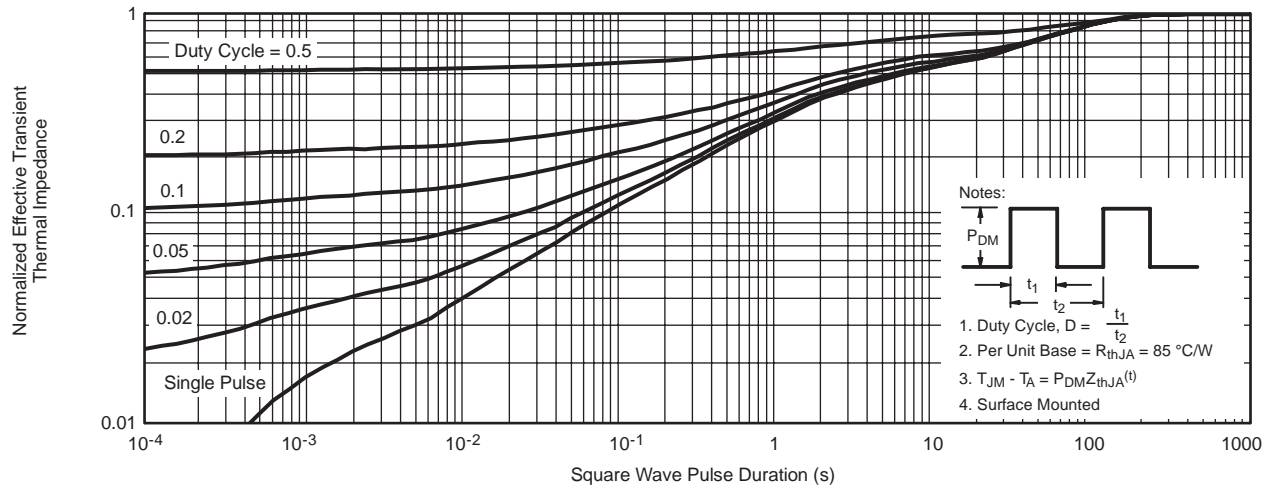
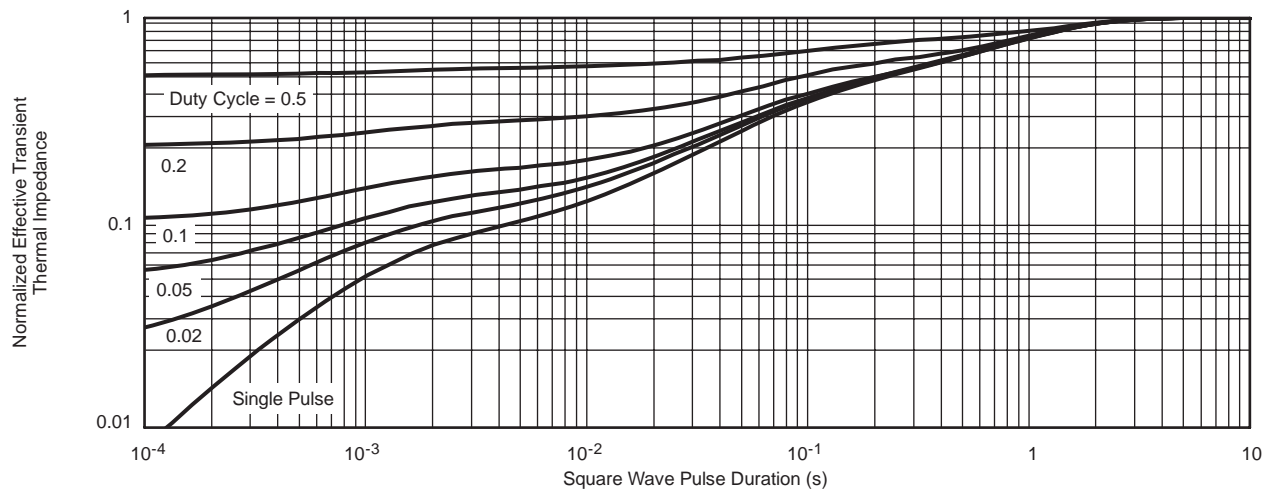
\*  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified

**Safe Operating Area**

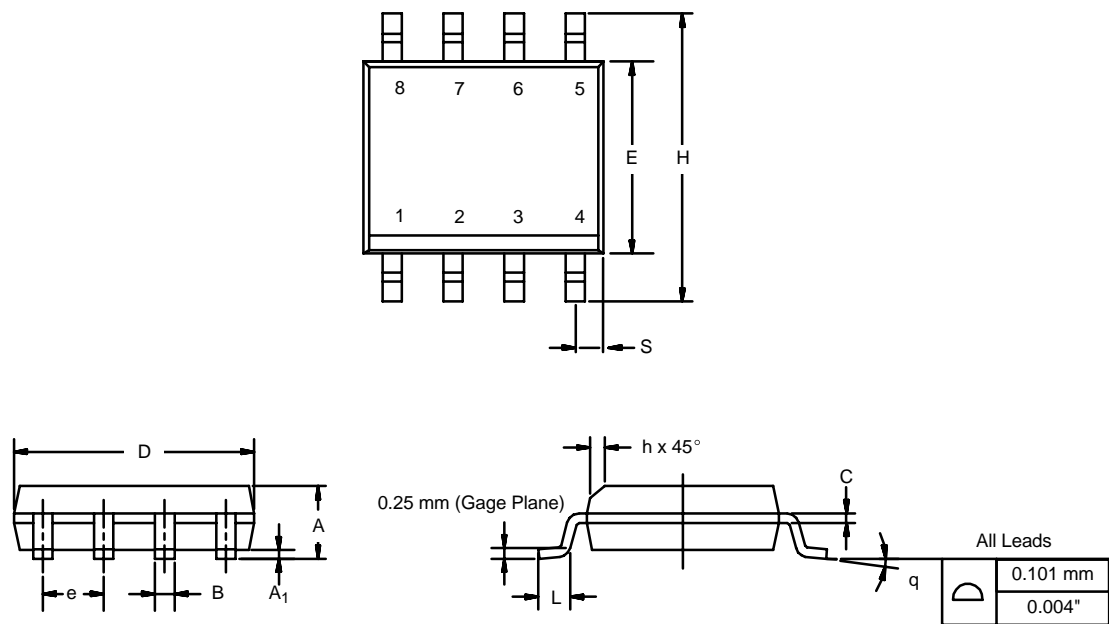
**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted

**Current Derating\***

**Power, Junction-to-Foot**

**Power Derating, Junction-to-Ambient**

\* The power dissipation  $P_D$  is based on  $T_{J(max)} = 150$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted

**Normalized Thermal Transient Impedance, Junction-to-Ambient**

**Normalized Thermal Transient Impedance, Junction-to-Foot**

**SOIC (NARROW): 8-LEAD**  
JEDEC Part Number: MS-012



DIM	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A <sub>1</sub>	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°
S	0.44	0.64	0.018	0.026
ECN: C-06527-Rev. I, 11-Sep-06				
DWG: 5498				

RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads  
Dimensions in Inches/(mm)



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