CLM5191HRT
HART调制解调器

简介

CLM5191HRT是一款单片CMOS调制解调器，用于高速可寻址远程

传感器(HART) 现场仪表和主机控制传输。调制解调器和一些外部无源组件提供满足HART物理层要求所需的所有功能，包括调制、解调、接收滤波、载波检测和传输信号整形。

CLM5191HRT使用每秒1200 bit的相位连续的频移键控（FSK)。为了节省功率，在发射操作期间将禁用/失能接收电路，反之亦然。这为在HART通信中的使用提供了半双工操作。

特点

- 单片、半双工每秒1200 bit的FSK调制解调器
- Bell 202变换频率为1200 Hz和2200 Hz
- 3.0V-5.5V的电源电压
- 发射信号波整形
- 接收带通滤波器
- 低功耗：安全应用的最佳选择
- 内部振荡器要求460.8 kHz晶体或陶瓷谐振器
- 符合HART物理层要求
- 工业温度范围为 −40℃至 +85℃
- 28引脚PLCC、32引脚QFN和32引脚LQFP封装
- 均是无铅器件

应用

- HART多路复用器
- HART调制解调器接口
- 4 – 20 mA的环路供电发射器

订购信息

零件号	温度范围	封装	状态
CLM5191HRTLG-XTP	-40°C ~ 85°C	LQFP-32	正常发货
CLM5191HRTPG-XTP	-40°C ~ 85°C	PLCC-28	正常发货
CLM5191HRTPG-XTD	-40°C ~ 85°C	PLCC-28	正常发货
CLM5191HRTLG-XTD	-40°C ~ 85°C	PLCC-28	正常发货
CLM5191HRTNG-XTP	-40°C ~ 85°C	QFN-32	正常发货

框图

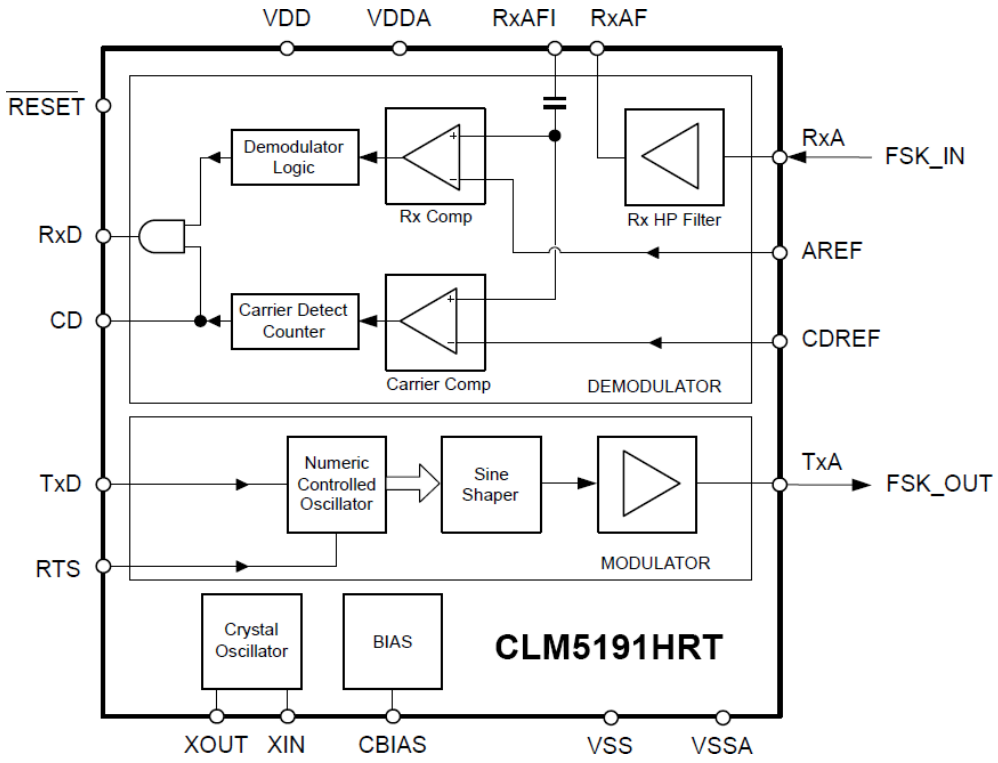


图1. CLM5191HRT框图

电气特性

表1. 最大极限值

Symbol	Parameter	Min	Max	Units
T_A	Ambient	−40	+85	°C
T_S	Storage Temperature	−55	+150	°C
T_J	Junction Temperature	−40	+85	°C
V_{DD}	Supply Voltage	−0.3	6.0	V
V_{IN}, V_{OUT}	DC Input, Output	−0.3	VDD + 0.3	V

超过最大极限值表中列出的应力可能会损坏器件。如果超过这些限制中的任何一个，则可能会发生损坏，并且可能会影响可靠性。

1. CMOS器件被高能静电放电损坏。器件必须存放在导电泡沫中或所有引脚均被分流。应采取预防措施，避免施加高于最大极限值的电压。高于最大极限值的应力可能会损坏器件。
2. 在插入或移除此器件之前，请先关掉电源。

表2. 直流特性 (V_{DD} = 3.0 V~5.5 V , V_{SS} = 0 V , T_A = − 40℃ ~ + 85℃)

Symbol	Parameter	V_{DD}	Min	Typ	Max	Units
V_{IL}	Input Voltage, Low	3.0 – 5.5 V			0.3 * V_{DD}	V
V_{IH}	Input Voltage, High	3.0 – 5.5 V	0.7 * V_{DD}			V
V_{OL}	Output Voltage, Low (I_{OL} = 0.67 mA)	3.0 – 5.5 V			0.4	V
V_{OH}	Output Voltage, High (I_{OH} = −0.67 mA)	3.0 – 5.5 V	2.4			V
C_{IN}	Input Capacitance of: Analog Input RXA Digital Input			 2.9 25 3.5		 pF pF pF
I_{IL}/I_{IH}	Input Leakage Current				±500	nA
I_{OLL}	Output Leakage Current				±10	µA
I_{DDA}	Power Supply Current (RBIAS = 500 kΩ, AREF = 1.235 V)	3.3 V 5.0 V	150 150	330 300	450 600	µA µA
I_{DDD}	Dynamic Digital Current	5.0 V	25		200	µA
A_{REF}	Analog Reference	3.3 V 5.0 V	1.2	1.235 2.5	2.6	V V
CD_{REF} (Note 3)	Carrier Detect Reference (AREF – 0.08 V)	3.3 V 5.0 V		1.15 2.42		V
C_{BIAS}	Comparator Bias Current (RBIAS = 500 kΩ, AREF = 1.235 V)			2.5		µA

3. HART规范要求载波检测 (CD) 须在80和120 mVp-p之间处于活动状态。将CDREF设置为AREF-0.08 VDC会将载波检测设置为标称100 mVp-p。

表3. 交流特性 (V_{DD} = 3.0 V~5.5 V , V_{SS} = 0 V , T_A = − 40℃ ~ + 85℃)

Pin Name	Description	Min	Typ	Max	Units
RxA	Receive analog input Leakage current Frequency – mark (logic 1) Frequency – space (logic 0)	 1190 2180	 1200 2200	 ±150 1210 2220	 nA Hz Hz
RxAF	Output of the high−pass filter Slew rate Gain bandwidth (GBW) Voltage range	 150 0.15	 0.025 	 V_{DD} – 0.15	 V/µs kHz V
RxAFI	Carrier detect and receive filter input Leakage current			 ±500	 nA
TxA	Modulator output Frequency – mark (logic 1) Frequency – space (logic 0) Amplitude (AREF 1.235 V) Slew Rate − mark (logic 1) Slew Rate − space (logic 0) Loading (AREF = 1.235 V)	 30	 1196.9 2194.3 500 1860 3300 	 	 Hz Hz mV V/s V/s kΩ
RxD	Receive digital output Rise/fall time	 20			ns
CD	Carrier detect output Rise/fall time	 20			ns

产品参数性能在所列测试条件的电气特性中被给出，除非另有说明。在不同条件下运行，则可能无法与该产品电气特性相吻合。

4. 模块化输出频率与输入时钟频率 (460.8 kHz) 成比例。

表4. 调制解调器特性 (V_{DD} = 3.0 V~5.5 V , V_{SS} = 0 V , T_A = − 40℃ ~ + 85℃)

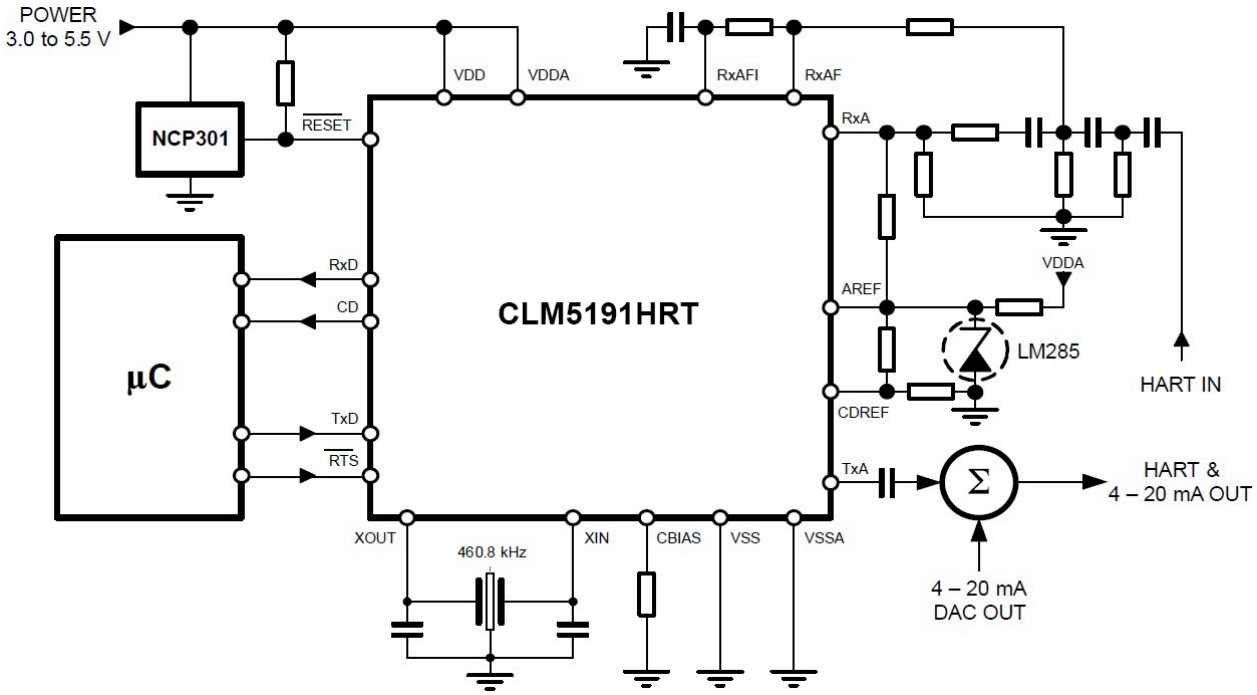
Parameter	Min	Typ	Max	Units
Demodulator jitter Conditions 1. Input frequencies at 1200 Hz ± 10 Hz, 2200 Hz ± 20 Hz 2. Clock frequency of 460.8 kHz ± 0.1% 3. Input (RxA) asymmetry, 0			12	% of 1 bit

表5. 陶瓷谐振器-外部时钟特性 (V_{DD} = 3.0 V~5.5 V , V_{SS} = 0 V , T_A = − 40℃ ~ + 85℃)

Parameter	Min	Typ	Max	Units
Resonator Tolerance Frequency		 460.8	 1.0 	 % kHz
External Clock frequency Duty cycle Amplitude	 456.2 40	 460.8 50 V_{OH} – V_{OL}	 465.4 60 	 kHz % V

典型应用

5.



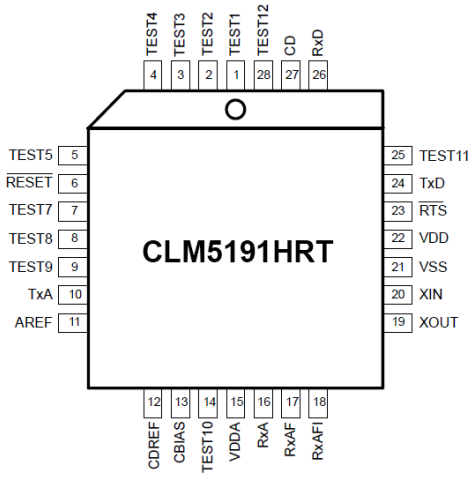


图3. 28引脚PLCC的CLM5191HRT引脚

表6. 28引脚PLCC的引脚汇总

Pin No.	Signal Name	Type	Pin Description
1	TEST1	Input	Connect to VSS
2, 3, 4	TEST2, 3, 4	–	Do Not Connect
5	TEST5	Input	Connect to VSS
6	RESETB	Input	Reset all digital logic when low
7, 8, 9	TEST7, 8, 9	Input	Connect to VSS
10	TxA	Output	Transmit Data Modulator output
11	AREF	Input	Analog reference voltage
12	CDREF	Input	Carrier detect reference voltage
13	CBIAS	Output	Comparator bias current
14	TEST10	Input	Connect to VSS
15	VDDA	Power	Analog supply voltage
16	RxA	Input	Receive Data Modulator input
17	RxAF	Output	Analog receive filter output
18	RxAFI	Input	Analog receive comparator input
19	XOUT	Output	Crystal oscillator output
20	XIN	Input	Crystal oscillator input
21	VSS	Ground	Ground
22	VDD	Power	Digital supply voltage
23	RTSB	Input	Request to send
24	TxD	Input	Input transmit date, transmitted HART data stream from microcontroller
25	TEST11	–	Do Not Connect
26	RxD	Output	Received demodulated HART data to microcontroller
27	CD	Output	Carrier detect output
28	TEST12	–	Do Not Connect

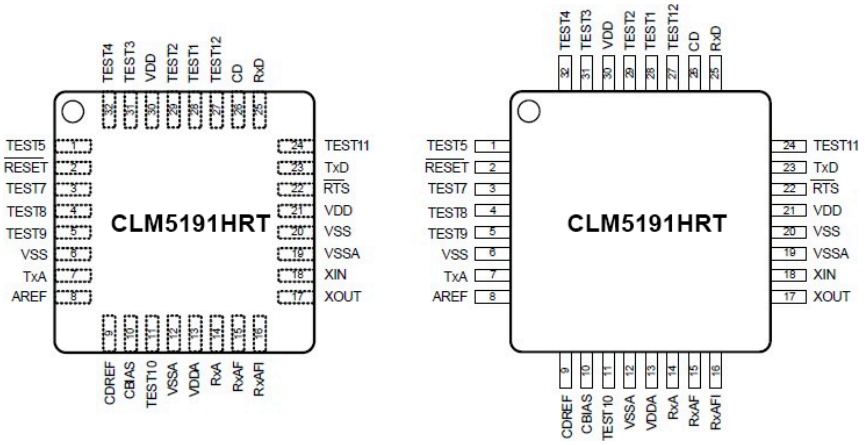


图4. 32引脚QFN和LQFP的CLM5191HRT引脚(顶视图)

表7. 32引脚QFN和LQFP的引脚

Pin No.	Signal Name	Type	Pin Description
1	TEST5	Input	Connect to VSS
2	RESETB	Input	Reset all logic when low, connect to VDD for normal operation
3, 4, 5	TEST7, 8, 9	Input	Connect to VSS
6	VSS	Ground	Digital ground
7	TxA	Output	Transmit Data Modulator output
8	AREF	Input	Analog reference voltage
9	CDREF	Input	Carrier detect reference voltage
10	CBIAS	Output	Comparator bias current
11	TEST10	Input	Connect to VSS
12	VSSA	Ground	Analog ground
13	VDDA	Power	Analog supply voltage
14	RxA	Input	Receive Data Modulator input
15	RxAF	Output	Analog receive filter output
16	RxAFI	Input	Analog receive comparator input
17	XOUT	Output	Crystal oscillator output
18	XIN	Input	Crystal oscillator input
19	VSSA	Ground	Analog ground
20	VSS	Ground	Digital ground
21	VDD	Power	Digital supply voltage
22	RTSB	Input	Request to send
23	TxD	Input	Input transmit data, transmit HART data stream from microcontroller
24	TEST11	–	Do Not Connect
25	RxD	Output	Received demodulated HART data to microcontroller
26	CD	Output	Carrier detect output
27	TEST12	–	Do Not Connect
28	TEST1	Input	Connect to VSS
29	TEST2	–	Do Not Connect
30	VDD	Power	Digital supply voltage
31, 32	TEST3, 4	–	Do Not Connect
EP	Exposed Pad	Power	Connect to VSS (QFN only)

引脚介绍

表8. 引脚介绍

Symbol	Pin Name	Description
AREF	Analog reference voltage	Receiver Reference Voltage. Normally 1.23 V is selected (in combination with VDDA = 3.3 V). See Table 2.
CDREF	Carrier detect reference voltage	Carrier Detect Reference voltage. The value should be 85 mV below AREF to set the carrier detection to a nominal of 100 mV_{p-p}.
RESETB	Reset digital logic	When at logic low (V_{SS}) this input holds all the digital logic in reset. During normal operation RESETB should be at V_{DD}. RESETB should be held low for a minimum of 10 nS after V_{DD} = 2.5 V as shown in Figure 14.
RTSB	Request to send	Active−low input selects the operation of the modulator. TxA is enabled when this signal is low. This signal must be held high during power−up.
RxA	Analog receive input	Receive Data Demodulator Input. Accepts a HART 1200 / 2200 Hz FSK modulated waveform input.
RxAFI	Analog receive comparator input	Positive input of the carrier detect comparator and the receiver filter comparator.
TxD	Digital transmit input	Input to the modulator accepts digital data in NRZ form. When TxD is low, the modulator output frequency is 2200 Hz. When TxD is high, the modulator output frequency is 1200 Hz.
XIN	Oscillator input	Input to the internal oscillator must be connected to a parallel mode 460.8 kHz ceramic resonator when using the internal oscillator or grounded when using an external 460.8 kHz clock signal.
CBIAS	Comparator bias current	Connection to the external bias resistor. R_{BIAS} should be selected such that AREF / R_{BIAS} = 2.5 μA ± 5 %
CD	Carrier detect output	Output goes high when a valid input is recognized on RxA. If the received signal is greater than the threshold specified on CDREF for four cycles of the RxA signal, the valid input is recognized.
RxAF	Analog receive filter output	The output of the three pole high pass receive data filter
RxD	Digital receive output	Signal outputs the digital receive data. When the received signal (RxA) is 1200 Hz, RxD outputs logic high. When the received signal (RxA) is 2200 Hz, RxD outputs logic low. The HART receive data stream is only active if Carrier Detect (CD) is high.
TxA	Analog transmit output	Transmit Data Modulator Output. A trapezoidal shaped waveform with a frequency of 1200 Hz or 2200 Hz corresponding to a data value of 1 or 0 respectively applied to TxD. TxA is active when RTSB is low. TxA equals 0.5 V when RTSB is high.
XOUT	Oscillator output	Output from the internal oscillator must be connected to an external 460.8 kHz clock signal or to a parallel mode 460.8 kHz ceramic resonator when using the internal oscillator.
TEST(12:1)	Factory test	Factory test pins; for normal operation, tie these signals as per Tables 6 and 7
VDD	Digital power	Power for the digital modem circuitry
VDDA	Analog supply voltage	Power for the analog modem circuitry
VSS	Ground	Digital ground (and Analog ground in the case of PLCC package)
VSSA	Analog ground	Analog ground

功能介绍

CLM5191HRT是用于高速可寻址远程传感器（HART）现场仪表和主机控制传输的单片调制解调器。调制解调器IC包含具有信号整形器的发射数据调制器、载波检测电路、模拟接收器、解调器电路和晶体振荡器，如图1 中的框图所示。

调制器在其数字输入TxD处接受数字数据，并在模拟输出TxA 处生成正弦形FSK 调制信号。数字 “1”（mark）以1200Hz的频率来呈现。数字 “0”（space） 以2200Hz的频率来呈现。所使用的比特率是1200波特。

解调器在其模拟输入端接收FSK信号，用带通滤波 器对其进行滤波，并生成2个数字信号: RxD，接收数据； CD，载波检测。在数字输出RxD处，接收原始的调制信号。CD输出载波检测信号。如果在 4 个连续载波周期内接收到的信号高于 100 mVpp，则它变为逻辑高电平。

使用简单的外部谐振器或外部时钟源，振荡器为调制解调器提供了稳定的时基。

详细介绍

调制器

调制器在TxD输入端接受NRZ形式的数字数据，并在TxA输出端产生FSK调制信号。

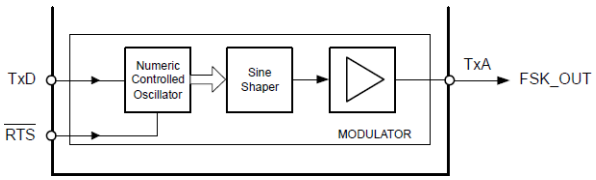


图5. 调制器框图

逻辑“1” （mark）由频率fm = 1200Hz来表示。
逻辑 “0” （space）由频率fs = 2200Hz来表示。

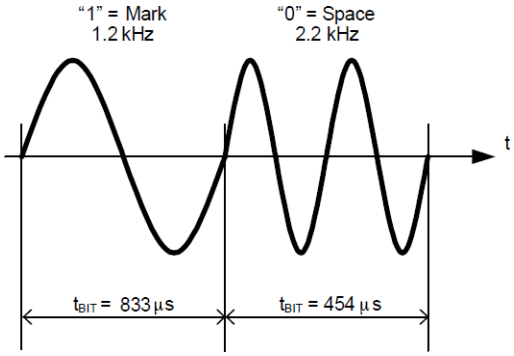


图6.调制时序

数控振荡器NCO以相位连续模式工作， 防止在mark和space频率之间切换时突然发生相移。控制信号RTSB（请求发送）使能NCO。当RTSB为逻辑低电平时，调制器处于有效的活动状态，且CLM5191HRT处于发送模式。而当RTSB为逻辑高时，调制器将被失能，此时CLM5191HRT处于接收模式。

NCO的数字输出在波形整形块中被整形为梯形信号。该电路将上升沿和下降沿控制在标准HART波形的极限之内。图7给出了在TxA处捕获的mark和space频率的发射信号。在mark频率下，转换速率为SR_m = 1860 V/s，在space频率下，转换速率为SR_S = 3300 V/s。当^{AREF} = 1.235 V时候，TxA将有大约0.25到0.75 V_{DC}的电压摆幅。

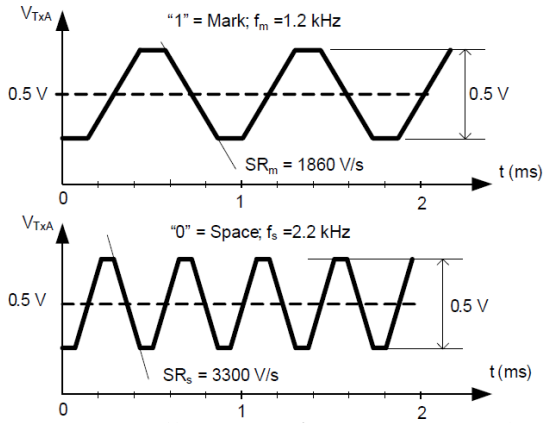


图7. 调制器输出信号，TxA引脚（mark和space频率）

解调器

解调器在RxA输入处接受FSK信号，并在RxD输出处重建原始调制信号。图8解释了解调的过程。

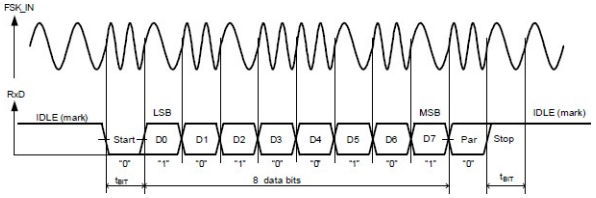


图8.调制时序

此HART位流遵循标准的11位UART帧，具体为1个开始位，8个数据位，1个奇偶位（奇数）和1个停止位。通信速度为1200波特。

接收滤波器和比较器

首先使用围绕低噪声接收器运算放大器构建的带通滤波器“Rx HP 滤波器”对接收到的FSK信号进行滤波。该滤波器可阻止HART信号频带之外的干扰。

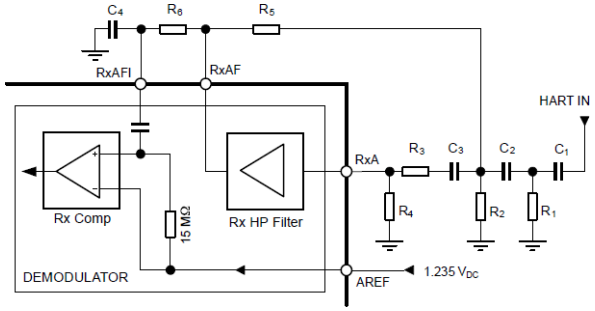


图9. 解调器接收滤波器和信号比较器

滤波器输出被送入Rx比较器。阈值等于模拟地， 其使比较器在滤波FSK信号的每个过零时进行切换。给定的输入频率如在HART规范内（时钟频率为460.8 kHz (±1.0%) 和零输入（RxA）不对称），则最大的解调器抖动12%（1位）。

载波检测电路

低HART输入信号电平会增加产生位错误的风险。因此，最小信号幅度被设定为80-120 mVpp。如果接收到的信号低于此电平，则解调器将被失能。

此电平检测将在载波检测器中完成。解调器的输出由载波检测信号 (CD) 来量化，因此，只有足够大的RxA信号 (典型100 mvp-p) 被载波检测电路检测到，才能在RxD产生接收的串行数据。

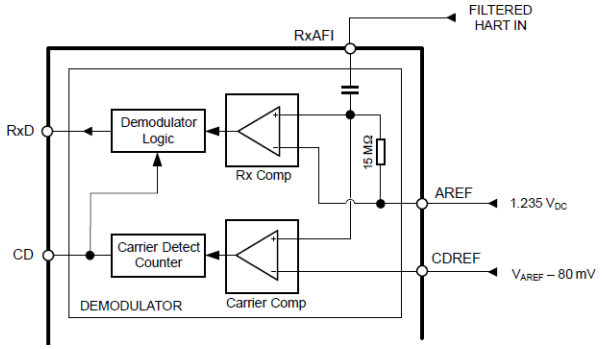


图10. 解调器载波和信号比较器

如果RxAFI电压低于CDREF，则图10中所示的载波检测比较器将生成逻辑低输出。比较器输出将被反馈到载波检测块中。载波检测块驱动载波检测输出CD为高

如果RTSB为高且比较器发出的四个连续脉冲到达时候。只要RTSB为高，并且在小于2.5 ms内接收到下一个比较器脉冲，则CD就保持为高。一旦CD进入非激活状态， 比较器需要连续发出四个脉冲才能再次置位CD。当接 收信号为3.33Hz时，四个连续脉冲等于1200 ms；当接收信号为2200 HZ时，四个连续脉冲等于1.82 ms。

其它模拟电路

电压基准

CLM5191HRT需要两个基准电压，AREF和CDREF。AREF设置内部运算放大器的直流工作点，并且是Rx比 较器的基准输入。如果CLM5191HRT在V_{DD} = 3.3 V下工作， 建议使用ON半导体的LM285D 1.235 V的基准。

CD （载波检测） 变为活动状态的电平由直流电压差(CDREF - AREF) 来确定。选择80 mV的电压差会将载波检测设置为标称100 mV_{p-p}。

偏置电流电阻

CLM5191HRT要求在CBIAS和V_{SS}之间连接偏置电流电阻R_{bias}。偏置电流控制内部运算放大器和比较器的工作参数，其应设置为2.5 μA。

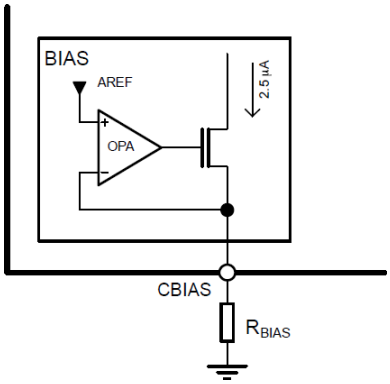


图11. 偏置电路

偏置电流电阻的值由基准电压AREF和以下公式确定：

$$R_{BIAS} = \frac{AREF}{2.5\ \mu A}$$

当AREF等于1.235V时推荐的偏置电流电阻为500KΩ。

振荡器

CLM5191HRT需要一个460.8 kHz的时钟信号。其可以由外部时钟或连接到CLM5191HRT内部振荡器的谐振器来提供。

内部振荡器选项

振荡器单元将与460.8 kHz晶体或陶瓷谐振器一起工作。XIN和XOUT之间可以连接一个并联的谐振陶瓷谐振器。图12给出了使用460.8 kHz (1%容差) 的并联谐振晶体和两个调谐电容Cx的时钟产生的晶体选项。电容的实际值可能取决于谐振器制造商的建议值。通常， 使用100 pF至470 pF范围内的电容。

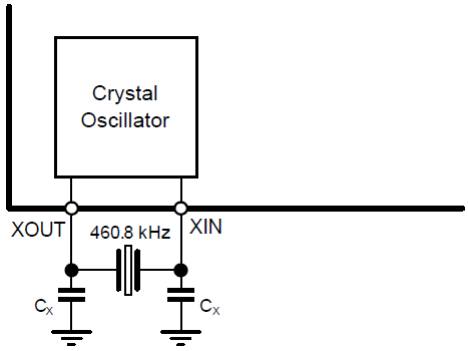


图12. 晶体振荡器

外部时钟选项

可能需要使用如图13所示的外部460.8 kHz的时钟而不是内部振荡器。当使用外部时钟时，CLM5191HRT消耗的电流将更少。当时钟连接到XOUT，XIN连接到V_{SS}时，电流消耗将最小。

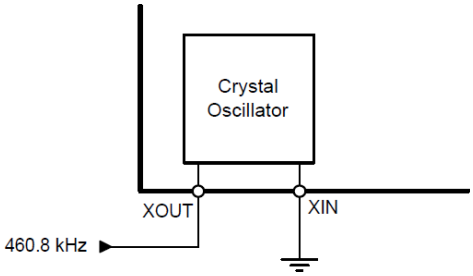
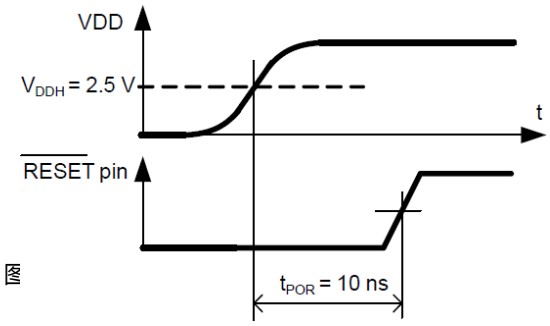


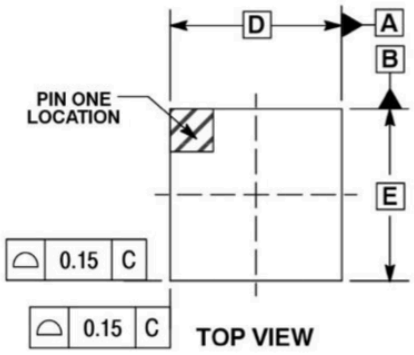
图13. 外部时钟振荡器

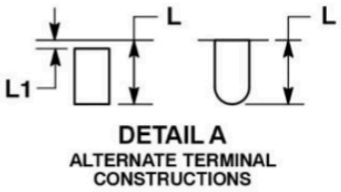
复位电源

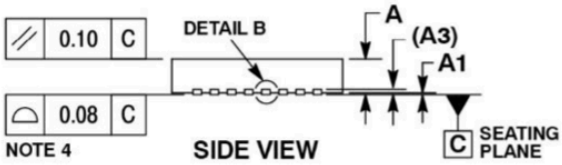
在启动过程中，RESETB引脚应保持低电平，直到V_{DD}上的电压电平高于最小电平V_{DDH} = 2.5 V，以保证数字电路的正确操作。如图14所示，在达到该阈值电压之后，RESETB应至少保持低电平为t_{POR} = 10 ns。

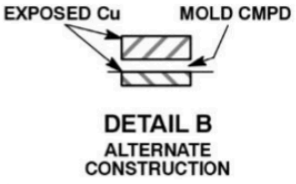


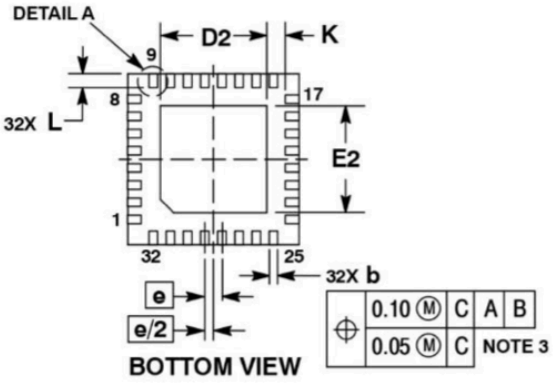
图







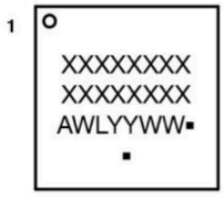




NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	---	0.05
A3	0.20 REF	
b	0.18	0.30
D	5.00 BSC	
D2	2.95	3.25
E	5.00 BSC	
E2	2.95	3.25
e	0.50 BSC	
K	0.20	---
L	0.30	0.50
L1	---	0.15

GENERIC MARKING DIAGRAM*

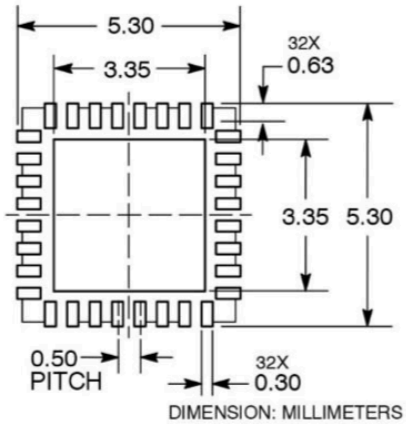


XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
▪ = Pb–Free Package

(Note: Microdot may be in either location)

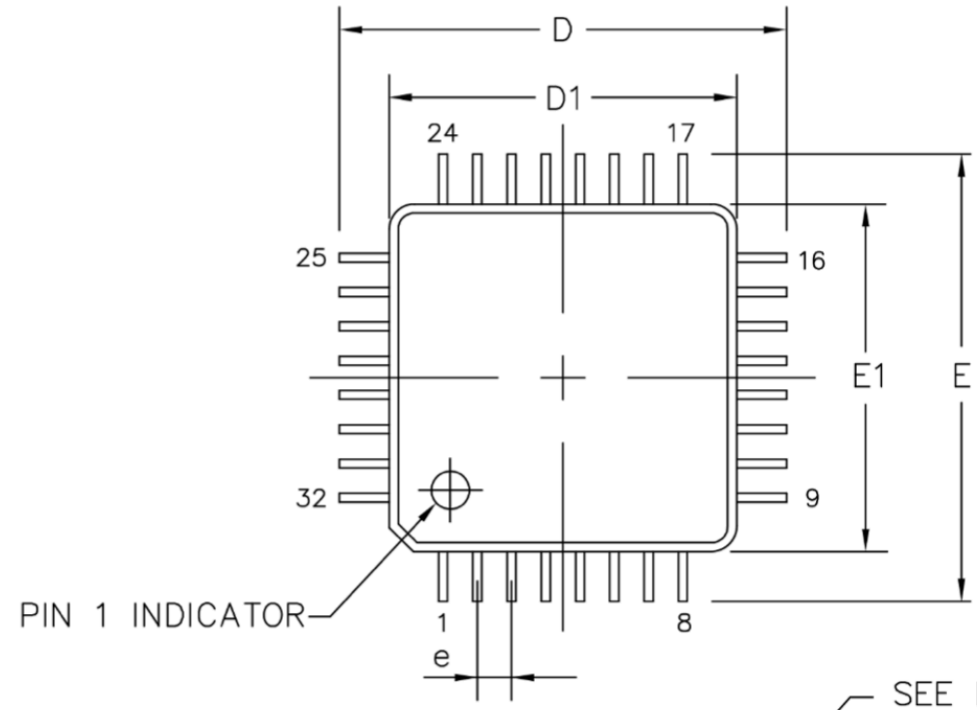
*This information is generic. Please refer to device data sheet for actual part marking.
Pb–Free indicator, "G" or microdot " ▪", may or may not be present.

RECOMMENDED SOLDERING FOOTPRINT*

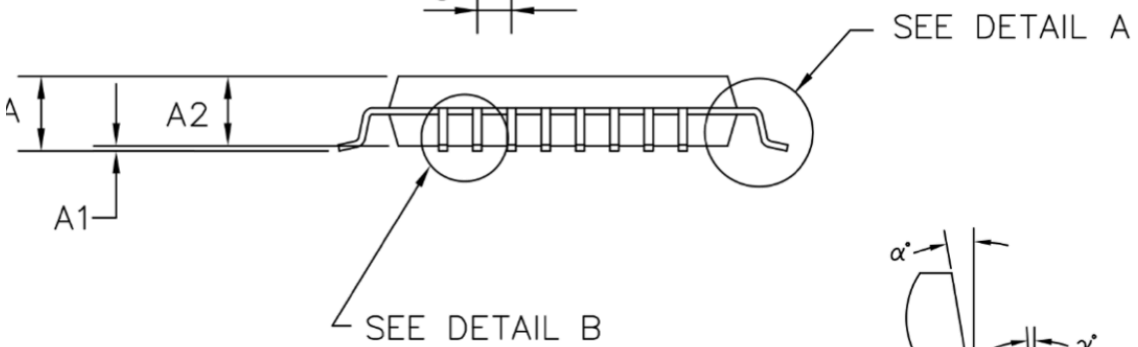


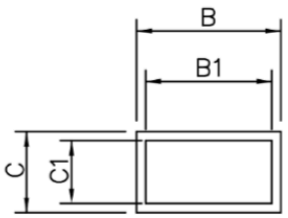
DIMENSION: MILLIMETERS

*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

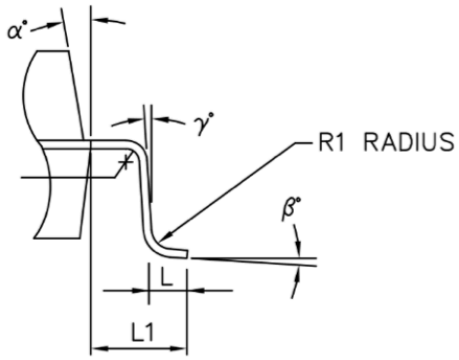


SYMBOL	MIN	NOM	MAX
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
B	0.30	0.37	0.45
B1	0.30	0.35	0.40
C	0.09	–	0.20
C1	0.09	–	0.16
D	9.00 BSC		
D1	7.00 BSC		
E	9.00 BSC		
E1	7.00 BSC		
e	0.80 BSC.		
L	0.45	0.60	0.75
L1	1.00		
R1	0.08	–	0.20
α°	11	–	13
β°	0	–	7
γ°	0	–	–



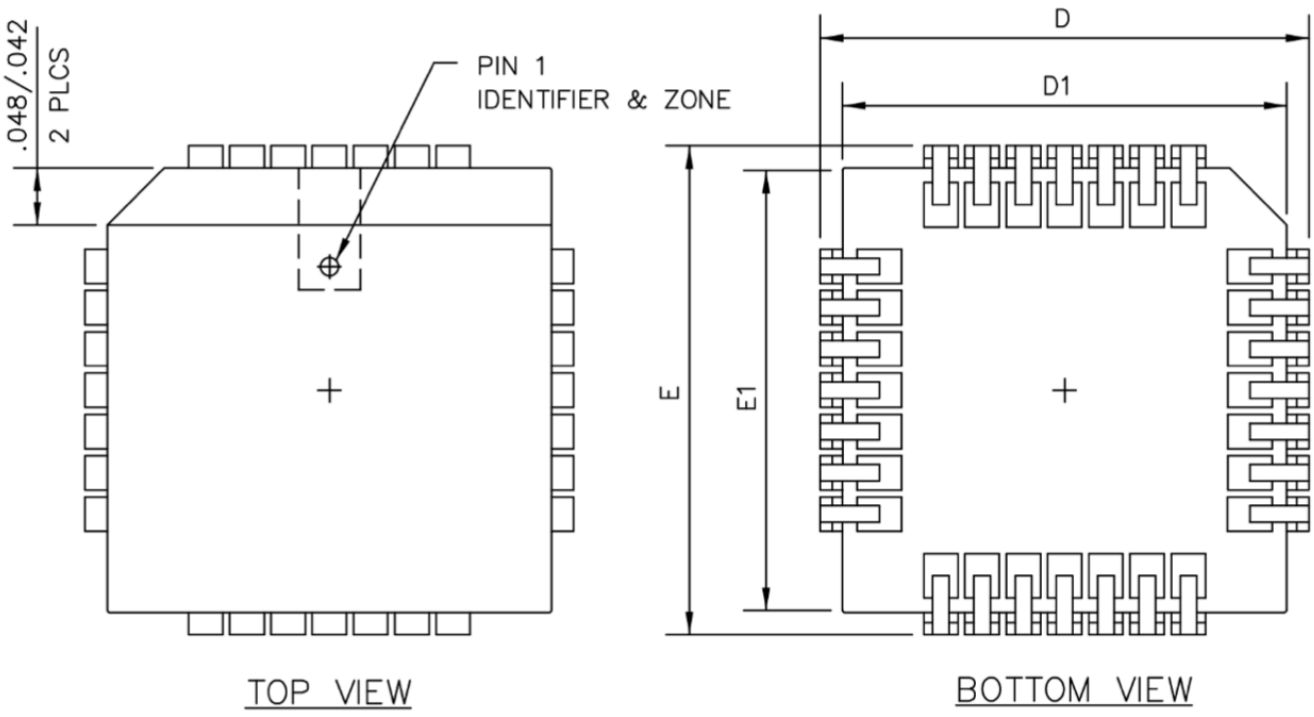


DETAIL B



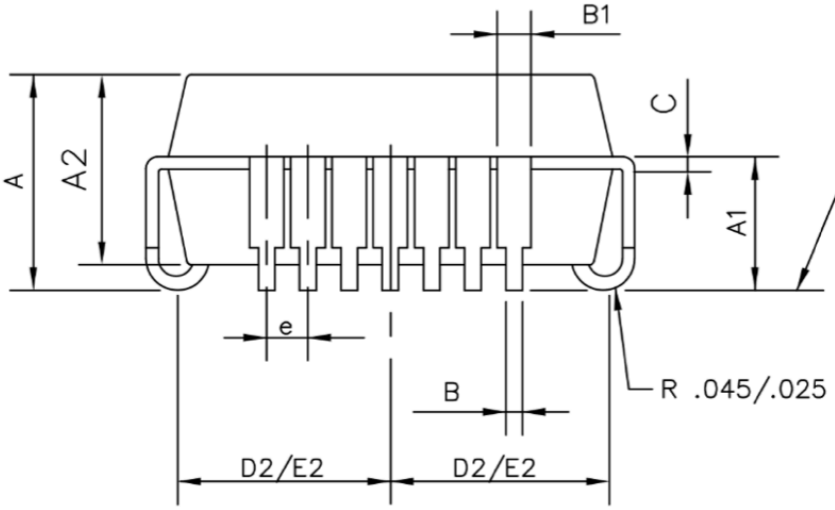
DETAIL A

ALL DIMENSIONS IN MM



TOP VIEW

BOTTOM VIEW



SIDE VIEW

SYMBOL	MIN	NOM	MAX
A	0.165	0.172	0.180
A1	0.090	0.105	0.120
A2	0.148	0.152	0.156
B	0.013	0.017	0.021
B1	0.026	0.029	0.032
C	0.008	0.010	0.012
D	0.485	0.490	0.495
D1	0.450	0.453	0.456
D2	0.195	0.210	0.215
E	0.485	0.490	0.495
E1	0.450	0.453	0.456
E2	0.195	0.210	0.215
e	0.050 REF.		

ALL DIMENSIONS ARE IN INCHES.