

STM4470E-VB Datasheet

N-Channel 40-V (D-S) MOSFET

PRODUCT SUMMARY

V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A) ^d	Q _g (Typ.)
40	0.014 at V _{GS} = 10 V	10	15 nC
	0.016 at V _{GS} = 4.5 V	9	

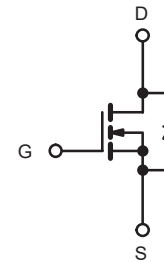
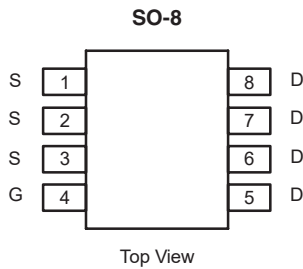
FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET® Power MOSFET
- 100 % R_g Tested
- 100 % UIS Tested
- Compliant to RoHS directive 2002/95/EC



APPLICATIONS

- Synchronous Rectification
- POL, IBC
- Secondary Side



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T_A = 25 °C, unless otherwise noted

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V _{DS}	40	V
Gate-Source Voltage	V _{GS}	± 20	
Continuous Drain Current (T _J = 150 °C)	I _D	T _C = 25 °C	A
		T _C = 70 °C	
		T _A = 25 °C	
		T _A = 70 °C	
Pulsed Drain Current	I _{DM}	50	A
Avalanche Current	I _{AS}	15	
Avalanche Energy	E _{AS}	11	mJ
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C	A
		T _A = 25 °C	
Maximum Power Dissipation	P _D	T _C = 25 °C	W
		T _C = 70 °C	
		T _A = 25 °C	
		T _A = 70 °C	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150	°C

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{a, c}	R _{thJA}	37	50	°C/W
Maximum Junction-to-Foot (Drain)	R _{thJF}	17	21	

Notes:

- Surface Mounted on 1" x 1" FR4 board.
- t = 10 s.
- Maximum under Steady State conditions is 85 °C/W.
- Based on T_C = 25 °C.

SPECIFICATIONS T _J = 25 °C, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	40			V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	I _D = 250 μA		40		mV/°C
V _{GS(th)} Temperature Coefficient	ΔV _{GS(th)} /T _J			- 6		
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	1		3	V
Gate-Source Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 40 V, V _{GS} = 0 V			1	μA
		V _{DS} = 40 V, V _{GS} = 0 V, T _J = 55 °C			5	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	50			A
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 10 V, I _D = 12.4 A		0.014		Ω
		V _{GS} = 4.5 V, I _D = 10.8 A		0.016		
Forward Transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 12.4 A		56		S
Dynamic ^b						
Input Capacitance	C _{iss}	V _{DS} = 20 V, V _{GS} = 0 V, f = 1 MHz		2000		pF
Output Capacitance	C _{oss}			260		
Reverse Transfer Capacitance	C _{rss}			150		
Total Gate Charge	Q _g	V _{DS} = 10 V, V _{GS} = 10 V, I _D = 12.4 A		33	50	nC
		V _{DS} = 10 V, V _{GS} = 4.5 V, I _D = 12.4 A		15	23	
Gate-Source Charge	Q _{gs}			6.7		
Gate-Drain Charge	Q _{gd}			5.1		
Gate Resistance	R _g	f = 1 MHz		1.4	2.1	Ω
Turn-On Delay Time	t _{d(on)}	V _{DD} = 20 V, R _L = 2 Ω I _D ≅ 10 A, V _{GEN} = 4.5 V, R _g = 1 Ω		25	40	ns
Rise Time	t _r			12	20	
Turn-Off Delay Time	t _{d(off)}			25	40	
Fall Time	t _f			10	15	
Turn-On Delay Time	t _{d(on)}	V _{DD} = 20 V, R _L = 2 Ω I _D ≅ 10 A, V _{GEN} = 10 V, R _g = 1 Ω		10	15	
Rise Time	t _r			15	25	
Turn-Off Delay Time	t _{d(off)}			30	45	
Fall Time	t _f			10	15	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C			30	A
Pulse Diode Forward Current	I _{SM}				50	
Body Diode Voltage	V _{SD}	I _S = 10 A, V _{GS} = 0 V		0.8	1.2	V
Body Diode Reverse Recovery Time	t _{rr}	I _F = 10 A, dI/dt = 100 A/μs, T _J = 25 °C		30	60	ns
Body Diode Reverse Recovery Charge	Q _{rr}			26	52	nC
Reverse Recovery Fall Time	t _a			17.5		ns
Reverse Recovery Rise Time	t _b			12.5		

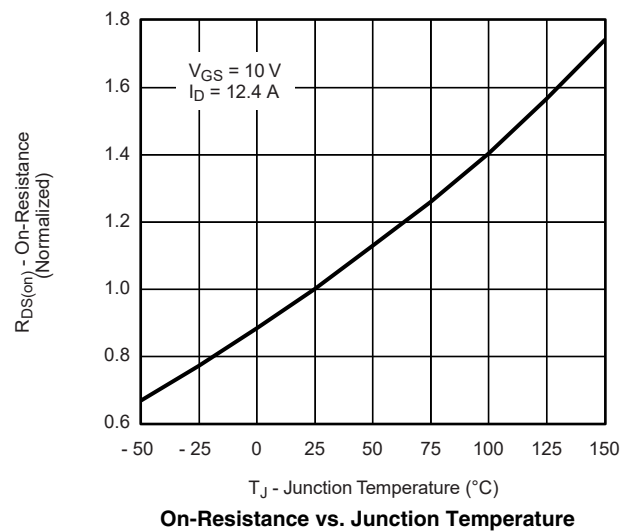
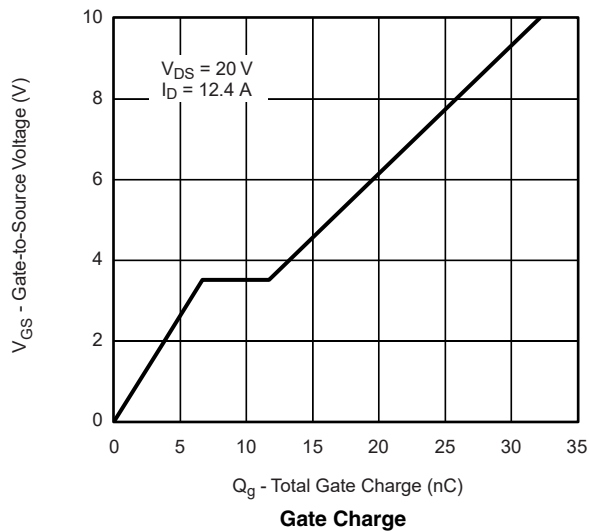
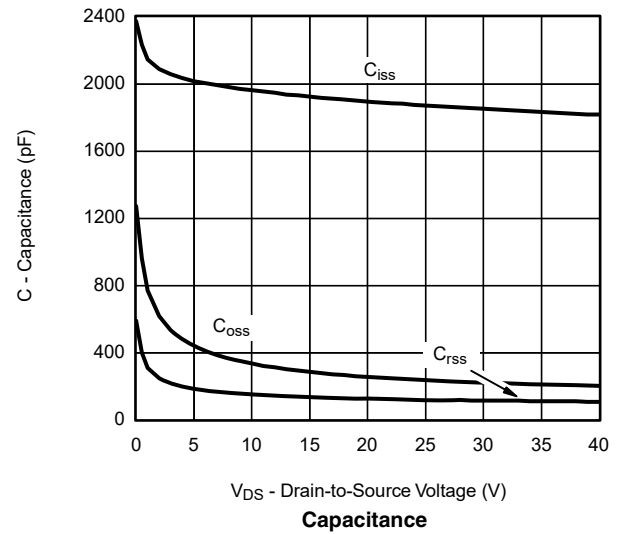
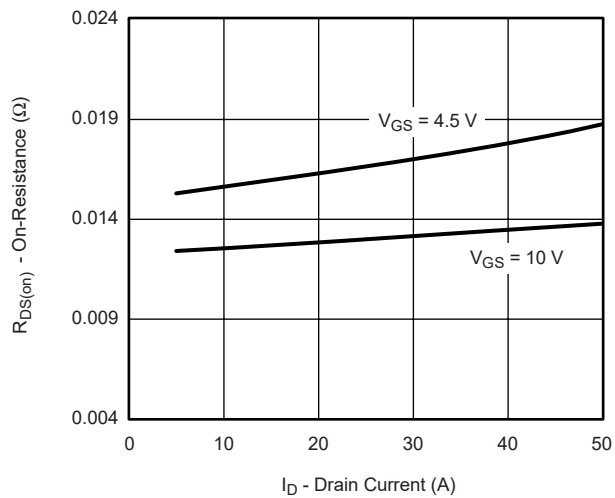
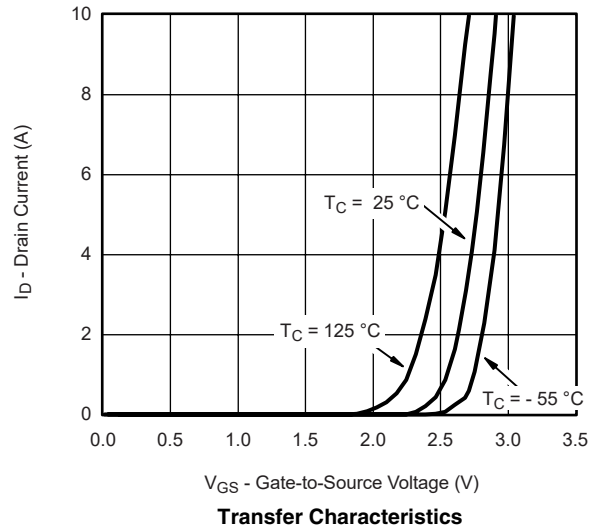
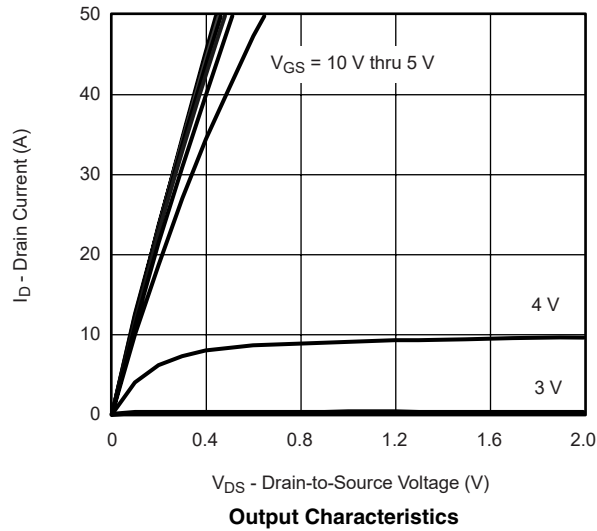
Notes:

a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$

b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

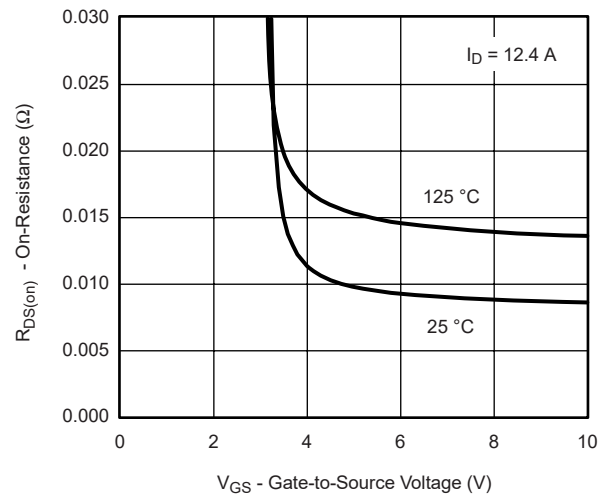
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



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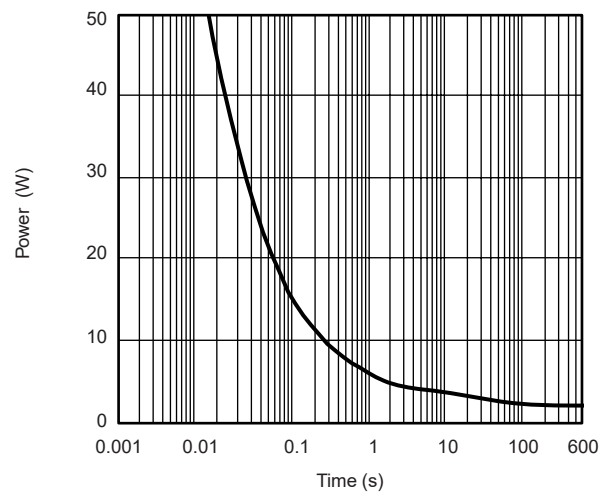
Source-Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

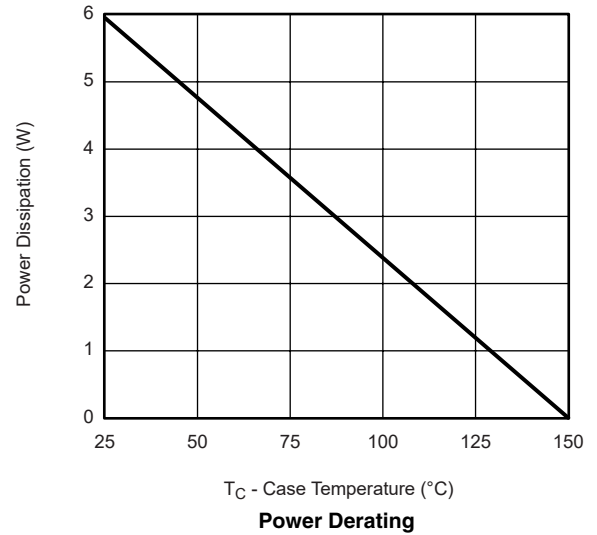
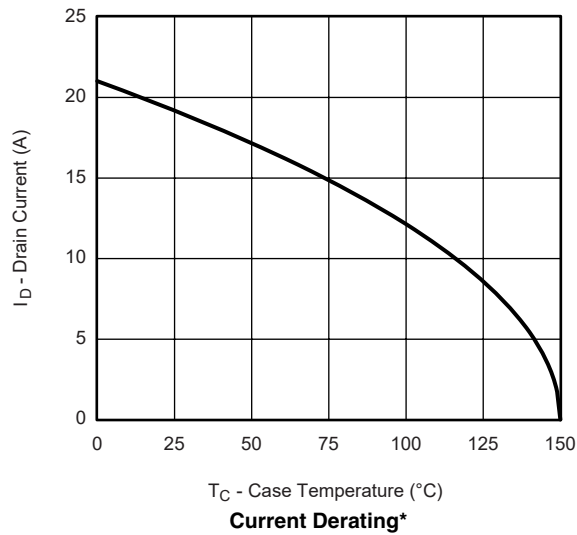


Single Pulse Power (Junction-to-Ambient)



* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Ambient

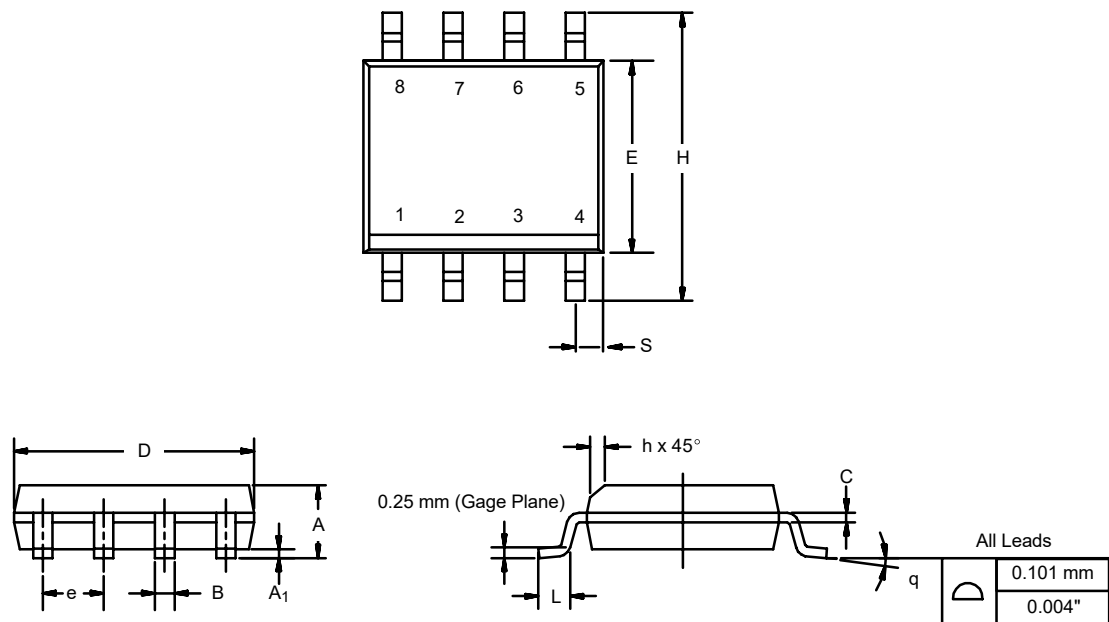
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



SOIC (NARROW): 8-LEAD
JEDEC Part Number: MS-012



DIM	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A ₁	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°
S	0.44	0.64	0.018	0.026
ECN: C-06527-Rev. I, 11-Sep-06				
DWG: 5498				

RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads
Dimensions in Inches/(mm)

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