

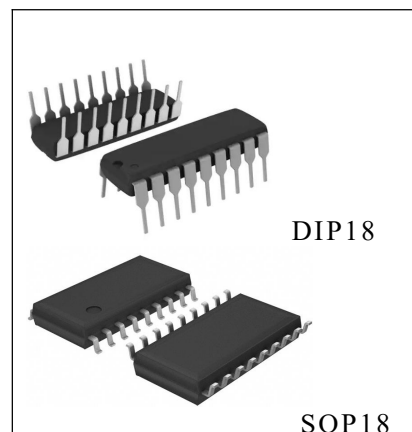
ULN2803

Octal High Voltage, High Current Darlington Transistor Arrays

General Description

The eight NPN Darlington connected transistors in this family of arrays are ideally suited for interfacing between low logic level digital circuitry (such as TTL, CMOS or PMOS/NMOS) and the higher current/voltage requirements of lamps, relays, printer hammers or other similar loads for a broad range of computer, industrial, and consumer applications. All devices feature open-collector outputs and free wheeling clamp diodes for transient suppression

The ULN2803 is designed to be compatible with standard TTL families while the ULN2804 is optimized for 6 to 15 volt high level CMOS or PMOS.



Package Information

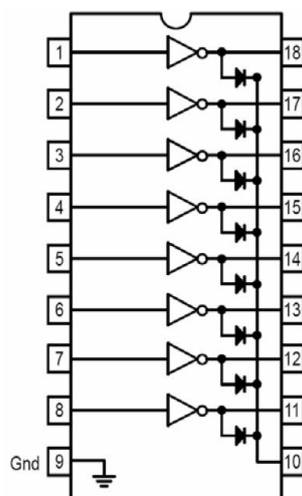
Part NO.	Package Description	Package Marking	Package Option
ULN2803	DIP18	CHMC SXXXX ULN2803	20/Tube
ULN2803F	SOP18	CHMC SXXXX ULN2803F	40/Tube 1500/Reel

CHMC:Trademark

ULN2803/ULN2803F:Part NO.

SXXXX:Lot NO.

Pin Connection



ULN2803(DIP18)/ULN2803F(SOP18)

Absolute Maximum Ratings

($T_A=25^{\circ}\text{C}$ and rating apply to any one device in the package, unless otherwise noted.)

Characteristic		Symbol	Limit	Unit
Output voltage		V_O	50	V
Input voltage		V_I	30	V
Collector current-continuous		I_C	500	mA/ch
Base current-continuous		I_B	25	mA
Clamp diode reverse voltage		V_R	50	V
Clamp diode forward current		I_F	500	mA
Power Dissipation	DIP18	P_D	1.47	W
	SOP18		0.92/1.31(Note)	
Operating temperature		T_{opr}	$-40 \sim +85$	$^{\circ}\text{C}$
Storage temperature		T_{stg}	$-55 \sim +150$	$^{\circ}\text{C}$
Junction temperature		T_J	125	$^{\circ}\text{C}$

Note: 1. On Glass Epoxy PCB ($75 \times 114 \times 1.6 \text{ mm Cu } 20\%$)

2. $R_{\theta JA}=55^{\circ}\text{C/W}$

3. Do not exceed maximum current limit per driver.

Electrical Characteristics ($T_A=25^{\circ}\text{C}$, unless otherwise noted)

Characteristic	Symbol	Test condition	Limit			Unit
			Min.	Typ.	Max.	
Output leakage current (Fig.1)	I_{CEX}	$V_O=50\text{V}, T_A=70^{\circ}\text{C}$			100	μA
		$V_O=50\text{V}, T_A=25^{\circ}\text{C}$			50	
Collector-Emitter saturation voltage(Fig.2)	$V_{CE(sat)}$	$I_C=350\text{mA}, I_B=500\mu\text{A}$		1.1	1.6	V
		$I_C=200\text{mA}, I_B=350\mu\text{A}$		0.95	1.3	
		$I_C=100\text{mA}, I_B=250\mu\text{A}$		0.85	1.1	
Input current-on condition (Fig.4)	$I_{I(on)}$	$V_I=3.85\text{V}$		1.1	1.35	mA
Input voltage-on condition (Fig.5)	$V_{I(on)}$	$V_{CE}=2.0\text{V}, I_C=200\text{mA}$		1.7	2.4	V
		$V_{CE}=2.0\text{V}, I_C=250\text{mA}$		1.75	2.7	
		$V_{CE}=2.0\text{V}, I_C=300\text{mA}$		1.8	3.0	
Input current-off Condition (Fig.3)	$I_{I(off)}$	$I_C=500\mu\text{A}, T_A=70^{\circ}\text{C}$	50	100		μA
Input capacitance	C_I			15	25	pF
Turn-on delay time (50% E_I to 50% E_O)	t_{on}			0.25	1.0	μs
Turn-off delay time (50% E_I to 50% E_O)	t_{off}			0.25	1.0	μs
Clamp diode leakage Current($V_R=50\text{V}$)(Fig.6)	I_R	$T_A=25^{\circ}\text{C}$			50	μA
		$T_A=70^{\circ}\text{C}$			100	
Clamp diode forward Voltage (Fig.7)	V_F	$I_F=350\text{mA}$		1.5	2.0	V

Test Circuit

Figure 1.

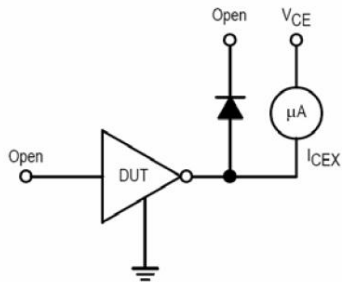


Figure 2.

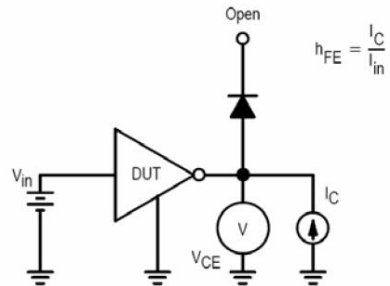


Figure 3.

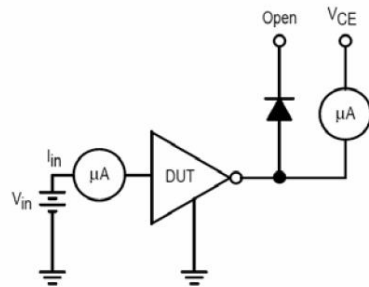


Figure 4.

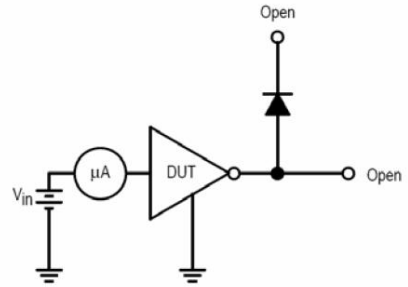


Figure 5.

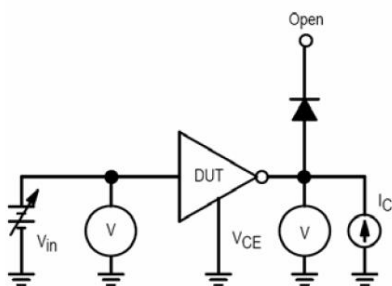


Figure 6.

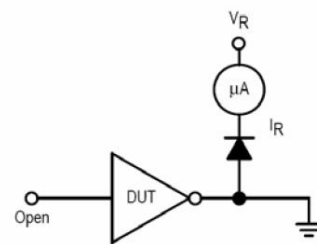
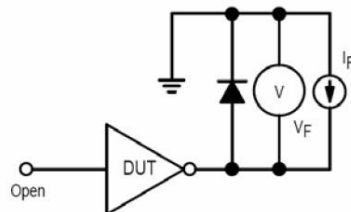
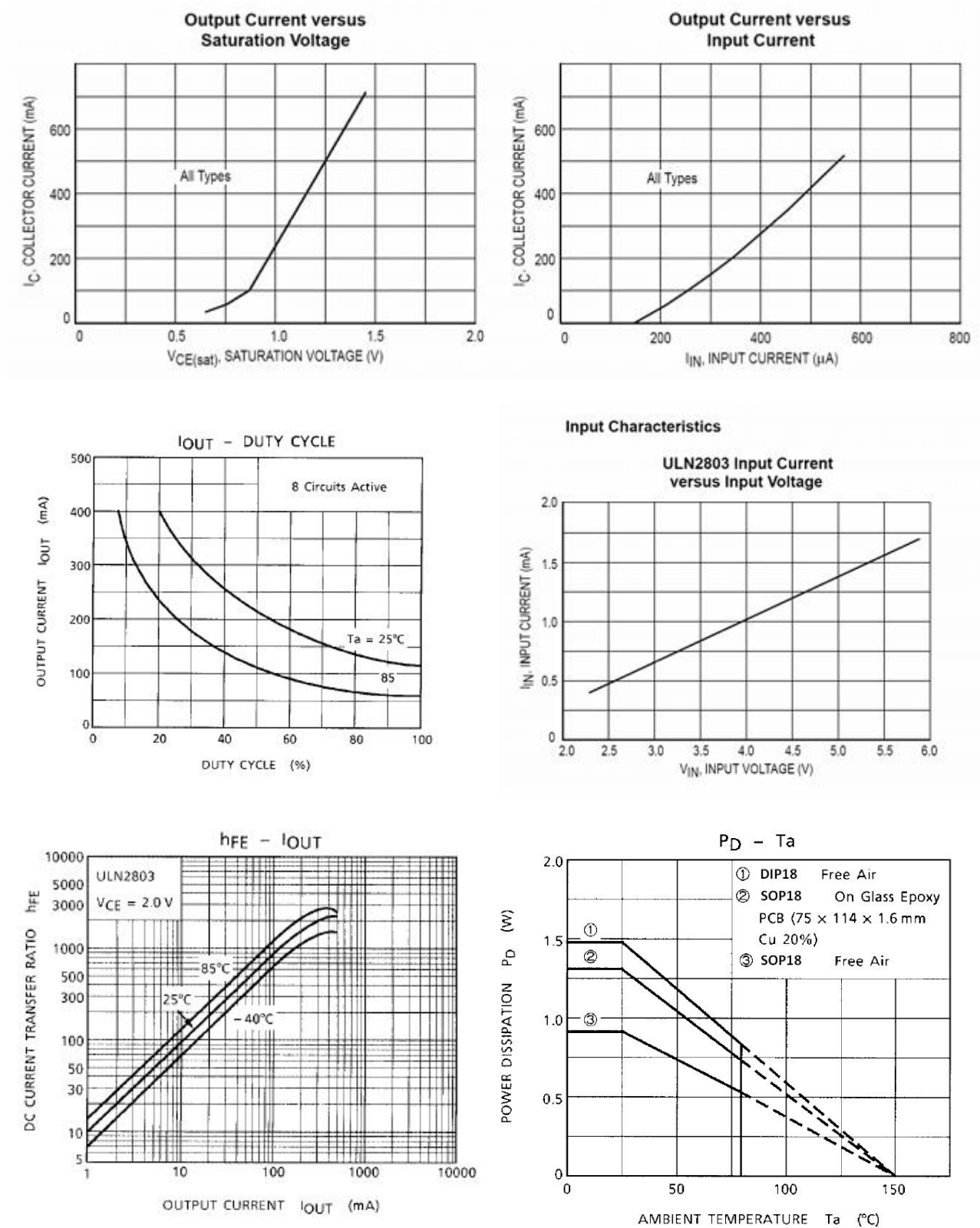
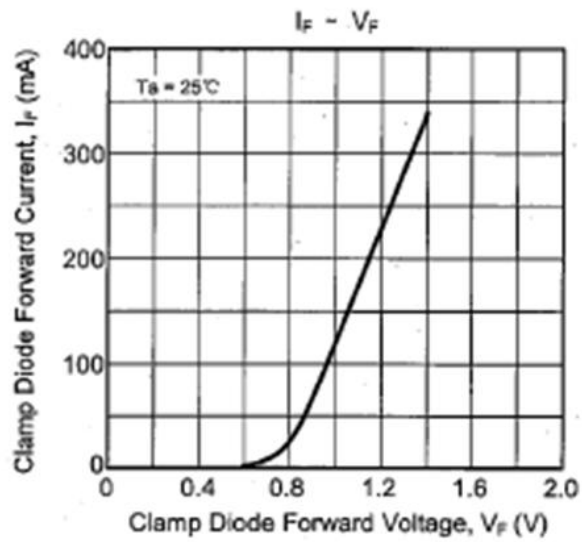


Figure 7.

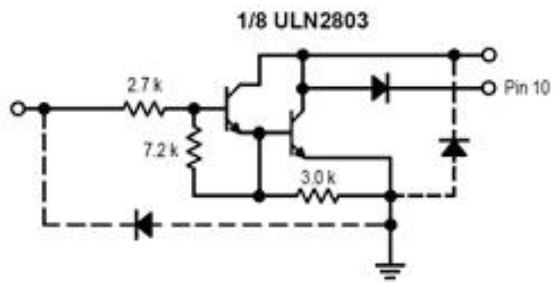


Typical Curve

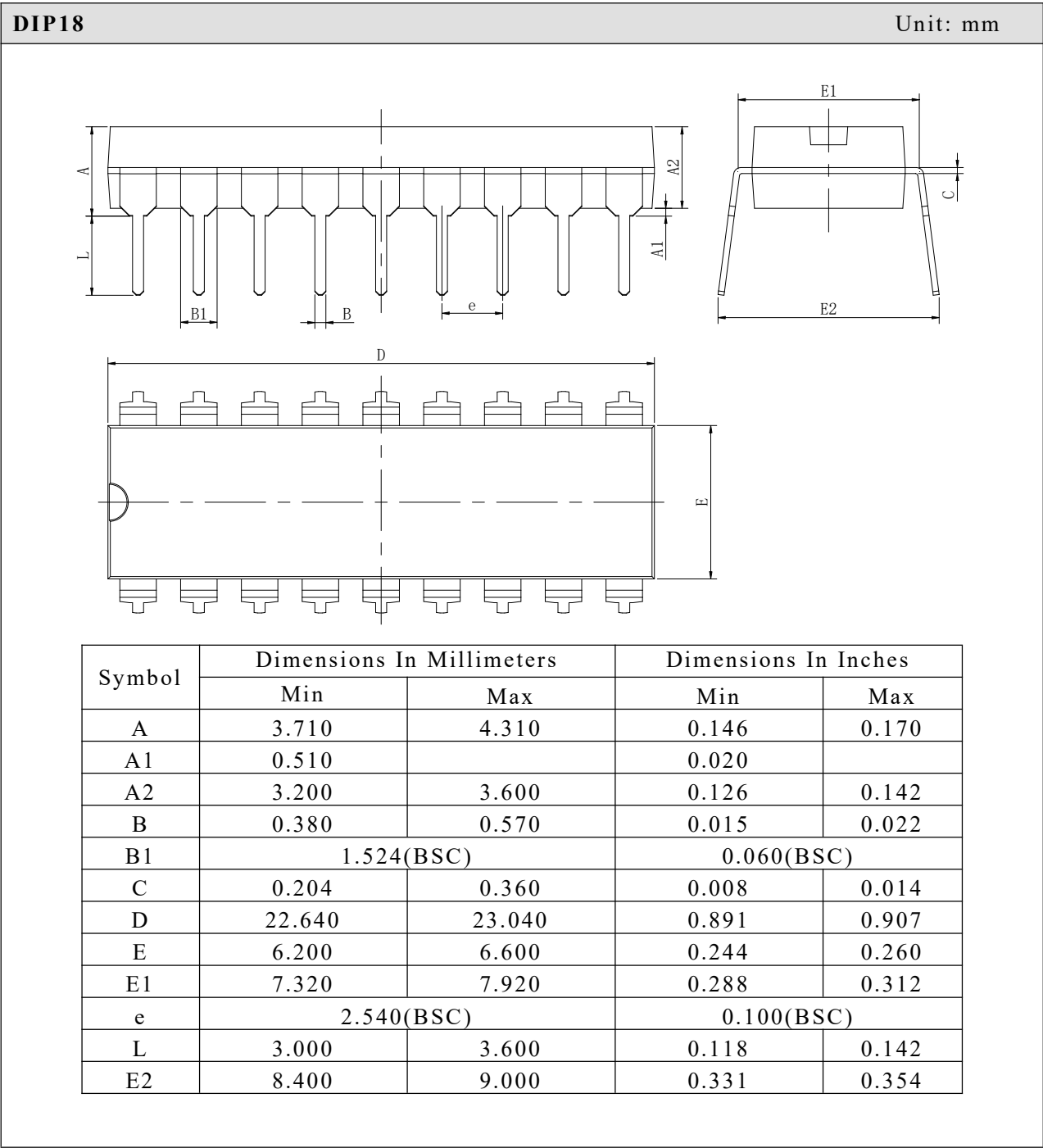




Representative Schematic Diagrams

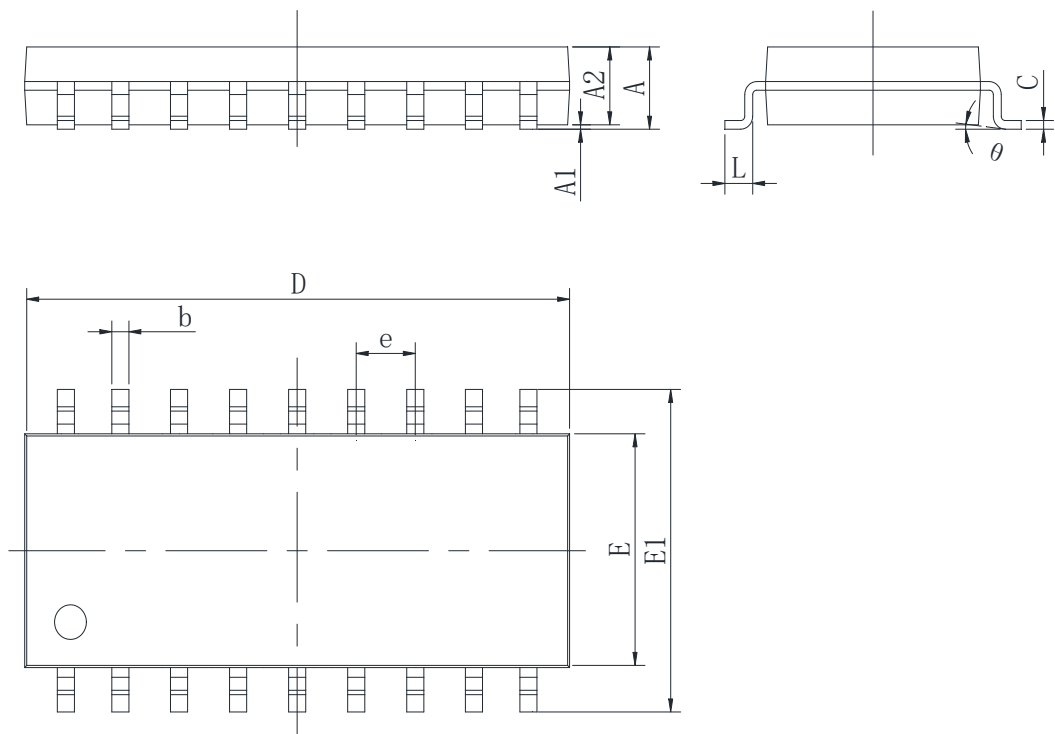


Outline Dimensions



SOP18

Unit: mm



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A		2.650		0.104
A1	0.100	0.300	0.004	0.012
A2	2.100	2.500	0.083	0.098
b	0.330	0.510	0.013	0.020
c	0.204	0.330	0.008	0.013
D	11.250	11.750	0.442	0.462
E	7.400	7.600	0.291	0.299
E1	10.210	10.610	0.402	0.418
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Statements

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