



CD4017

5-stage Johnson Decade Counter

Product Specification

Specification Revision History:

Version	Date	Description
2019-07-A1	2019-07	New
2023-04-B1	2023-04	Update the template



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1、General Description

The CD4017 is a 5-stage Johnson decade counter with ten spike-free decoded active HIGH outputs (Q0 to Q9), an active LOW carry output from the most significant flip-flop ($\overline{Q}5-9$), active HIGH and active LOW clock inputs (CP0, $\overline{CP}1$) and an overriding asynchronous master reset input (MR).

The counter is advanced by either a LOW-to-HIGH transition at CP0 while $\overline{CP}1$ is LOW or a HIGH-to-LOW transition at $\overline{CP}1$ while CP0 is HIGH.

When cascading counters, the $\overline{Q}5-9$ output, which is LOW while the counter is in states 5, 6, 7, 8, and 9, can be used to drive the CP0 input of the next counter. A HIGH on MR resets the counter to zero (Q0= $\overline{Q}5-9$ =HIGH; Q1 to Q9=LOW) independent of the clock inputs (CP0, $\overline{CP}1$).

Automatic counter code correction is provided by an internal circuit: following any illegal code the counter returns to a proper counting mode within 11 clock pulses.

It operates over a recommended V_{DD} power supply range of 3V to 15V referenced to V_{SS} (usually ground). Unused inputs must be connected to V_{DD} , V_{SS} , or another input.

Features:

- Wide supply voltage range from 3V to 15V
- Automatic counter correction
- Tolerant of slow clock rise and fall times
- 5V, 10V, and 15V parametric ratings
- Standardized symmetrical output characteristics
- Specified from -40°C to +125°C
- Packaging information: DIP16/SOP16/TSSOP16

**Ordering Information:****Tube packing specifications:**

Part number	Packaging form	Marking code	Tube quantity	Boxed tube quantity	Boxed quantity	Notes
CD4017DA16.TB	DIP16	CD4017	25 PCS/tube	40 tube/box	1000 PCS/box	Dimensions of plastic enclosure: 19.0mm×6.4mm Pin spacing: 2.54mm
CD4017SA16.TB	SOP16	CD4017	50 PCS/tube	200 tube/box	10000 PCS/box	Dimensions of plastic enclosure: 10.0mm×3.9mm Pin spacing: 1.27mm
CD4017TA16.TB	TSSOP16	CD4017	96 PCS/tube	200 tube/box	19200 PCS/box	Dimensions of plastic enclosure: 5.0mm×4.4mm Pin spacing: 0.65mm

Reel packing specifications:

Part number	Packaging form	Marking code	Reel quantity	Boxed reel quantity	Notes
CD4017SA16.TR	SOP16	CD4017	4000 PCS/reel	8000 PCS/box	Dimensions of plastic enclosure: 10.0mm×3.9mm Pin spacing:1.27mm
CD4017TA16.TR	TSSOP16	CD4017	5000 PCS/reel	10000 PCS/box	Dimensions of plastic enclosure: 5.0mm×4.4mm Pin spacing:0.65mm

Note: If the physical information is inconsistent with the ordering information, please refer to the actual product.



2、Block Diagram And Pin Description

2.1、Block Diagram

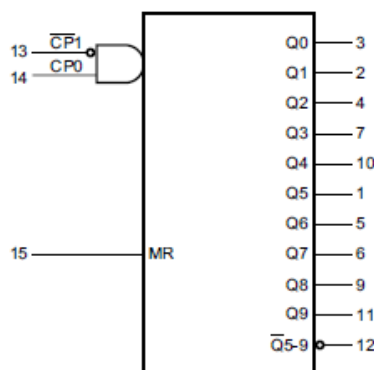


Figure 1. Logic symbol

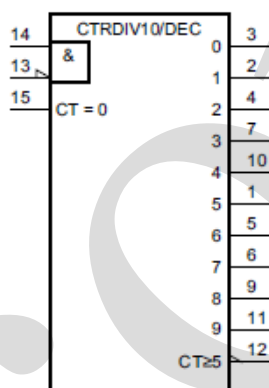


Figure 2. IEE logic symbol

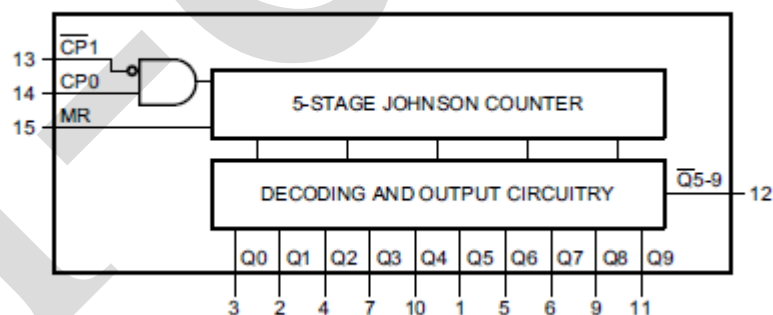


Figure 3. Functional diagram

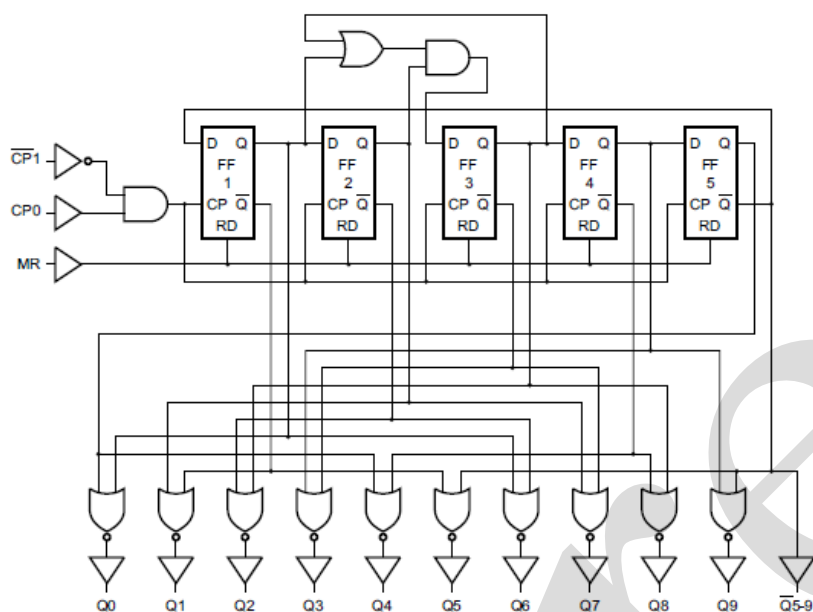


Figure 4. Logic diagram

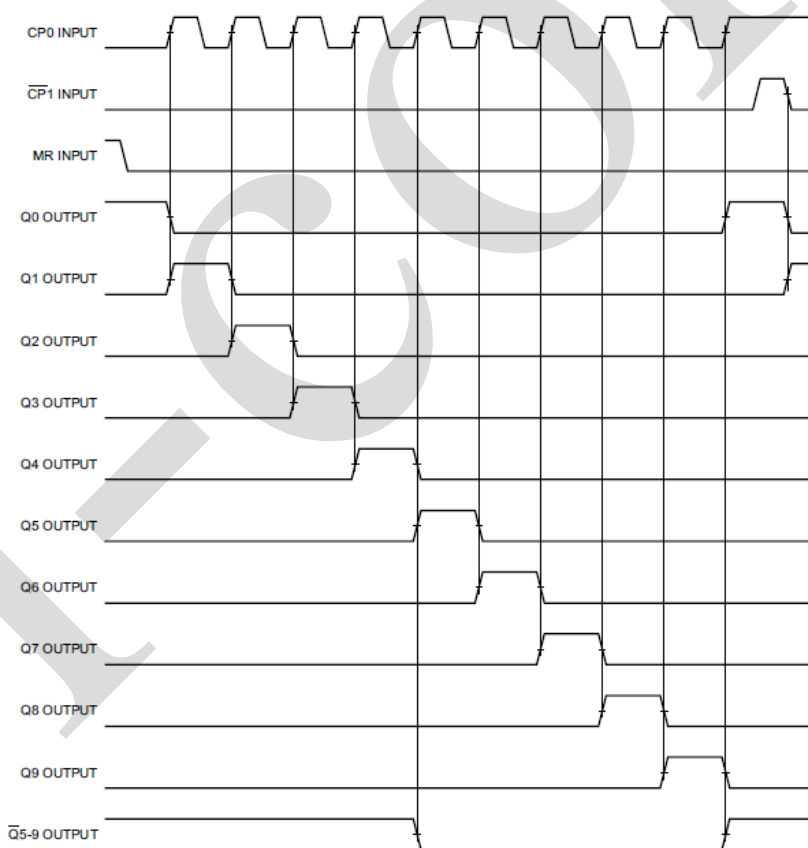
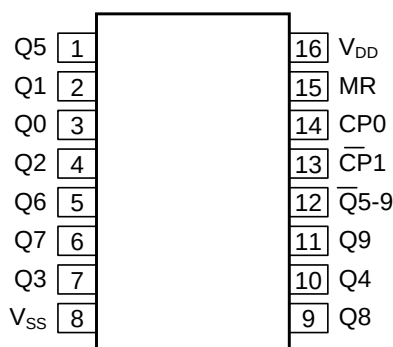


Figure 5. Timing diagram



2.2、Pin Configurations



2.3、Pin Description

Pin No.	Pin Name	Description
1	Q5	decoded output
2	Q1	decoded output
3	Q0	decoded output
4	Q2	decoded output
5	Q6	decoded output
6	Q7	decoded output
7	Q3	decoded output
8	VSS	ground (0V)
9	Q8	decoded output
10	Q4	decoded output
11	Q9	decoded output
12	$\overline{Q5-9}$	carry output (active LOW)
13	$\overline{CP1}$	clock input (HIGH-to-LOW edge-triggered)
14	CP0	clock input (LOW-to-HIGH edge-triggered)
15	MR	master reset input
16	VDD	supply voltage

2.4、Function Table

Input			Operation
MR	CP0	$\overline{CP1}$	
H	X	X	Q0= $\overline{Q5-9}$ =H; Q1 to Q9=L
L	H	↓	counter advances
L	↑	L	counter advances
L	L	X	no change
L	X	H	no change
L	H	↑	no change
L	↓	L	no change

Note:

H=HIGH voltage level; L=LOW voltage level; X=don't care;

↑=positive-going transition; ↓=negative-going transition.



3、Electrical Parameter

3.1、Absolute Maximum Ratings

(Voltages are referenced to V_{SS} (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Max.	Unit
supply voltage	V _{DD}	-		-0.5	+18	V
DC input current	I _{IK}	any one input		-	±10	mA
input voltage	V _I	all inputs		-0.5	V _{DD} +0.5	V
storage temperature	T _{stg}	-		-65	+150	°C
total power dissipation	P _{tot}	-		-	500	mW
device dissipation	P	per output transistor		-	100	mW
Soldering temperature	T _L	10s	DIP	245		°C
			SOP/TSSOP	260		

3.2、Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
supply voltage	V_{DD}	-	3	-	15	V
ambient temperature	T_{amb}	in free air	-40	-	+125	°C
clock input frequency	f_{CL}	$V_{DD}=5V$	-	-	2.5	MHz
		$V_{DD}=10V$	-	-	5	MHz
		$V_{DD}=15V$	-	-	5.5	MHz
clock pulse width	t_w	$V_{DD}=5V$	200	-	-	ns
		$V_{DD}=10V$	90	-	-	ns
		$V_{DD}=15V$	60	-	-	ns
clock rise and fall time	t_{rCL}, t_{fCL}	$V_{DD}=5V$	unlimited			-
		$V_{DD}=10V$				-
		$V_{DD}=15V$				-
clock inhibit setup time	t_s	$V_{DD}=5V$	230	-	-	ns
		$V_{DD}=10V$	100	-	-	ns
		$V_{DD}=15V$	70	-	-	ns
reset pulse width	t_{RW}	$V_{DD}=5V$	260	-	-	ns
		$V_{DD}=10V$	110	-	-	ns
		$V_{DD}=15V$	60	-	-	ns
reset removal time	t_{rec}	$V_{DD}=5V$	400	-	-	ns
		$V_{DD}=10V$	280	-	-	ns
		$V_{DD}=15V$	150	-	-	ns



3.3、Electrical Characteristics

3.3.1、DC Characteristics 1

($T_{amb}=25^{\circ}\text{C}$, voltages are referenced to V_{SS} (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions (V)			$T_{amb}=25^{\circ}\text{C}$			Unit
		V_O	V_{IN}	V_{DD}	Min.	Typ.	Max.	
supply current	I_{DD}	-	0, 5	5	-	-	5	μA
		-	0, 10	10	-	-	10	μA
		-	0, 15	15	-	-	20	μA
LOW-level output current	I_{OL}	0.4	0, 5	5	0.51	1	-	mA
		0.5	0, 10	10	1.3	2.6	-	mA
		1.5	0, 15	15	3.4	6.8	-	mA
HIGH-level output current	I_{OH}	4.6	0, 5	5	-0.51	-1	-	mA
		2.5	0, 5	5	-1.6	-3.2	-	mA
		9.5	0, 10	10	-1.3	-2.6	-	mA
		13.5	0, 15	15	-3.4	-6.8	-	mA
LOW-level output voltage	V_{OL}	-	0, 5	5	-	0	0.05	V
		-	0, 10	10	-	0	0.05	V
		-	0, 15	15	-	0	0.05	V
HIGH-level output voltage	V_{OH}	-	0, 5	5	4.95	5	-	V
		-	0, 10	10	9.95	10	-	V
		-	0, 15	15	14.95	15	-	V
LOW-level input voltage	V_{IL}	0.5, 4.5	-	5	-	-	1.5	V
		1, 9	-	10	-	-	3	V
		1.5, 13.5	-	15	-	-	4	V
HIGH-level input voltage	V_{IH}	0.5, 4.5	-	5	3.5	-	-	V
		1, 9	-	10	7	-	-	V
		1.5, 13.5	-	15	11	-	-	V
input leakage current	I_I	-	0, 15	15	-	-	± 1	μA



3.3.2、DC Characteristics 2

($T_{amb}=-40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, voltages are referenced to V_{SS} (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions (V)			$T_{amb}=-40^{\circ}\text{C}$		$T_{amb}=+85^{\circ}\text{C}$		$T_{amb}=+125^{\circ}\text{C}$		Unit
		V_O	V_{IN}	V_{DD}	Min.	Max.	Min.	Max.	Min.	Max.	
supply current	I_{DD}	-	0, 5	5	-	5	-	150	-	150	μA
		-	0, 10	10	-	10	-	300	-	300	μA
		-	0, 15	15	-	20	-	600	-	600	μA
LOW-level output current	I_{OL}	0.4	0, 5	5	0.61	-	0.42	-	0.36	-	mA
		0.5	0, 10	10	1.5	-	1.1	-	0.9	-	mA
		1.5	0, 15	15	4	-	2.8	-	2.4	-	mA
HIGH-level output current	I_{OH}	4.6	0, 5	5	-0.61	-	-0.42	-	-0.36	-	mA
		2.5	0, 5	5	-1.8	-	-1.3	-	-1.15	-	mA
		9.5	0, 10	10	-1.5	-	-1.1	-	-0.9	-	mA
		13.5	0, 15	15	-4.2	-	-2.8	-	-2.4	-	mA
LOW-level output voltage	V_{OL}	-	0, 5	5	-	0.05	-	0.05	-	0.05	V
		-	0, 10	10	-	0.05	-	0.05	-	0.05	V
		-	0, 15	15	-	0.05	-	0.05	-	0.05	V
HIGH-level output voltage	V_{OH}	-	0, 5	5	4.95	-	4.95	-	4.95	-	V
		-	0, 10	10	9.95	-	9.95	-	9.95	-	V
		-	0, 15	15	14.95	-	14.95	-	14.95	-	V
LOW-level input voltage	V_{IL}	0.5, 4.5	-	5	-	1.5	-	1.5	-	1.5	V
		1, 9	-	10	-	3	-	3	-	3	V
		1.5, 13.5	-	15	-	4	-	4	-	4	V
HIGH-level input voltage	V_{IH}	0.5, 4.5	-	5	3.5	-	3.5	-	3.5	-	V
		1, 9	-	10	7	-	7	-	7	-	V
		1.5, 13.5	-	15	11	-	11	-	11	-	V
input leakage current	I_I	-	0, 15	15	-	± 1	-	± 1	-	± 1	μA



3.3.3、AC Characteristics

($T_{amb}=25^{\circ}\text{C}$, $V_{SS}=0\text{V}$, t_r , $t_f=20\text{ns}$, $C_L=50\text{pF}$, $R_L=200\text{k}\Omega$, unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
propagation delay time	$t_{\text{PHL}}, t_{\text{PLH}}$	CP0, $\overline{\text{CP1}}$ to Q0 to Q9; see Figure 7	$V_{\text{DD}}=5\text{V}$	-	325	650	ns
			$V_{\text{DD}}=10\text{V}$	-	135	270	ns
			$V_{\text{DD}}=15\text{V}$	-	85	170	ns
		CP0, $\overline{\text{CP1}}$ to $\overline{\text{Q5-9}}$; see Figure 7	$V_{\text{DD}}=5\text{V}$	-	300	600	ns
			$V_{\text{DD}}=10\text{V}$	-	125	250	ns
			$V_{\text{DD}}=15\text{V}$	-	80	160	ns
		MR to Q0 to Q9; see Figure 7	$V_{\text{DD}}=5\text{V}$	-	265	530	ns
			$V_{\text{DD}}=10\text{V}$	-	115	230	ns
			$V_{\text{DD}}=15\text{V}$	-	85	170	ns
transition time	t_{t}	see Figure 7	$V_{\text{DD}}=5\text{V}$	-	100	200	ns
			$V_{\text{DD}}=10\text{V}$	-	50	100	ns
			$V_{\text{DD}}=15\text{V}$	-	40	80	ns
pulse width	t_{w}	see Figure 8	$V_{\text{DD}}=5\text{V}$	-	100	200	ns
			$V_{\text{DD}}=10\text{V}$	-	45	90	ns
			$V_{\text{DD}}=15\text{V}$	-	30	60	ns
clock rise and fall time	$t_{\text{rCL}}, t_{\text{fCL}}$	-	$V_{\text{DD}}=5\text{V}$	unlimited			-
			$V_{\text{DD}}=10\text{V}$				-
			$V_{\text{DD}}=15\text{V}$				-
maximum clock frequency	f_{CL}	see Figure 8	$V_{\text{DD}}=5\text{V}$	2.5	5	-	MHz
			$V_{\text{DD}}=10\text{V}$	5	10	-	MHz
			$V_{\text{DD}}=15\text{V}$	5.5	11	-	MHz
setup time	t_{s}	$\text{CP0 to } \overline{\text{CP1}}$; see Figure 9	$V_{\text{DD}}=5\text{V}$	-	115	230	ns
			$V_{\text{DD}}=10\text{V}$	-	50	100	ns
			$V_{\text{DD}}=15\text{V}$	-	35	70	ns
reset removal time	t_{rec}	MR input; see Figure 8	$V_{\text{DD}}=5\text{V}$	-	200	400	ns
			$V_{\text{DD}}=10\text{V}$	-	140	280	ns
			$V_{\text{DD}}=15\text{V}$	-	75	150	ns
input capacitance	C_{I}	any input		-	5	-	pF

Note: t_t is the same as t_{TLH} and t_{THL} .



4、Testing Circuit

4.1、AC Testing Circuit

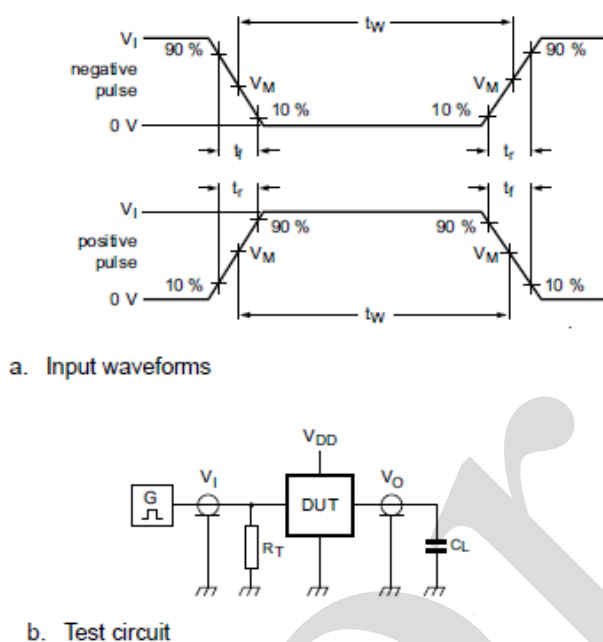


Figure 6. Test circuit for switching times

Definitions for test circuit:

DUT=Device Under Test.

C_L =Load capacitance including jig and probe capacitance.

R_T =Termination resistance should be equal to the output impedance Z_o of the pulse generator.

4.2、AC Testing Waveforms

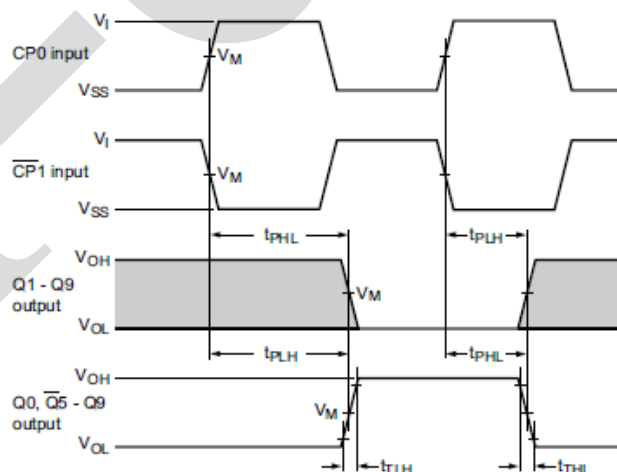


Figure 7. Waveforms showing the propagation delays for CP0, CP1 to Qn, Q5-9 outputs and the output transition times

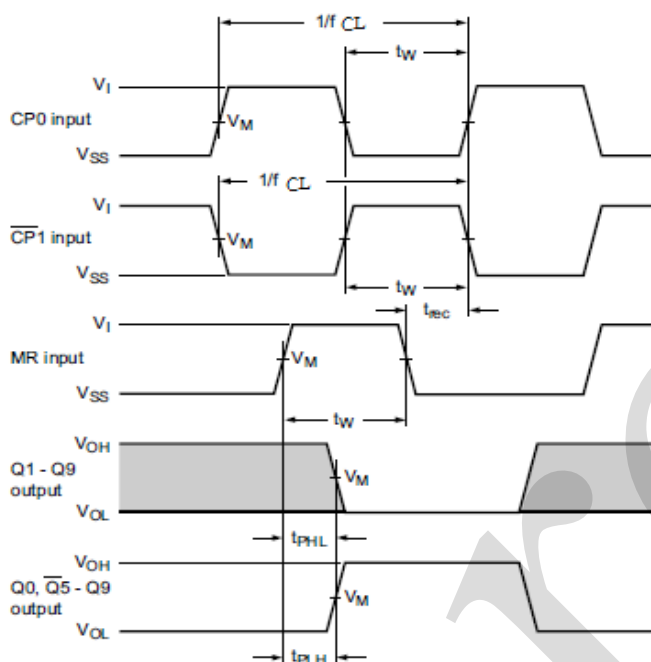


Figure 8. Waveforms showing the minimum pulse width for CP0, $\overline{\text{CP1}}$ and MR input; the maximum frequency for CP0 and $\overline{\text{CP1}}$ input; the recovery time for MR and the MR input to Qn and $\overline{\text{Q5-9}}$ output propagation delay

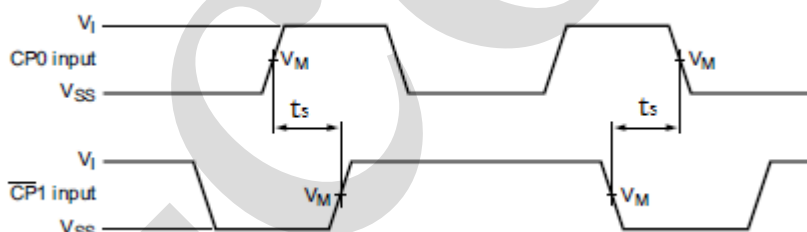


Figure 9. Waveforms showing hold times for CP0 to $\overline{\text{CP1}}$ and $\overline{\text{CP1}}$ to CP0

4.3、 Measurement Points

Supply voltage	Input	Output
V_{DD}	V_M	V_M
5V to 15V	$0.5 \times V_{DD}$	$0.5 \times V_{DD}$

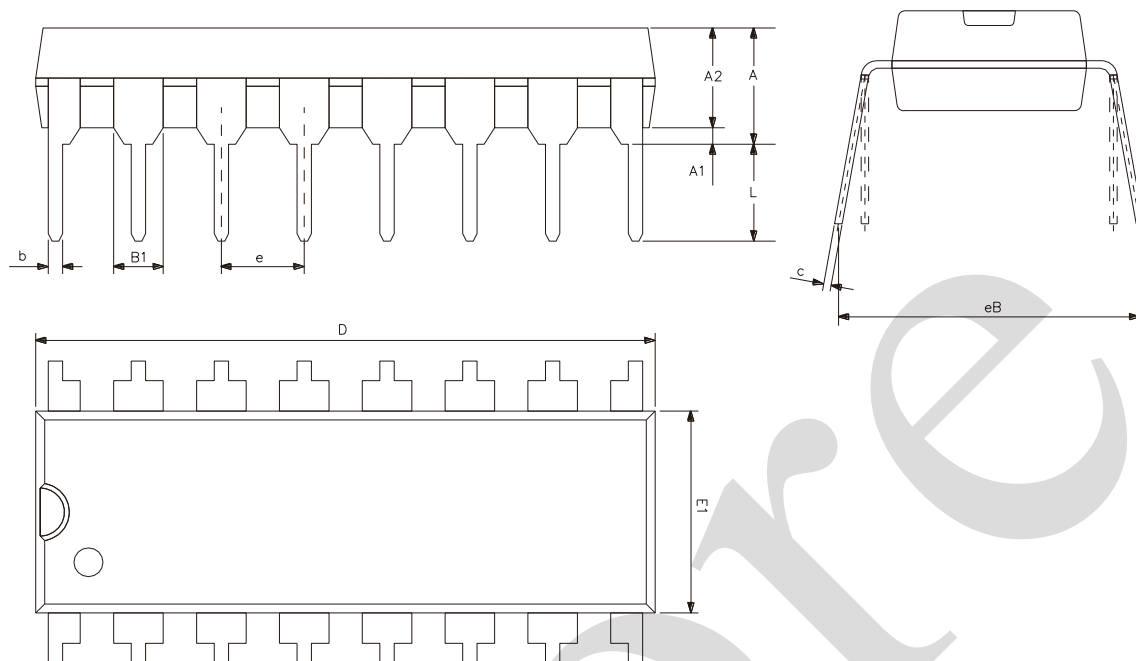
4.4、 Test Data

Supply voltage	Input		Load
V_{DD}	V_I	t_r, t_f	C_L
5V to 15V	V_{SS} or V_{DD}	$\leq 20\text{ns}$	50pF



5、Package Information

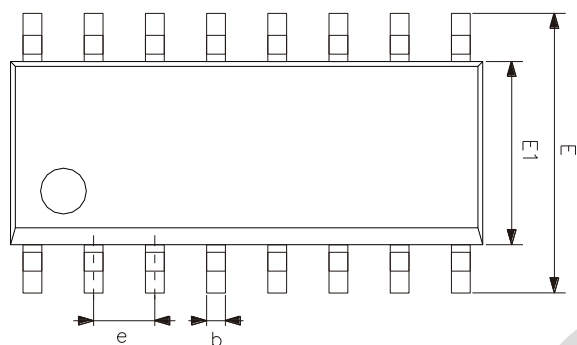
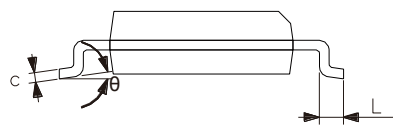
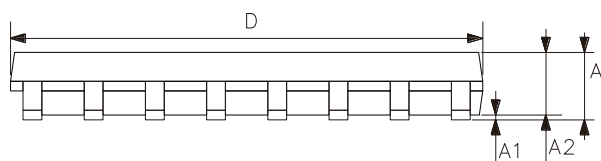
5.1、DIP16



Symbol	Dimensions (mm)	
	Min.	Max.
A2	3.20	3.60
A1	0.51	-
A	3.60	5.33
L	3.00	3.60
b	0.36	0.56
B1	1.52	
D	18.80	19.94
E1	6.20	6.60
e	2.54	
c	0.20	0.36
eB	7.62	9.30



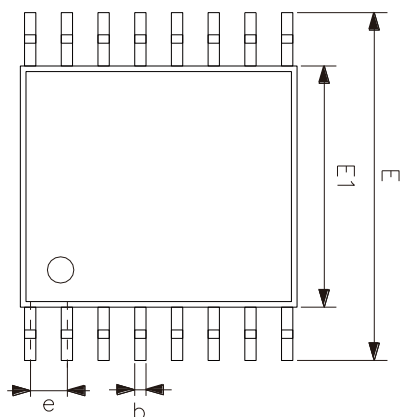
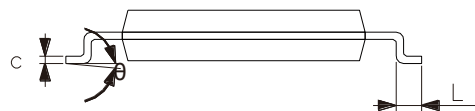
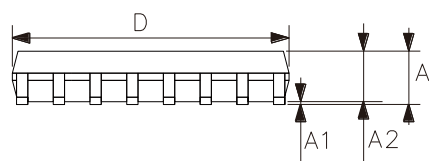
5.2、SOP16



Symbol	Dimensions (mm)	
	Min.	Max.
A	1.35	1.80
A1	0.10	0.25
A2	1.25	1.55
b	0.33	0.51
c	0.19	0.25
D	9.50	10.10
E	5.80	6.30
E1	3.70	4.10
e	1.27	
L	0.35	0.89
θ	0°	8°



5.3、TSSOP16



Symbol	Dimensions (mm)	
	Min.	Max.
A	-	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	4.90	5.10
E1	4.30	4.50
E	6.20	6.60
e	0.65	
L	0.45	0.75
θ	0°	8°



6、Statements And Notes

6.1、The name and content of Hazardous substances or Elements in the product

Part name	Hazardous substances or Elements									
	Lead and lead compounds	Mercury and mercury compounds	Cadmium and cadmium compounds	Hexavalent chromium compounds	Polybrominated biphenyls	Polybrominated biphenyl ethers	Dibutyl phthalate	Butylbenzyl phthalate	Di-2-ethylhexyl phthalate	Diisobutyl phthalate
Lead frame	○	○	○	○	○	○	○	○	○	○
Plastic resin	○	○	○	○	○	○	○	○	○	○
Chip	○	○	○	○	○	○	○	○	○	○
The lead	○	○	○	○	○	○	○	○	○	○
Plastic sheet installed	○	○	○	○	○	○	○	○	○	○
explanation	○: Indicates that the content of hazardous substances or elements in the detection limit of the following the SJ/T11363-2006 standard. ×: Indicates that the content of hazardous substances or elements exceeding the SJ/T11363-2006 Standard limit requirements.									

6.2、Notes

We Recommend you to read this chapter carefully before using this product.

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