SIG1230A: 10/80SPS, 20-bit Sigma-Delta ADC with PGA

FEATURES

PGA Gain: 64 or 128
Data Rates: 10SPS or 80SPS
RMS Noise: 32nV at 10SPS
Offset Drift: 10nV/°C
Gain Drift: 2ppm/°C
Internal or External Clock
Parity Check
Power Supply
AVDD: 2.7V to 5.25V
DVDD: 2.7V to 5.25V
Current: 0.8mA
Package: 16-lead TSSOP

APPLICATIONS

Weigh Scales
Strain Gauges
Pressure Sensors
Industrial Process Control

DESCRIPTION

The SIG1230A is a low noise, low drift, and high-resolution 20-bit analog-to-digital converter (ADC) with integrated programmable gain amplifier (PGA) that offers high-accuracy measurement solutions for bridge sensors.

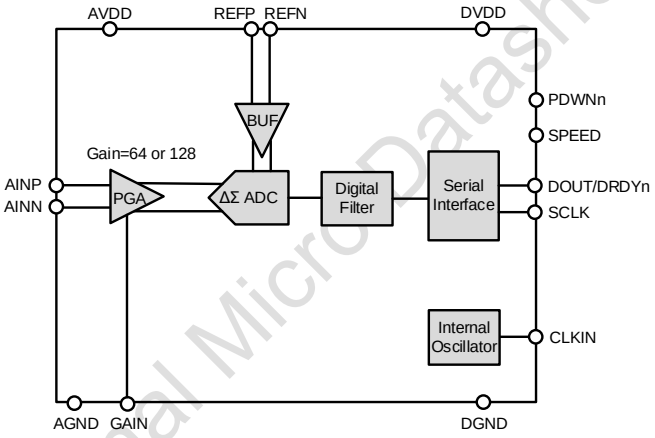
The device contains a low noise PGA with gains selected from 64 or 128, a delta-sigma (Δ-Σ) modulator, and a SINC4 digital filter. Two data rates are provided from the device: 10SPS and 80SPS.

SPI-compatible interface is used for device configuration and parity check is provided for data integrity.

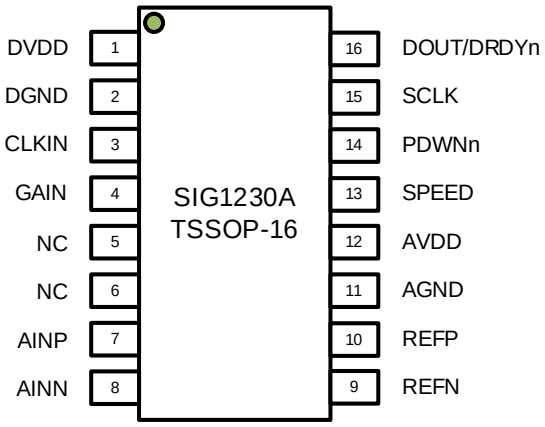
The on-chip oscillator or an external clock can be used as the clock source to the device.

The SIG1230A is available in 16-lead TSSOP package and is fully specified over the -40°C to +125°C temperature range.

Function Block Diagram

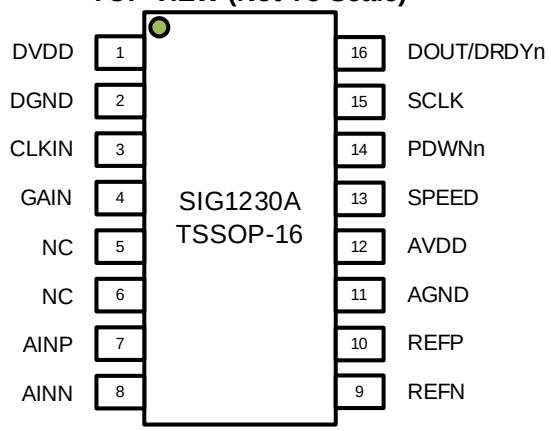


TSSOP-16



PIN CONFIGURATION and DESCRIPTIONS

TOP VIEW (Not To Scale)



PIN		FUNCTION	DESCRIPTION
NO.	NAME		
1	DVDD	Digital	Digital power supply, 2.7V to 5.25V.
2	DGND	Digital	Digital ground reference point.
3	CLKIN	Digital Input	1) Internal oscillator: Connect to DGND. 2) External clock: Connect to external clock input.
4	GAIN	Digital Input	PGA gain control: DGND for gain=64 and DVDD for gain=128. Gain=64 if float.
5	NC	Digital	No connection (float) or connect to DVDD/DGND.
6	NC	Digital	No connection (float) or connect to DVDD/DGND.
7	AINP	Analog Input	Positive analog input.
8	AINN	Analog Input	Negative analog input.
9	REFN	Analog Input	Negative reference input.
10	REFP	Analog Input	Positive reference input.
11	AVSS	Analog	Negative analog power supply.
12	AVDD	Analog	Positive analog power supply. 2.7V to 5.25V relative to AVSS.
13	SPEED	Digital Input	Date rate select: DGND for 10SPS and DVDD for 80SPS.
14	PDWNn	Digital Input	Power-Down signal. Active low. ADC enters power-down mode if holding pin low.
15	SCLK	Digital Input	Serial data clock.
16	DOUT/DRDYn	Digital Output	Serial data output and data ready indicator.

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKING OPTION
SIG1230A	TSSOP-16	-40°C to +125°C	SIG1230A-ITSP16-RL	Reel, 5000

SPECIFICATIONS

Absolute Maximum Ratings

Over operating free-air temperature range, unless otherwise noted.(1)

		MIN	MAX	UNIT
Voltage	AVDD to AVSS	–0.3	6.5	V
	AVSS to DGND	–0.3	0.3	V
	DVDD to DGND	–0.3	6.5	V
	Analog input	V_{AVSS} – 0.3	V_{AVDD} + 0.3	V
	Digital input	V_{DGND} – 0.3	V_{DVDD} + 0.3	V
Current	Input current	–10	10	mA
Temperature	Junction (T_J)	–50	150	°C
	Storage (T_{stg})	-60	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD Ratings

SYMBOL	PARAMTER	CONDITION	VALUE	UNIT
HBM	Human-body Model	ANSI/ESDA/JEDEC JS-001	±4000	V
CDM	Charged-device model	JEDEC EIA/JS-002-2022	±2000	V

This integrated circuit can be damaged by ESD. Signal Micro recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

Electrical Characteristics

Minimum/Maximum specifications apply from -40˚C to +125˚C. Typical specifications are at +25˚C. All specification are at V_{AVDD}=5V, V_{AVSS}=0V, V_{DVDD}=3.3V, V_{REF}=5V, f_{CLK}=1.536MHz, data rate=10SPS, unless otherwise noted.

PARAMETER	TEST CONDITION OR NOTES	MIN(1)	TYP	MAX(1)	UNITS
ANALOG INPUTS					
Differential Input Voltage	$V_{IN} = V_{INP} – V_{INN}$	$–0.5·V_{REF}$/Gain		$+0.5·V_{REF}$/Gain	V
Absolute Input Voltage		V_{AVSS} + 0.5		V_{AVDD} – 0.5	V
Common Mode Input Range		V_{AVSS} + 0.5 + $\|V_{INMAX}\|$·Gain		V_{AVDD} – 0.5 – $\|V_{INMAX}\|$·Gain	V
Absolute Input Current			±1		nA
SYSTEM PERFORMANCE					
PGA Gain			64/128		V/V
Resolution			20		Bits
Data Rate			10/80		SPS
Noise			See Noise Table 1		
Integral Nonlinearity (INL)			±15		ppm
Offset Error			±2		µV
Offset Drift vs. Temperature			±10		nV/°C
Gain Error			±0.3		%
Gain Drift vs. Temperature		-5	±2	+5	ppm/°C
Normal Mode Rejection (NMRR)	f_{IN}=50/60Hz, ±2%,	100	110		dB
Common Mode Rejection (CMRR)	f_{IN}=50/60Hz	100	120		dB
Power Supply Rejection(2) (PSRR)	AVDD	75	90		dB
	DVDD	80	120		dB
REFERENCE INPUT					
Differential Reference Voltage (V_{REF})	$V_{REF} = V_{REFP} – V_{REFN}$	0.5		$V_{AVDD} – V_{AVSS}$ + 0.1	V
Absolute Negative Reference Voltage (V_{REFN})		V_{AVSS} – 0.05		V_{REFP} – 0.5	V
Absolute Positive Reference Voltage (V_{REFP})		V_{REFN} + 0.5		V_{AVDD} + 0.05	V
Average Voltage Input Current			75		nA
ADC CLOCK					
External Clock	Frequency Range	1	1.536	1.6	MHz
	Duty Cycle	40%		60%	
Internal Oscillator	Nominal Frequency		1.536		MHz
	Accuracy	–3%	±0.5%	3%	
DIGITAL INPUT/OUTPUT					
High-level Output Voltage (V_{OH})	I_{OH} = 4mA	$0.8·V_{DVDD}$			V
Low-level Output Voltage (V_{OL})	I_{OL} = –4mA			$0.2·V_{DVDD}$	V
High-level Input Voltage (V_{IH})		$0.7·V_{DVDD}$		V_{DVDD}	V
Low-level Input Voltage (V_{IL})		V_{DGND}		$0.3·V_{DVDD}$	V
Input Hysteresis			0.5		V
Input Leakage				±10	µA
POWER SUPPLY					
AVSS Voltage (V_{AVSS})			0		V
AVDD Voltage (V_{AVDD})		2.7		5.25	V
DVDD Voltage (V_{DVDD})		2.7		5.25	V
AVDD, AVSS Current (I_{AVDD})	Normal Mode		0.6	0.8	mA
	Standby Mode		1		µA
	Power-Down		1		µA

DVDD Current (I_{DVDD})	Normal Mode		170	230	µA
	Standby Mode		20		µA
	Power-Down		1		µA
Total Power Dissipation AVSS Voltage (V_{AVSS})	Normal Mode		3.5		mW
	Standby Mode		0.1		mW
	Power-Down		0.01		mW
TEMPERATURE RANGE					
Specified temperature range		–40		125	°C
Operating temperature range		–50		125	°C
Storage temperature range		–60		150	°C

(1) Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
(2) Power supply rejection is specified DC change in voltage.

Timing Requirements: Serial Interface

Over the operating ambient temperature range and DVDD = 2.7V to 5.25V, unless otherwise noted.

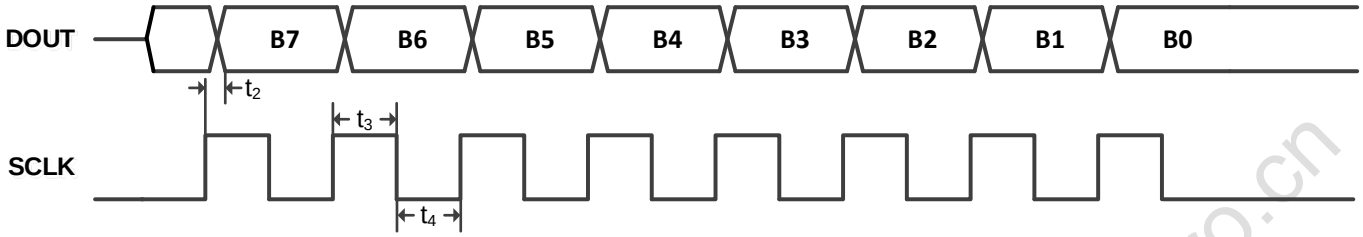


Figure 1. Serial Interface Timing Requirements

SYMBOL	DESCRIPTION	MIN	MAX	UNIT
t_2	SCLK rising edge to valid DOUT/DRDYn: propagation delay(1)		50	ns
t_3	SCLK high pulse width	200		ns
t_4	SCLK low pulse width	200		ns
	SCLK period	400	10^6	ns

(1) DOUT load = 20pF || 100kΩ to DGND.

NOISE PERFORMANCE

Table 1 and Table 2 show ADC noise performance in root mean square (RMS) value, peak-to-peak values, effective number of bits (ENOB), and noise-free bits. The ENOB and noise-free bits listed in the tables are calculated using Equation (1) and Equation (2):

$$\text{ENOB} = \log_2(\mathbf{0.5} \cdot V_{REF}/\text{Gain}/V_{RMS}) \quad (1)$$

$$\text{Noise Free Bits} = \log_2(\mathbf{0.5} \cdot V_{REF}/\text{Gain}/V_{p\text{-}p}) \quad (2)$$

The noise data listed in the table are typical and are generated from continuous ADC readings with differential input voltage of 0 V.

Table 1. ADC Noise in μVRMS (μVPP) at T_A = 25°C, V_{AVDD} = 5 V, V_{REF} = 5 V

Data Rate	Gain	RMS Noise(nV)	Peak-to-Peak Noise(nV)	ENOB(RMS)	Noise-Free Bits
10SPS	64	40	222	20.9	18.4
10SPS	128	32	149	20.2	18.0
80SPS	64	100	595	19.6	17.0
80SPS	128	85	483	18.8	16.3

Table 2. ADC Noise in μVRMS (μVPP) at T_A = 25°C, V_{AVDD} = 3 V, V_{REF} = 3 V

Data Rate	Gain	RMS Noise(nV)	Peak-to-Peak Noise(nV)	ENOB(RMS)	Noise-Free Bits
10SPS	64	40	222	20.2	17.7
10SPS	128	32	149	19.5	17.3
80SPS	64	100	595	18.8	16.3
80SPS	128	85	483	18.1	15.6

REVISION HISTORY

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

DATE	REVISION	CHANGE
May. 20, 2022		Initial release.

DISCLAIMER

Signal Micro reserves the right to make any change in circuit design, specification or other related things if necessary without notice at any time.

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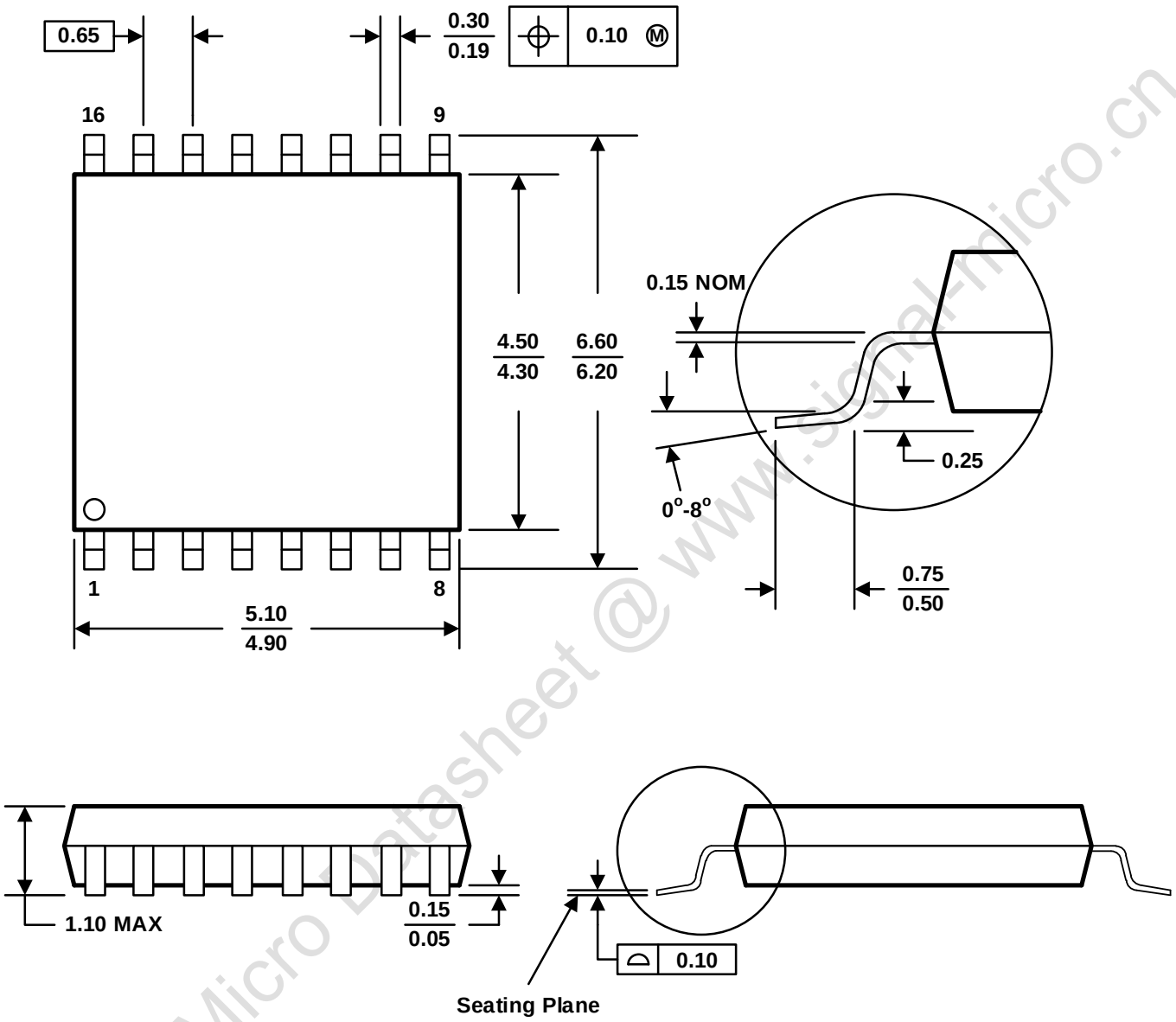
PACKAGE OUTLINE DIMENSIONS



A. Compliant to JEDEC STARDARDS MO-153-AD.
B. All linear dimensions are in millimeters.
C. This drawing is subject to change without notice.