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BCM84891L

10GBASE-T/5GBASE-T/2.5GBASE-T/1000BASE-T/100BASE-TX Transceiver

General Description

The Broadcom® BCM84891L is a single 10GBASE-T/5GBASE-T/2.5GBASE-T/1000BASE-T/100BASE-TX Ethernet CMOS transceiver. The device performs all physical-layer functions for 10GBASE-T, 5GBASE-T, 2.5GBASE-T, 1000BASE-T, and 100BASE-TX Ethernet on Category 6, 6A, or 7 twisted-pair cable. The 5GBASE-T, 2.5GBASE-T, 1000BASE-T, and 100BASE-TX can operate on standard Category 5e UTP. The BCM84891L supports the XFI/10GBASE-KR, USXGMII, 5000BASE-R, 2500BASE-R, 5000BASE-X, 2500BASE-X, and 1000BASE-X (SGMII) interface for connection to a MAC. The BCM84891L is a highly integrated solution that combines digital adaptive equalizers, ADCs, phase-locked loops, line drivers, encoders, decoders, echo cancelers, crosstalk cancelers, and all the required support circuitry.

The BCM84891L features the Energy Efficient Ethernet (EEE) protocol. EEE enables the BCM84891L to auto-negotiate and operate with EEE-compliant link partners to reduce overall system power during low utilization of the link. Broadcom's AutogrEEEn® mode permits legacy systems to enjoy the power saving benefits of EEE.

The BCM84891L automatically negotiates an operating speed with any transceiver on the opposite end of the line. The BCM84891L features Enhanced Cable Diagnostics, which detects common cable problems such as shorts, opens, and cable length.

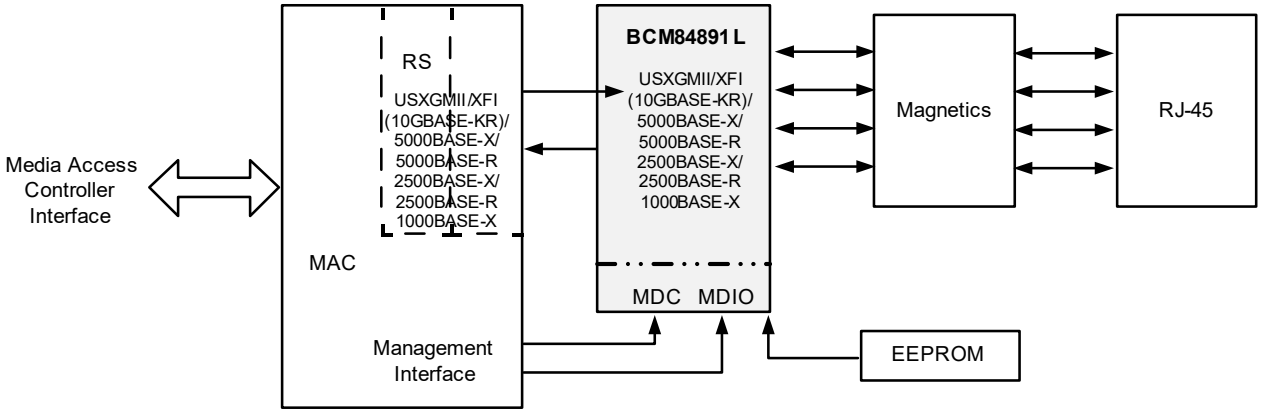
Applications

- 10-Gigabit Ethernet (GbE) switches and uplinks
- 10GbE server adapter
- 10GbE host control

Features

- Single-chip integrated single Ethernet transceiver-MAC to magnetics:
  - 10GBASE-T IEEE 802.3an
  - 5GBASE-T IEEE 802.3bz
  - 2.5GBASE-T IEEE 802.3bz
  - 1000BASE-T IEEE 802.3ab
  - 100BASE-TX IEEE 802.3u
- IEEE 802.3z
- IEEE 802.3az
- XFI/10GBASE-KR, USXGMII, 5000BASE-X, 2500BASE-X, 5000BASE-R, 2500BASE-R, and 1000BASE-X (SGMII) MAC Interface
- 5G rate over USXGMII/XFI/5000BASE-R/5000BASE-X MAC interface
- 2.5G rate over USXGMII/XFI/2500BASE-R/2500BASE-X MAC interface
- IEEE 1588-2008 version 2-compliant
- IEEE fast retrain and link monitoring
- EEE on 10GBASE-T, 5GBASE-T, 2.5GBASE-T, 1000BASE-T, and 100BASE-TX Auto-sense mode
- Trace matched output impedance
- Line-side loopback
- Low electromagnetic interference (EMI) emissions
- Enhanced cable diagnostics
- Support for jumbo packets up to 18 KB
- Detection and correction of pair swaps (MDI crossover), pair skew, and pair polarity
- Auto-negotiation with next page support
- IEEE 1149.1 (JTAG) and IEEE 1149.6 (ACJTAG) boundary scan support
- Low-power, 0.8V CMOS core
- 1.2V, 2.5V, or 3.3V MDIO I/O, 1.8V CMOS I/O
- Device package: 8 mm × 8 mm BGA

Figure 1: Functional Block Diagram



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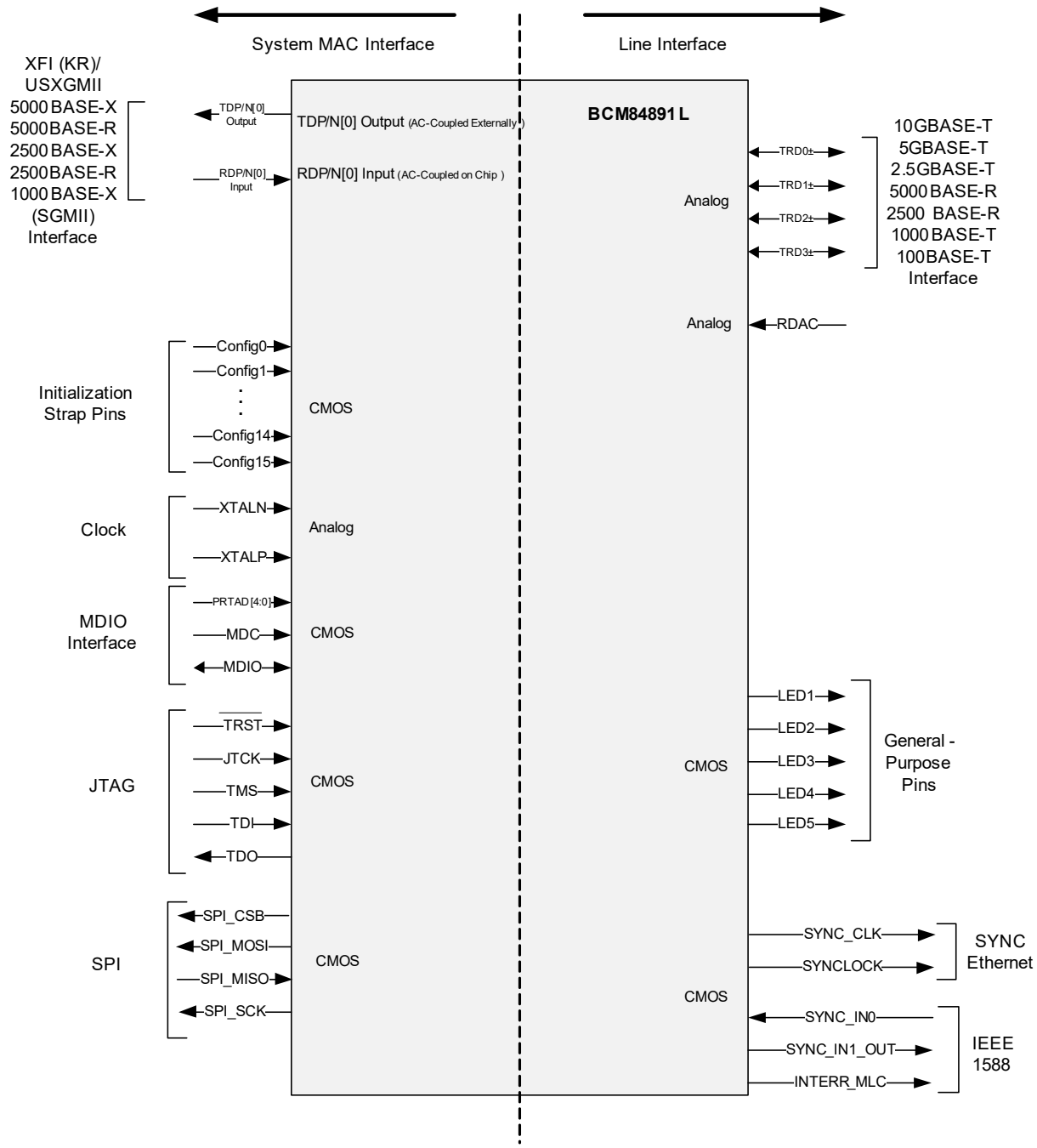
Chapter 1: Functional Description

1.1 Overview

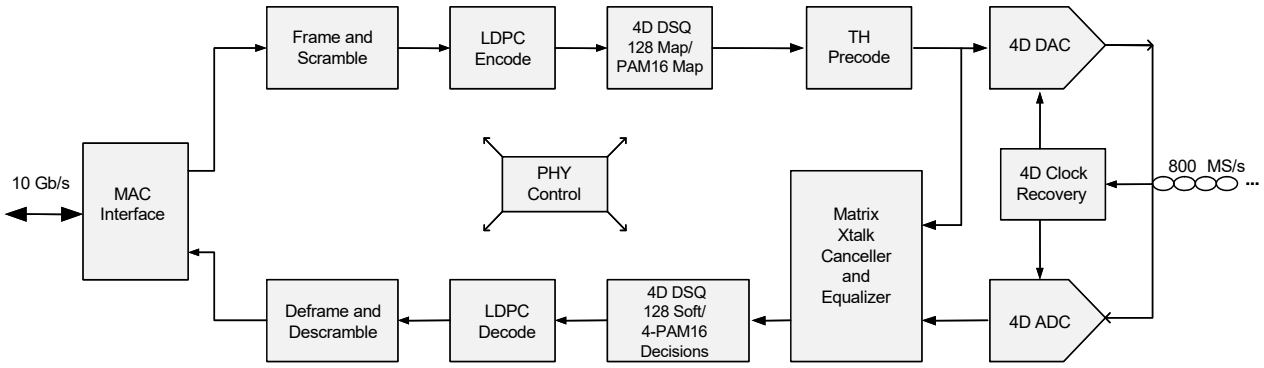
The figure below shows the system MAC and line interface on the BCM84891L.

Figure 2: Interface Block Diagram Per-Port



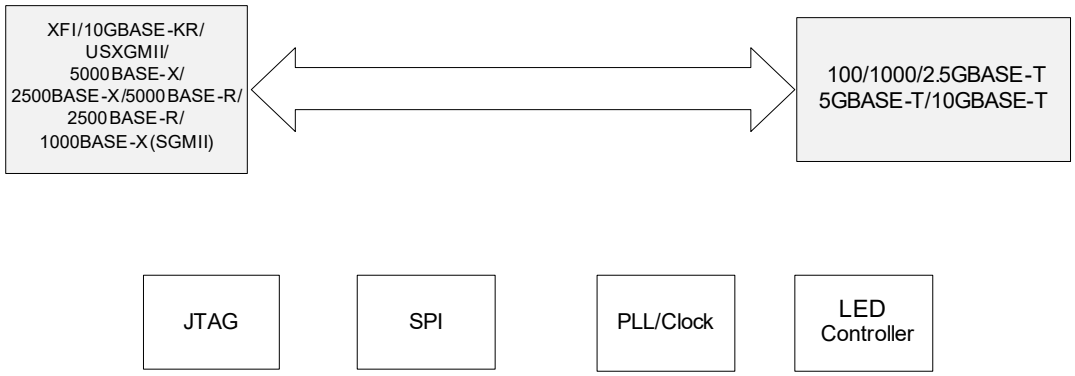
The figure below shows the major 10G/5G/2.5GBASE-T functions of the BCM84891L. 15867339858

Figure 3: BCM84891L 10GBASE-T/5G/2.5GBASE-T Block Diagram



The figure below shows the BCM84891L data path block diagram.

Figure 4: Data Path Block Diagram



1.2 Device Functions

The BCM84891L is a 10GBASE-T/1000BASE-T/100BASE-TX transceiver that performs all the physical layer (PHY) interface function for 10GBASE-T, 1000BASE-T, 100BASE-T Ethernet on Category 6, 6A, or 7 twisted-pair cable. 5GBASE-T, 2.5GBASE-T, 1000BASE-T, and 100BASE-TX operations are supported on Category 5e UTP. The BCM84891L connects to a Media Access Controller (MAC) or switch controller through XFI/10GBASE-KR or USXGMII for 10GBASE-T, USXGMII, 5000BASE-X, 5000BASE-R, or 5G rate over XFI for 5GBASE-T USXGMII, 2500BASE-X, 2500BASE-R, or 2.5G rate over XFI for 2.5GBASE-T and USXGMII, 1000BASE-X (SGMII) for 1000BASE-T/100BASE-TX.

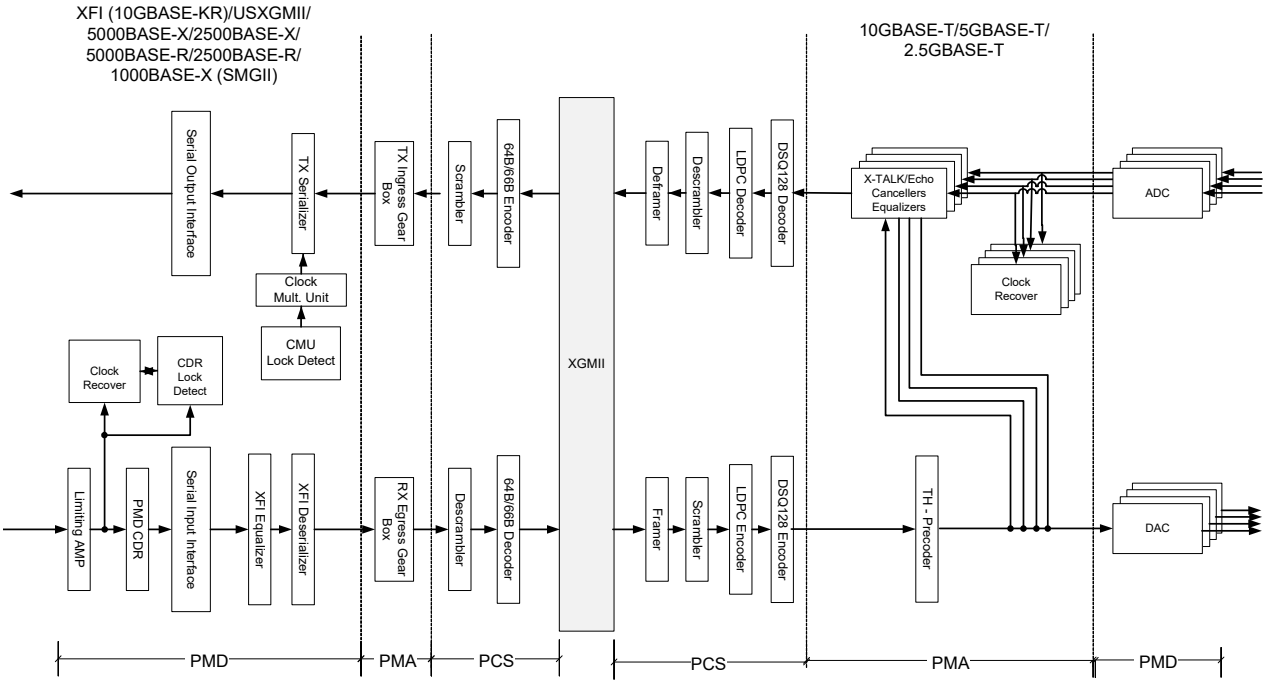
The device is fully compliant with the IEEE 802.3 standard for 10GBASE-T, 1000BASE-T, and 100BASE-T. Operation of 5GBASE-T and 2.5GBASE-T are compliant to IEEE 802.3bz. It connects to twisted-pair wiring of the network through isolation transformers. The BCM84891L can be programmed to auto-negotiate its operating speed based on the capabilities advertised by the link partner.

The BCM84891L device adheres to Broadcom's quality procedures and meets or exceeds the performance and functionality tested as part of a comprehensive product characterization, qualification, and functional verification process.

1.3 Operation Modes

The BCM84891L supports XFI/USXGMII/5000BASE-X/2500BASE-X/1000BASE-X (SGMII)-to-Copper (10GBASE-T/5GBASE-T/2.5GBASE-T/1000BASE-T/100BASE-TX). Figure 5 shows the supported configuration for the XFI/USXGMII/5000BASE-X/2500BASE-X/1000BASE-X (SGMII)-to-Copper operation mode.

Figure 5: Functional Block Architecture for the XFI (10GBASE-KR)/2500BASE-X/1000BASE-X(SGMII)-to-Copper Configuration



1.4 10GBASE-T

The BCM84891L supports the 10GBASE-T transmission rate, per the IEEE P802.3an standard.

1.4.1 Transmit Path

The transmitter path collects the 64-bit parallel data stream at the XGMII interface and reformats the data into 10GBASE-T/1000BASE-T over four twisted-pairs.

1.4.1.1 Scramble and Frame

Scrambling or randomizing of the transmit data is necessary to minimize baseline wander and ensure proper operation of adaptive receiver subsystems, such as clock recovery and equalization. All data entering the PHY is scrambled by a 58-bit self-synchronizing scrambler. With continuous 10 Gb/s operation, this scrambler does not repeat more often than once every 55 years.

PHY-level frames are not visible to higher layers but are necessary to allow for proper synchronization and alignment of Low-Density Parity-Check (LDPC) blocks between the transmitter and receiver. PHY-level frames contain data from 50 consecutive 65-bit XGMII data/control blocks. A CRC-8 is computed across 50 × 65 = 3250 bits and appended to the frame. One additional bit is added for vendor-specific purposes, bringing the total PHY-level frame payload to (1 + 50) × (65 + 8) = 3259 bits.

1.4.1.2 LDPC Encode

A low-density parity check code is an error correcting code, a method of transmitting a message over a noisy transmission channel. The BCM84891L adds 325 parity bits to blocks of 1723 data bits. This block encoding operation is equivalent to a matrix multiplication of c = xG, where x is a 1723-bit input vector [x0, x1, …, x1772], c is a 2048 output code vector [c0, c1, …, c2043], and G is the code generator matrix.

From the PHY frame payload of 3259 bits, 1723 bits are encoded by the LDPC encoder and 1536 bits remain uncoded. The 325 parity bits are added to the 3259-bit payload for a total encoded PHY frame size of 3584 bits. Code block boundaries are recovered at the receiver through PHY frame boundaries.

1.4.1.3 DSQ128 Map (10GBASE-T)

The 3584 bit encoded PHY frame contains 3584 ÷ 7 = 512, 7-bit DSQ128 symbols. Each 7-bit symbol maps to a single point in a two-dimensional symbol constellation. Each DSQ128 symbol is transmitted in two consecutive sample intervals: first the I value, then the Q value. The I-Q ordering is aligned with the PHY frame boundary so that it can be recovered by the receiver. Each 512 symbol PHY frame is divided across four-wire pairs. In each symbol interval, four symbols are transmitted in parallel across the four wires: either four I values or four Q values.

1.4.1.4 PAM16 Mapping (IEEE 802.3bz)

The 2048 bit encoded PHY frame contains 2048 ÷ 4 = 512, 4-bit gray-coded PAM16 symbols. Each 4-bit symbol maps to a single point in a one-dimensional symbol constellation. The frame structure for 2.5G and 5G modes are identical except the symbol duration is 320 ns and 640 ns for 5G and 2.5G, respectively. Each 512 symbol PHY frame is divided across four-wire pairs. In each symbol interval, four PAM16 symbols are transmitted in parallel across the four wires.

1.4.1.5 Tomlinson-Harashima Precode

Each dimension (four I values or four Q values) of the four channel symbols from the 4D DSQ128 mapper is passed through a Tomlinson-Harashima Precoder (THP). The THP is similar in structure to a Decision-Feedback Equalizer (DFE), but it is used in the transmitter rather than the receiver to avoid DFE error propagation issues. The coefficient values for the THP are determined as part of the link start-up sequence and remain fixed during data transfer.

1.4.1.6 DAC

Each of the four outputs from the precoders are converted to an analog signal using integrated digital-to-analog converters (DAC). The DAC drives the 100Ω twisted-pair cable (through a transformer) with a differential signal. The average transmit power is 4.2 dBm for 100m (or greater) cables and backs off in value as the cable length is reduced.

1.4.2 Receive Path

The receiver path accepts 10GBASE-T framing over four twisted-pairs and reformats the data into a 64-bit parallel data stream at the XGMII interface.

1.4.2.1 Four-Channel ADC

The signal received on each of the four wire pairs is converted to a digital representation by integrated analog-to-digital converters (ADC).

1.4.2.2 Clock Recovery

The optimal sampling instant for each of the four ADCs is determined by the clock recovery circuit. In slave mode, the frequency and phase are derived from the received data, so that the slave is frequency- and phase-locked with the master.

1.4.2.3 Matrix Crosstalk Canceler and Equalizer

The major cancellable/suppressible signal impairments are crosstalk within and between the four-wire pairs and intersymbol interference (ISI) caused by the insertion loss of a wire pair. Each receiver processes crosstalk from four local transmitters: three transmitters couple through near-end crosstalk (NEXT) channels and one transmitter (on the same wire) couple through the echo channel (echo is caused by the non-ideal return loss of the various components of the channel). The four crosstalk sources per each of the four receivers result in a 4x4 matrix crosstalk channel connecting the four local transmitters to the four local receivers. Adaptive matrix crosstalk cancellation removes the crosstalk from the signal. The matrix crosstalk canceler continuously adapts to track changes in the crosstalk and echo channels.

Each local receiver is connected to a remote transmitter by a direct channel (the wire) and to three other remote transmitters by crosstalk channels. These are also called far-end crosstalk (FEXT) channels. This arrangement operates as a 4x4 matrix channel connecting the four local receivers to the four remote transmitters. Adaptive matrix equalization counters the effects of the matrix signal channel. The matrix equalizer continuously adapts to track changes in the FEXT and ISI channels.

1.4.2.4 Echo Canceler

Because of simultaneous bidirectional transmission of data on each cable pair in 10G/5G/2.5GBASE-T, echo impairments from the local transmitters are present at each receiver. A digital echo canceler subtracts an estimate of the echo from the received signal. The digital echo canceler coefficients are adaptive to track the varying echo transfer function caused by different channels, transmitters, cable geometry, and environmental conditions.

1.4.2.5 Four-Channel DSQ128 Soft LDP Decision and LDPC Decoder (10GBASE-T)

The objective of matrix equalization, matrix crosstalk cancellation, and clock recovery processes is to reconstruct, as closely as possible, the original DSQ128 symbol transmitted by the link partner. The LDPC decoding algorithm uses soft decision decoding to greatly aid the correct detection of a block of received symbols.

At the transmitter, the LDPC encoder combines with the DSQ128 symbol mapper to set the LDPC block (PHY frame) of data sent. The LDPC decoder uses soft decisions to recover the LDPC block data sent. DSQ128 symbols are demapped into 7-bit data. A CRC-8 is computed across the recovered data bits in each PHY frame and compared to the transmitted value to detect block errors.

1.4.2.6 Four-Channel PAM16 Soft LDP Decision and LDPC Decoder (IEEE 802.3bz)

The objective of the matrix equalization, matrix crosstalk cancellation, and the clock recovery processes is to reconstruct, as closely as possible similar to 10GBASE-T, where the original PAM16 symbol is transmitted by the link partner. The LDPC decoding algorithm uses soft decision decoding to greatly aid the correct detection of a block of received symbols.

At the transmitter, the LDPC encoder combines with the PAM16 symbol mapper to set the LDPC block (PHY frame) of data sent. The LDPC decoder uses soft decisions to recover the LDPC block data sent. PAM16 symbols are demapped into 4-bit data.

1.4.2.7 Deframe and Descramble

After LDPC decoding, PHY-level framing is no longer required as PHY-level frames are not visible to higher layers. All non-payload bits are removed by the deframing operation prior to transmission to the MAC. Each recovered PHY-level frame contains sufficient payload data to create 50 consecutive 65-bit XGMII data/control blocks. The recovered payload data bits are descrambled with the same 58-bit scrambler polynomial used at the transmitter. The device uses a side-stream scrambler that is synchronized by the Physical Coding Sublayer (PCS) receive block.

1.5 XFI (10GBASE-KR)/USXGMII/5000BASE-X/2500BASE-X/ 5000BASE-R/2500BASE-R

The XFI (10GBASE-KR)/5000BASE-X/2500BASE-X/5000BASE-R/2500BASE-R is a high-speed serial interface with fully integrated 10 Gb/2.5 Gb/1 Gb serial Ethernet PCS and Physical Media Attachment (PMA) functions. It includes 64-bit/66-bit coding and 8B/10B coding, block scrambling, a Clock Multiplication Unit (CMU), and Clock and Data Recovery (CDR). The XFI (10GBASE-KR) interface adheres to INF-8077i SFF standard.

NOTE: 10GBASE-KR mode is disabled as default. When KR mode is enabled through the command handler, 5000BASE-X/2500BASE-X is not supported and the user should enable 2.5 Gb rate over the XFI interface signals in 10GBASE-KR mode.

1.5.1 Transmit Path

At the XGMII interface, the XFI (10GBASE-KR) receives data that is transmitted serially towards the MAC side (the system side). Data gets 64-bit/66-bit encoded, then scrambled before being transmitted.

1.5.1.1 64-Bit/66-Bit Encoder

The PCS on the XFI (10GBASE-KR) side encodes 64-bit data into 66-bit blocks and inserts the necessary control codes required for transmission across the communication link. The encoding, defined by the IEEE 802.3ae clause 49 for transmission code, ensures sufficient transitions are present in the PHY bit stream to make clock recovery possible at the receiver.

1.5.1.1.1 Scrambler

Data blocks received from the 64-bit/66-bit encoder are passed through a scrambler polynomial and then passed onto the gearbox.

1.5.1.2 XFI (10GBASE-KR) Ingress TX Gearbox

The TX gearbox is a buffer that prepares the 66-bit block data for efficient serialization in the PMA sublayer.

1.5.1.3 XFI (10GBASE-KR) Ingress TX Serializer

Data is read out of the gearbox and then converted to a 10.3125 Gb/s serial stream and driven off-chip. Bit 0 of frame 0 (LSB) is shifted out first.

1.5.1.4 XFI (10GBASE-KR) Clock Multiplication Unit

The XFI (10GBASE-KR) CMU has a PLL that generates the 10.3125/3.125 GHz clock by multiplying the external reference clock (either 50 MHz or 156.25 MHz).

1.5.1.5 XFI (10GBASE-KR) CMU Lock Detect

The BCM84891L contains a lock detect circuit, which monitors the frequency of the internal VCO.

1.5.1.6 XFI (10GBASE-KR) CMOS Differential Serial Output Interface

The CMOS differential serial outputs (XFI_OP/N) must be AC-coupled. The CMOS differential outputs are powered at +1.0V. These high-speed CMOS differential outputs consist of a differential pair designed to drive a 100Ω differential transmission line. The output driver is back terminated to 50Ω on-chip, to snub any reflections.

Provisions are provided through the Management Interface for deactivating the output transmitter by transmitting a constant logical low level (0) at the XFI (10GBASE-KR) output.

NOTE: CMOS differential output drivers do not have on-chip built-in AC-Coupling. External AC-coupling should be used to drive the receiver input device. AC-coupling prevents voltage drops across the input devices of the receiver when the input signals are sourced from a device with a higher operating voltage.

The CMOS differential output includes a four-tap (pre, main, post1, and post2 cursor) preemphasis control. To configure a port with a particular preemphasis setting, see Table 1. To use typical values for the XFI/10GBASE-KR transmit preemphasis, no special register setting or command is required.

Figure 6: Preemphasis with Repeating Pattern of Four 1s and Four 0s

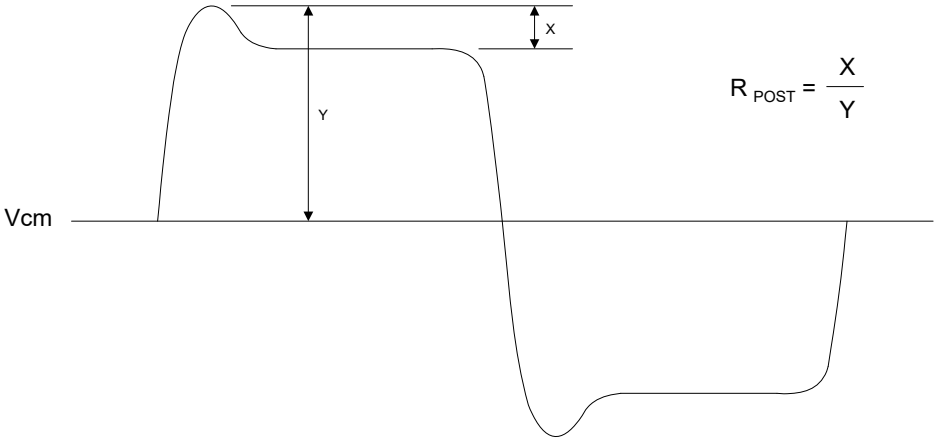


Table 1: Main and Post Cursor Settings

Main Tap Setting	Post Tap Setting	RPOST (Post-to-Main Cursor)
60	0	0.00
59	1	0.03
58	2	0.07
57	3	0.10
56	4	0.13
55	5	0.17

Table 1: Main and Post Cursor Settings (Continued)

Main Tap Setting	Post Tap Setting	RPOST (Post-to-Main Cursor)
54	6	0.20
53	7	0.23
52	8	0.27
51	9	0.30
50	10	0.33
49	11	0.37
48	12	0.40
47	13	0.43
46	14	0.47
45	15	0.50
44	16	0.53
43	17	0.57
42	18	0.60
41	19[a]	0.63
40	20[a]	0.67
39	21[a]	0.70
38	22[a]	0.73
37	23[a]	0.77

a. If post 2 to 1 = 1.

1.5.2 Receive Path

The receive path accepts the 10.3125 Gb/s data at the XFI (10GBASE-KR) receivers and sends the data for 10.3125 Gb/s serial transmission at the XGPHY copper interface.

1.5.2.1 Limiting Amplifier

The BCM84891L differential limiting amplifier at the receiver path provides post-amplification of low-level signals between XFI (10GBASE-KR) input and the XFI (10GBASE-KR) clock recovery inputs. The differential voltage peak-to-peak swing can be between (TBD) and (TBD). The serial input has an internal 100Ω termination between the differential lines and internally biased.

1.5.2.2 XFI/10GBASE-KR Clock Recovery

The XFI (10GBASE-KR) CDR generates a clock that is at the same frequency as the incoming data bit rate, 10.3125 Gb/s, at the serial data inputs, XFI_I P/N. The clock is phase-aligned so that it samples the data at the center of the data eye pattern.

The phase relationship between the edge transitions of the data and those of the generated clock are compared by a phase/frequency discriminator. Output pulses from the discriminator indicate the required direction of phase corrections. These pulses are smoothed by a loop filter. Frequency stability without incoming data is guaranteed by an internal reference clock that the PLL locks onto when data is lost.

1.5.2.3 XFI/10GBASE-KR CDR Lock Detect

The BCM84891L contains a lock detect circuit that monitors the 10.3125 GHz frequency of the internal VCO. The frequency of the incoming data stream must be within ±100 ppm of the 10.3125 Gb/s data stream for the lock detector to declare signal lock. CDR_LOL goes low when the XFI (10GBASE-KR) CDR is locked to the incoming data.

1.5.2.4 XFI/10GBASE-KR PMD CDR Lock to Incoming Data Detector

The BCM84891L contains a loss-of-signal (LoS) detect circuit that monitors the integrity of the serial receiver data path. A peak detector looks for a minimum amplitude swing. If the serial data input is not present, the PMD_LOS bit in XFI (10GBASE-KR) CDR PHY Control Status Register (TBD) is set to 1.

1.5.2.5 XFI/10GBASE-KR Serial Input Interface

The XFI (10GBASE-KR) serial inputs (XFI_IP/N) have built-in AC-coupling. AC-coupling prevents voltage drops across the input devices of the BCM84891L when the input signals are sourced from a device with a higher operating voltage.

1.5.2.6 XFI/10GBASE-KR Equalizer

The BCM84891L includes a programmable equalizer, which provides frequency response peaking centered around the serial input signal to reduce the effects of ISI caused by long PCB traces.

1.5.2.7 XFI/10GBASE-KR Deserializer

The XFI (10GBASE-KR) serial data stream is deserialized to a 64-bit word by a serial-to-parallel converter. The CDR output clocks the serial-to-parallel converter. Under normal operation, the CDR recovers the clock from the data. If data is not present, the clock is recovered from the internal reference clock. The output of this stage is sent to the RX Gearbox.

1.5.2.8 XFI/10GBASE-KR Egress RX Gearbox

The RX gearbox is a buffer that receives serial data from the PMA sublayer and converts it into 66-bit blocks. The 66-block data is passed to the descrambler.

1.5.2.8.1 Descrambler

The 66-bit data blocks are received from the gearbox and passed through a descrambling polynomial.

1.5.2.9 64-Bit/66-Bit Synchronizer/Decoder

A Frame Synchronizer searches for valid sync-header bits to identify the boundaries of the 66-bit data frames. When valid sync-headers are obtained, lock is achieved. A descrambler processes the payload to reverse the effect of the scrambler by using the same polynomial as the link partner's TX polynomial. The receiver process decodes blocks according to IEEE 802.3ae Clause 49.

1.6 5G or 2.5G Rate Over XFI Interface in 10GBASE-R

The BCM84891L supports 5G transfer rate over XFI interface in 10GBASE-R mode when the line side is linked at 5GBASE-T. In addition to 2500BASE-X/2500BASE-R mode, the BCM84891L supports 2.5G rate over XFI interface in 10GBASE-R when the line side is linked at 2.5GBASE-T.

The BCM84891L requires to be configured for 2.5G/5G rate over XFI mode using the command handler (see Section 1.22, MDIO Command Handler Function) after reset and before the line side auto-negotiates to link at 5GBASE-T/5GBASE-T. The BCM84891L is set to operate as 2500X/5000X mode at default.

The 5G or 2.5G transfer rate over XFI in 10GBASE-R mode is handled by the BCM84891L through data rate shaping buffer by inserting or deleting idles. The BCM84891L expects to receive packets with sufficient Inter Packet Idles from the MAC (switch/controller) for the 5G or 2.5G rate effectively transfer over the XFI interface in 10GBASE-R mode.

NOTE:

- AutogrEEEn mode is not supported when 5G or 2.5G rate over XFI interface in 10GBASE-R mode is used.
- 5G or 2.5G rate over XFI interface in 10GBASE-R mode is supported when KR is enabled.
- 2500X is not supported when KR mode is enabled. When KR mode is used, first enable the 2.5G rate over XFI interface in 10GBASE-R mode through the command handler.
- The maximum packet size is 15 KB for 5GBASE-T and 10 KB for 2.5GBASE-T when the MAC interface is 10G.

1.7 100BASE-TX/1000BASE-T

1.7.1 Encoder

In 100BASE-TX mode, the BCM84891L transmits a continuous data stream over the twisted-pair cable. The transmit packet is encapsulated by replacing the first two nibbles of preamble with a start-of-stream delimiter (J/K codes) and appending an end-of-stream delimiter (T/R codes) to the end of the packet. The transmitter repeatedly sends the idle code groups between packets. The encoded data stream is serialized and then scrambled by the stream cipher block, as described in Section 1.7.12, Stream Cipher. The scrambled data is then encoded into MLT3 signal levels.

In 1000BASE-T mode, the BCM84891L simultaneously transmits and receives a continuous data stream on all four pairs of the Category 5 cable. Byte-wide data from the transmit data pins is scrambled when the transmit enable is asserted and the trellis code is modulated into a four-dimensional constellation, each dimension of which is transmitted on a separate channel of the transmit data stream. The transmit packet is encapsulated by replacing the first two bytes of the preamble with a start-of-stream delimiter and appending an end-of-stream delimiter to the end of the packet. When the transmit error input is asserted during a packet transmission, a transmit error code group is sent in place of the corresponding data code group. The transmitter sends idle code groups or carrier extend code groups between packets. Carrier extension is used by the MAC to separate packets within a multiple-packet burst, and is indicated by asserting the transmit error signal and placing 0Fh on the transmit data pins while the transmit enable is low. A carrier extend error is indicated by replacing the transmit data input with 1Fh during carrier extension.

The transmitter encoding for each of the data rates complies with the applicable IEEE standard.

1.7.2 Decoder

In 100BASE-TX mode, following equalization and clock recovery, the receive data stream is converted from MLT3 to serial nonreturn to zero (NRZ) data. The NRZ data is descrambled by the stream cipher block, as described later in this document. The descrambled data is then deserialized and aligned into 5-bit code groups. The 5-bit code groups are decoded into 4-bit data nibbles. The start-of-stream delimiter is replaced with preamble nibbles, and the end-of-stream delimiter and idle codes are replaced with 0h. When an invalid code group is detected in the data stream, the BCM84891L flags the error with an in-band status code that indicates error.

In the 1000BASE-T mode, following clock recovery, equalization, crosstalk and echo cancellation and gain adjustment, the data stream is passed through the Viterbi decoder, descramble, and translated back into byte-wide data.

The start-of-stream delimiter is replaced with preamble bytes, and the end-of-stream delimiter and idle codes are replaced with 00h. Carrier extend codes are replaced with 0Fh or 1Fh. Decoding complies with IEEE 802.3ab standard.

1.7.3 Carrier Sense

Carrier sense is reported with the in-band status mechanized according to the standard. In 1000BASE-T SGMII mode, the carrier sense information is encoded into the control signals.

1.7.4 Link Monitor

In 100BASE-TX mode, receive signal energy is detected by monitoring the receive pair for transitions in the signal level. Signal levels are qualified using squelch detect circuits. When no signal is detected on the receive pair, the link monitor enters the Link Fail state and the transmission and reception of data packets are disabled. When a valid signal is detected on the receive pair for a minimum of 1 ms, the link monitor enters link-pass state and the transmit and receive functions are enabled.

Following the auto-negotiation in the 1000BASE-T mode, the master transceiver begins sending data on the media. The slave transceiver also begins transmitting when it has recovered the master transceiver’s timing. To complete the process, each end of the link continuously monitors its local receiver status. The master begins training its receiver when it detects the slave's transmitted signal. When the local receiver status has been good for at least 1 microsecond (µs), the link monitor enters the link-pass state and the transmission and reception of data packets are enabled. When the local receiver status is bad for more than 750 ms, the link monitor enters the link-fail state, and the transmission and reception of data packets are then disabled.

1.7.5 Digital Adaptive Equalizer (100/1000BASE-T Only)

The digital adaptive equalizer removes ISI created by the transmission channel media. The equalizer accepts sampled unequalized data from the ADC on each channel and produces equalized data. The BCM84891L achieves optimum signal-to-noise ratio by using a combination of Feed-Forward Equalization (FFE) and Decision-Feedback Equalization (DFE) techniques. Under harsh noise environments, these powerful techniques achieve a Bit Error Rate (BER) of less than 1×10^{-12} for transmissions up to 100m on Category 5 twisted-pair cabling. The all-digital nature of the design makes the performance very robust. The filter coefficients are self-adapting to accommodate varying conditions of cable quality and cable length.

1.7.6 Echo Canceler

Because of simultaneous bidirectional transmission of data on each cable pair in 1000BASE-T, echo impairments from the local transmitters are present at each receiver. A digital echo canceler subtracts an estimate of the echo from the received signal at the output of the FFE. The digital echo canceler coefficients are adaptive to track the varying echo transfer function caused by different channels, transmitters, cable geometry, and environmental conditions.

1.7.7 Crosstalk Canceler

The BCM84891L transmits and receives a continuous data stream on four channels. For a given channel, the signals sent by the other three local transmitters cause impairments on the received signal because of near-end crosstalk (NEXT) between the pairs. The effect can be canceled because each receiver has access to the data for the other three pairs that cause this interference. The output of the adaptive NEXT canceling filters is added to the FFE output to cancel the NEXT impairment.

1.7.8 Analog-to-Digital Converter

Each receive channel has its own 125 MHz ADC that samples the incoming data on the receive channel and feeds the output to the digital adaptive equalizer. Advanced analog circuit techniques achieve the following results:

- Low offset
- High-power supply noise rejection
- Fast settling time
- Low bit error rate

1.7.9 Clock Recovery/Generator

The clock recovery and generator block creates the transmit and receive clocks for 1000BASE-T and 100BASE-TX operation. In 100BASE-TX mode, the transmit clock is locked to a multiple of the 50 MHz crystal input, and the receive clock is locked to the incoming data stream.

In 1000BASE-T mode, the two ends of the link perform loop timing. One end of the link is configured as the master, and the other is configured as the slave. The master transmit and receive clocks are locked to a multiple of the 50 MHz crystal input. The slave transmit and receive clocks are locked to the incoming receive data stream. Loop timing allows for the straightforward cancellation of echo and NEXT impairments by ensuring that the transmitter and receiver at each end of the link are operating at the same frequency.

1.7.10 Baseline Wander Correction

1000BASE-T and 100BASE-TX data streams are not always DC-balanced and thus have spectral energy down to DC; however, magnetics introduce high-pass filtering that removes some of this low-frequency energy. The loss of this low-frequency energy causes a form of intersymbol interference called *baseline wander*. Baseline wander is an apparent time-varying and pattern-dependent shift of the DC offset of the signal that is actually due to the absence of DC/low-frequency energy caused by the high-pass filtering in the system. The presence of this type of intersymbol interference can greatly reduce the noise immunity and performance of the receiver. The BCM84891L automatically compensates for baseline wander by restoring the missing low-frequency energy to the receive signal, which significantly improves the performance of the receiver and greatly reduces the probability of symbol errors.

1.7.11 Multimode TX Digital-to-Analog Converter

The multimode transmit DAC transmits PAM5- and MLT3-coded symbols. The transmit DAC performs signal wave shaping that decreases the unwanted high-frequency signal components and reduces electromagnetic interference (EMI). The transmit DAC uses a current drive output that is well-balanced, and, therefore, produces low-noise transmit signals.

1.7.12 Stream Cipher

In 1000BASE-T and 100BASE-TX modes, the transmit data stream is scrambled to reduce radiated emissions and to ensure that there are adequate transitions within the data stream. The 1000BASE-T scrambler also ensures that there is no correlation among symbols on the four different wire pairs and in the transmit and receive data streams. The scrambler reduces peak emissions by spreading the signal energy over the transmit frequency range and eliminating peaks at certain frequencies. The randomization of the data stream also assists the digital adaptive equalizers and echo/crosstalk cancelers. The algorithms in these circuits require there to be no sequential or cross-channel correlation among symbols in the various data streams.

In 100BASE-TX mode, the transmit data stream is scrambled by exclusive-ORing the encoded serial data stream. This is done with the output of an 11-bit-wide Linear Feedback Shift Register (LFSR), producing a 2047-bit nonrepeating sequence.

In 1000BASE-T mode, the transmit data stream is scrambled by exclusive-ORing the input data byte with an 8-bit-wide cipher text word. The cipher text word generates each symbol period from eight uncorrelated maximal length data sequences that are produced by linear remappings of the 33-bit-wide LFSR output. After the scrambled data bytes are encoded, the sign of each transmitted symbol is again randomized by a 4-bit-wide cipher text word that is generated in the same manner as the 8-bit word. The master and slave transmitters use different scrambler sequences to generate the cipher text words. For repeater or switch applications, where all ports can transmit the same data simultaneously, signal energy is randomized further by using a unique seed to initialize the scrambler sequence for each PHY.

The receiver descrambles the incoming data stream by exclusive-ORing it with the same sequence generated at the transmitter. The descrambler detects the state of the transmit LFSR by looking for a sequence representing consecutive idle code groups. The descrambler locks to the scrambler state after detecting a sufficient number of consecutive idle codes. The BCM84891L enables transmission and reception of packet data only when the descrambler is locked. The receiver continually monitors the input data stream to ensure that it has not lost synchronization by checking that inter-packet gaps containing idles or frame extensions are received at expected intervals and by monitoring idle error rate during idles. When the BCM84891L detects loss of synchronization, it notifies the remote PHY of the inability to receive packets (1000BASE-T mode only) and attempts to resynchronize to the received data stream. If the descrambler is unable to resynchronize for a period of 750 ms, the BCM84891L is forced into the link-fail state.

1.7.13 Wire Map and Pair Skew Correction

During 1000BASE-T operation, the BCM84891L can automatically detect and correct some UTP cable wiring errors. The symbol decoder detects and compensates for (internal to the BCM84891L) the following errors:

- Wiring errors caused by the swapping of pairs within the UTP cable.
- Polarity errors caused by the swapping of wires within a pair.

The BCM84891L also automatically compensates for differences in the arrival times of symbols on the four pairs of the UTP cable. The varying arrival times are caused by differing propagation delays (commonly referred to as delay skew) between the wire pairs. The BCM84891L can tolerate delay skews of up to 64 ns. Auto-negotiation must be enabled to take advantage of the wire map correction. During 100 Mb/s operation, the pair swaps are corrected. The delay skew is not an issue though, because only one pair of wires is used in each direction.

1.7.14 Automatic MDI Crossover

NOTE: This function only operates when copper auto-negotiation is enabled.

During copper auto-negotiation, one end of the link must perform an MDI crossover so that each transceiver's transmitter is connected to the other receiver. The BCM84891L can perform an automatic media-dependent interface (MDI) crossover, eliminating the need for crossover cables or cross-wired (MDIX) ports. During auto-negotiation, the BCM84891L normally transmits on the TRD±{0} pin and receives on the TRD±{1} pin.

When connecting to another device that does not perform MDI crossover, the BCM84891L automatically switches its TRD± pin pairs, when necessary, to communicate with the remote device. When connecting to another device that does have MDI crossover capability, an algorithm determines which end performs the crossover function.

During 1000BASE-T operation, the BCM84891L swaps the transmit symbols on pairs 0 and 1, and pairs 2 and 3 if auto-negotiation completes in the MDI crossover state. The 1000BASE-T receiver automatically detects pair swaps on the receive inputs and aligns the symbols properly within the decoder. During 100BASE-TX and 1000BASE-T operation, pair swaps automatically occur within the device and do not require user intervention.

1.7.15 100BASE-TX Forced Mode Auto-MDIX

NOTE: This function only operates when copper auto-negotiation is disabled.

This feature allows the user to disable the copper auto-negotiation in 100BASE-TX and still take advantage of the automatic MDI crossover function. Whenever the forced link is down for a least 4 seconds, auto-negotiation is internally enabled with its automatic MDI crossover function active until link pulses or 100TX idles are detected. Once detected, the PHY returns to forced mode operation.

The user should set the same speed in register 0 and the auto-negotiation advertisement register 4. For example, the user wanting to force 100TX full-duplex should write register 0 with 2100h and register 4 with 0181h. The feature is enabled by writing register 18h, shadow 7, bit 9 = 1. Copper link can be determined by reading register 19h, bit 2.

1.8 Auto-Negotiation

1.8.1 Copper Interface

The BCM84891L negotiates its mode of operation over the copper media using the auto-negotiation mechanism, defined in the IEEE 802.3u, IEEE 802.3ab, and IEEE 802.3an specifications. When the auto-negotiation function is enabled, the BCM84891L automatically chooses the mode of operation by advertising its abilities and comparing them with those received from its link partner. The BCM84891L can be configured to advertise the following modes:

- 10GBASE-T full-duplex
- 5GBASE-T full-duplex
- 2.5GBASE-T full-duplex
- 1000BASE-T full-duplex and/or half-duplex
- 100BASE-TX full-duplex and/or half-duplex

The transceiver negotiates with its link partner and chooses the highest common operating speed and duplex mode commonly referred to as highest common denominator (HCD). Auto-negotiation can be enabled or disabled by the hardware and software control, but is always required for 1000BASE-T, 2.5GBASE-T, 5GBASE-T, and 10GBASE-T operation.

1.9 5000BASE-X Interface

The BCM84891L can communicate with Ethernet MACs that support 5000BASE-X interface through XFI at 6.25 Gbaud (Gb/s) through the RDN[x]/RDP[x] and TDN[x]/TDP[x] pins. These pins include on-chip 100Ω differential termination resistors. The PCS sublayer uses 8B/10B coding defined by 1000BASE-X to carry date over 6.25 Gbaud rate.

1.10 2500BASE-X Interface

The BCM84891L can communicate with Ethernet MACs that support 2500BASE-X interface through XFI at 3.125 Gbaud (Gb/s) through the RDN[x]/RDP[x] and TDN[x]/TDP[x] pins. These pins include on-chip 100Ω differential termination resistors. The PCS sublayer uses 8B/10B coding defined by 1000BASE-X to carry date over 3.125 Gbaud rate.

1.11 Serial GMII Interface

The BCM84891L can communicate with Ethernet MACs that support SGMII interface through XFI (10GBASE-KR) at 1.25 Gbaud (Gb/s) through the RDN[x]/RDP[x] and TDN[x]/TDP[x] pins. These pins include on-chip 100Ω differential termination resistors.

1.12 USXGMII Interface

The BCM84891L can communicate with Ethernet MACs that support USXGMII interface through XFI (10GBASE-KR) at 10.3125 Gbaud (Gb/s) through the RDN[x]/RDP[x] and TDN[x]/TDP[x] pins. These pins include on-chip 100Ω differential termination resistors. Universal serial 10 Gb media-independent interface provides capability to carry multirate serial data path between PHY and a MAC sublayer using 64-bit/66-bit coding by replicating 100, 10, 4, 2, 1 times the symbol code for 100M/1G/2.5G/5G/10G bits data.

1.13 Synchronous Ethernet (SyncE) Recovered Clock

The BCM84891L Synchronous Ethernet (SyncE) Recovered Clock feature outputs a 25 MHz clock recovered from the slave PHYs MDI interface that can be used to synchronize the whole system with the master node/clock. The SyncE clock and corresponding SyncE lock signals are available on the SYNCECLOCK and SYNCELOCK balls when enabled through 1E.0x404F bit 4 and 1E.0xA04C bits[6:4]. The SYNCELOCK ball outputs high as soon as the recovered clock locks to the receive data timing.

1.13.1 SYNC_E Configuration 1 (DEVAD = 30, Address = 0x404F)

Table 2: SYNC_E Configuration 1 (30.0x404F)

Bit	Name	R/W	Description	Default
15:5	Reserved	RO	Reserved.	0
4	Enable SYNC_E	R/W	Enables Synchronous Ethernet Clocks onto output pad.	0
3:0	Reserved	RO	Reserved.	0

1.13.2 SYNC Common CFG Register (DEVAD = 30, Address = 0xA04C)

Table 3: SYNC Common CFG Register (0xA04C)

Bit	Name	R/W	Description	Default
15:10	Reserved	RSVD	Reserved bits. Write has no effect and read always returns 0.	0
9:4	Reserved	RO	Reserved	0
3	P3_LOCK_STATUS	RO	Lock status bit from Port 3.	0x0
2	P2_LOCK_STATUS	RO	Lock status bit from Port 2.	0x0
1	P1_LOCK_STATUS	RO	Lock status bit from Port 1.	0x0
0	P0_LOCK_STATUS	RO	Lock status bit from Port 0.	0x0

1.14 Energy Efficient Ethernet

The BCM84891L features the Energy Efficient Ethernet (EEE) protocol for 10GBASE-T, 5GBASE-T, 2.5BASE-T, 1000BASE-T, and 100BASE-TX speeds. EEE enables the BCM84891L to auto-negotiate and operate with EEE-compliant link partners to reduce overall system power during low utilization of the link. The BCM84891L is compliant with IEEE 802.3az-2010. The EEE function is enabled by advertising this capability in the EEE Advertisement Register (DEVAD = 7, Register 0x003C) and then, if the link partner also supports EEE, by appropriately signaling with a transition from IDLE to Low-power IDLE over XFI (10GBASE-KR) interfaces as defined and described in the draft specification.

The BCM84891L offers two basic modes of operation:

- Native EEE mode for switches and MACs that support LPI signaling across the XFI (10GBASE-KR) or SGMII interface.
- AutogrEEEn mode for legacy switches and MACs that do not support LPI signaling across the XFI/10GBASE-KR or SGMII interface.

In either native or AutogrEEEn mode, the PHY supports the following:

- 100BASE-TX (auto-negotiation must be enabled)
- 1000BASE-T (auto-negotiation must be enabled)
- 2.5GBASE-T (auto-negotiation must be enabled)
- 5GBASE-T (auto-negotiation must be enabled)
- 10GBASE-T (auto-negotiation must be enabled)

This low-power mode allows for systems on both sides of the link to disable portions of their functionality and save power during periods of low link utilization.

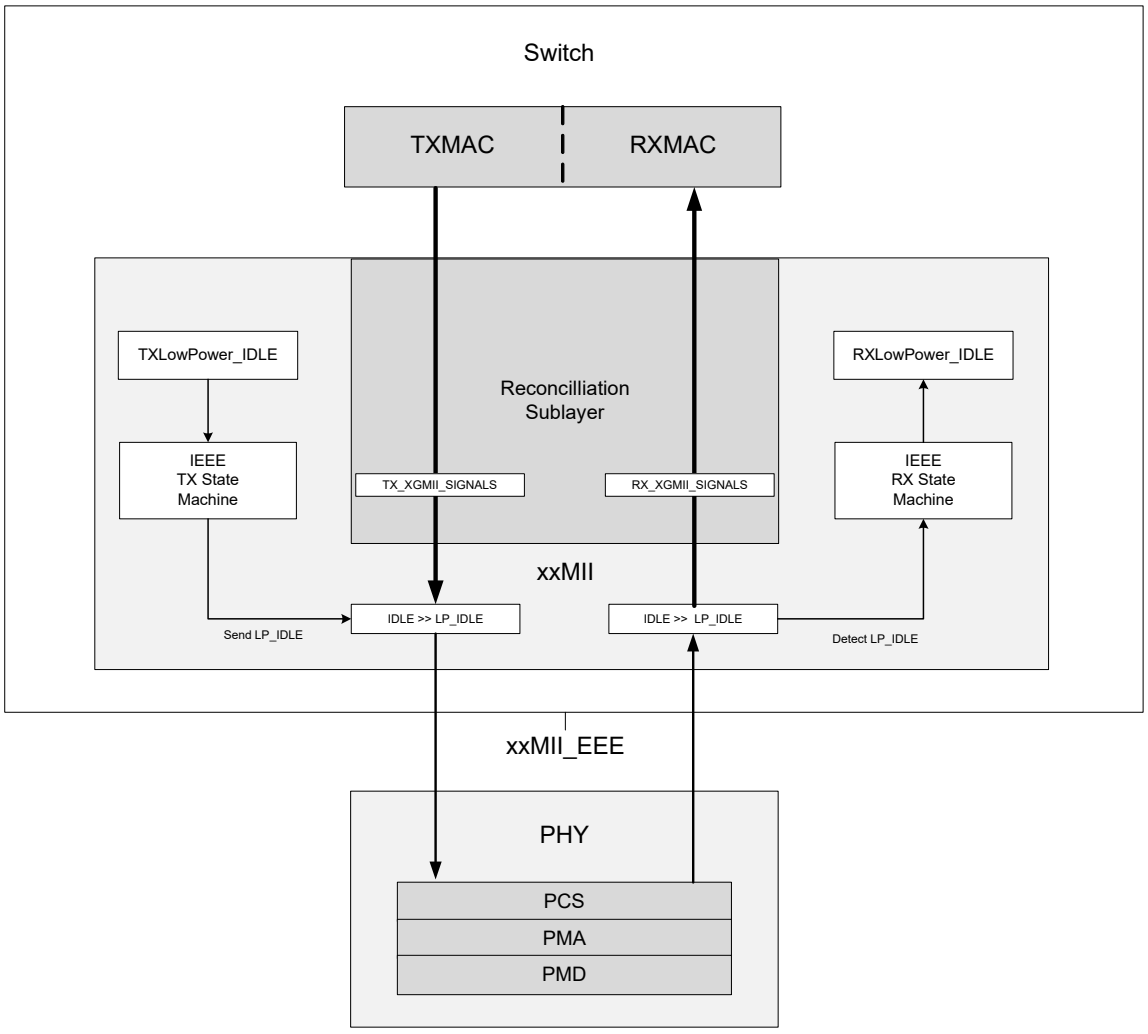
EEE also specifies the means for link partners to determine whether EEE is supported and to provision the best set of parameters common to both devices.

1.14.1 IEEE EEE Mode

The low-power operational mode is an optional mode that allows power saving by switching off parts of the communication device's functionality when no data is transmitted or/and received.

The decision on whether the system should enter Low-Power Idle (LPI) mode or exit LPI mode is done at the MAC level and is communicated to the PHY level to enable maximum power savings. Figure 7 shows a conceptual sketch of the decision flow and agents involved.

Figure 7: IEEE Energy Efficient Ethernet Mode: MAC/PHY Functional Blocks



1.14.1.1 Transmit Direction

In the transmit direction, the entrance to LPI mode of operation is triggered by the reception of LP_IDLE code words on the MAC interface. Following the reception of the LP_IDLE code word, PHY transmits special sleep signal to communicate to the link partner that the local system is entering LPI mode.

After the sleep signal transmission, the transmit function of the local PHY enters a quiet mode.

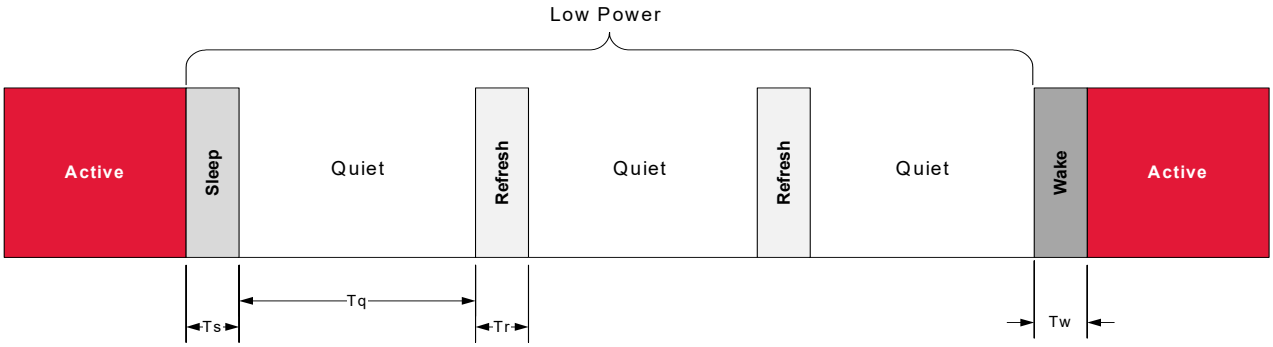
Periodically, the transmit function of the local PHY is enabled to transmit refresh signals that are used by the link partner to update adaptive filters and timing circuits in order to maintain link integrity. This quiet-refresh cycle continues until local MAC sends IDLE code words, which signals to the PHY that low-power idle mode should end.

The transmit function in the PHY communicates this to the link partner and then resumes normal operation mode after a predefined period of time.

In LPI mode, the PHY device is not immediately available for data transmission requests. The PHY awakens by sending normal idle codes on the MAC interface. Following IDLE code reception on the MAC interface, the PHY starts the waking up process. The maximum PHY recovery time (Tw) is different for different protocols. For 10GBASE-T, Tw is 4.48 µs. Note that in 10GBASE-T, WAKE time (Tw) includes the alert time. Figure 8 shows the time diagram of the transmission from a transmitter perspective.

When the link is established in 100BASE-TX and the MAC is transmitting idles, the BCM84891L can start sending LPI. When the link is established in 1000BASE-T, the BCM84891L enters LPI mode only after it transmits LP_SLEEP and receives LP_SLEEP from the link partner. The BCM84891L keeps the link related parameters up to date during refresh. The MAC determines when the BCM84891L stops sending LPI signals on the MDI and transition to normal mode. The BCM84891L stops transmitting LPI signals when the BCM84891L receives normal idles from the MAC. After PHY stop transmitting LPI signals, then after Tw = 20.5 µs for 100BASE-TX or Tw = 16.5 µs for 1000BASE-T link, the MAC may send normal data.

Figure 8: LPI Mode: Transmit Signal Diagram



1.14.1.2 Receive Direction

In the receive direction, the LPI operation is triggered by the reception of LP_IDLE code words from the PHY link partner. This signals that the link partner is about to enter LPI mode.

After sending the LP_IDLE code word, the link partner ceases transmission and enters quiet mode. During this time, the local receiver can disable some of the functionality to reduce power consumption.

Periodically, the link partner transmits refresh signals that are used by the local PHY to update adaptive coefficients and timing circuits.

This quiet-refresh cycle continues until the link partner initiates a transition back to full data mode by transmitting (in 10G, an ALERT signal followed by) a WAKE signal that allows the local receiver to prepare for the full data rate. After a system-specified recovery time, the link supports a nominal operational data rate.

In 100BASE-TX mode, the local PHY transmits a special LP_SLEEP signal to communicate to the link partner that the local system is entering LPI mode. In 1000BASE-T mode, the transmit function of the local PHY enters a quite mode only after the local PHY transmits LP_SLEEP and receives LP_LP_SLEEP from the remote PHY. If the remote PHY does not signal LPI, neither PHY can go quiet. The LPI requests are still passed from one end to the other end of the link, since other system energy saving may be achieved even if the PHY link does not go quiet.

The Tw waiting default for 100BASE-TX is 20.5 µs and for 1000BASE-T is 16.5 µs, unless through Link Layer Data Protocol (LLDP) the upper layer MACs have negotiated new values.

No data frames are lost or corrupted during the transition to or from the EEE mode.

1.14.2 AutogrEEEn Mode

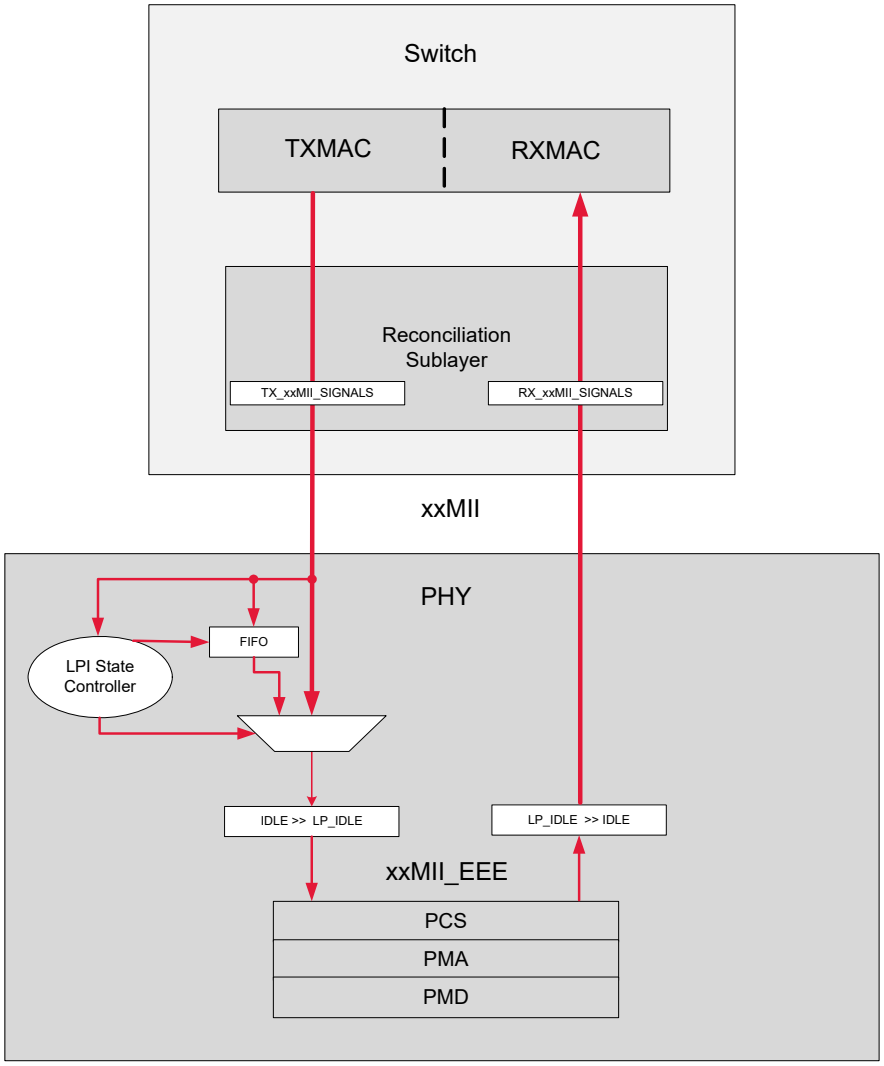
AutogrEEEn mode is a Broadcom mode that allows Broadcom PHYs to provide EEE functionality even when the MAC connected to the PHY does not support the EEE mode (this is particularly useful when using legacy MAC/switches).

In this mode, the EEE policy is managed by the PHY to utilize EEE technology with legacy MACs not supporting this feature. Figure 9 shows the AutogrEEEn functional blocks.

The PHY determines when to transmit LPI signals. This decision is done by counting the number of consecutive idle symbols (symbol-blocks in 10G) from the MAC and comparing this to the idle threshold value. The PHY immediately sends LPI _IDLEs to the MDI. The PHY stops sending LPI when non-idle characters are received from the MAC layer.

NOTE: AutogrEEEn mode is not supported for 5G or 2.5G rate over XFI mode.

Figure 9: AutogrEEEn Functional Blocks in the PHY



1.14.2.1 Idle Threshold

The idle threshold value defines the number of idles that the PHY waits before sending LPIs to the line in AutogrEEEn LPI mode. The unit of measurement of the idle threshold and the constant latency is the block, which is defined as 8-bits of control plus 64-bits of data. A frame is defined as 50 blocks.

The idle threshold value must be at least one block greater than the constant latency value. The constant latency value must be at least 23 frames (23 frames = 1150 blocks) for 10GBASE-T.

1.14.2.2 Constant Latency Operation

The internal FIFO in the PHY is filled with xxMII data until the constant latency value is reached. This value is approximately equal to {SLEEP + ALERT + WAKE} time (in 10GBASE-T, this is 23 frames).

When FIFO reaches its fill level, the data is transmitted from FIFO to the MDI, while new data is written into FIFO.

The PHY continues with this process until the number of consecutive idles received from the XGMII equals the threshold value entered by the user (or firmware). At this point, the PHY enters LPI (AutogrEEEn) mode and the PHY transmits LPI characters (instead of the idles found in the FIFO). It is important to remember that the idle threshold must be one block greater than the constant latency value.

This process continues until a non-idle character is detected at the XGMII interface. When a non-idle character is detected at the XGMII interface, the system stops sending LPI characters and resumes sending the idles that have been filling the FIFO.

1.14.2.3 Variable Latency Operation

In this mode, the internal FIFO adapts to the data content of the traffic detected at the xxMII interface. In the case of 10GBASE-T, the first non-idle data detected at the xxMII (while in LPI mode) can experience a minimum delay of 14 frames (min) or up to 23 frames (max). Traffic right behind the first non-idle data block can experience different delays, depending on the number of idles in between. In this mode, the user can select the number of idles detected at the xxMII before entering LPI (AutogrEEEn) mode.

1.15 Enabling and Disabling the EEE Feature in the PHY

The EEE feature is disabled by default. To put the device in either of the EEE modes, use the PHY's MDIO Command Handler. This is detailed in Table 5. After following the sequence, the local PHY will have advertised its new EEE capabilities to the remote PHY.

1.15.1 Enabling IEEE EEE Mode

To enable IEEE EEE for a port in the BCM84891L, use the command CMD_SET_EEE_MODE with the appropriate value, as described in Table 5.

Example: To advertise EEE in 10GBASE-T, write the MDIO Command Handler registers to enable the EEE modes. To monitor the link partner 10GBASE-T EEE advertising, check bit 3 of DEVAD = 7 Register 0x003D. To determine if the local device supports 10GBASE-T EEE, check bit 3 of DEVAD = 3 Register 0x0014.

1.15.2 Disabling IEEE EEE Mode

To disable IEEE EEE for a port in the BCM84891L, use the command CMD_SET_EEE_MODE with the appropriate value, as described in Table 5.

1.15.3 Enabling AutogrEEEn Mode

To enable AutogrEEEn for a port in the BCM84891L, use the command CMD_SET_EEE_MODE with the appropriate value, as described in Table 5.

1.15.4 Disabling AutogrEEEn Mode

To disable AutogrEEEn for a port in the BCM84891L, use the command CMD_SET_EEE_MODE with the appropriate value, as described in Table 5.

1.15.5 Monitoring EEE Readiness

After an AUTONEG restart, the user can monitor the readiness of EEE as described in Table 5.

To monitor the status/readiness of the EEE/AutogrEEEn feature for a port in the BCM84891L, use the command CMD_GET_EEE_MODE (and data registers: DATA2_REG, DATA3_REG, and DATA4_REG to monitor idle threshold and constant latency value) as described in Table 5.

1.15.6 Fast Retrain

1.15.6.1 IEEE Fast Retrain Mode

To advertise IEEE Fast Retrain mode:

- Use REG 1.0x00093[0] = 1 <=> Fast Retrain MODES are ENABLED
- Use REG 1.0x00093[4] = 1 <=> Advertise IEEE Fast Retrain

1.15.6.2 Negotiated Fast Retrain (NFR) Mode

When Fast Retrain MODES are ENABLED (that is, REG 1.0x00093[0] = 1) and IEEE Fast Retrain is NOT ENABLED (rather, REG 1.0x00093[4] = 0) then the port advertises NFR.

1.15.6.3 BCM84891L-Proprietary Fast Retrain Mode

- When BCM84891L recognizes another BCM84891L as link partner, it uses the proprietary Fast Retrain with 24 ms latency.
- When the BCM84891L recognizes a BCM84823 as link partner, it uses the NFR Fast Retrain method.

1.16 Jumbo Packets

The BCM84891L supports Ethernet packet sizes of up to 18 KB for 10GBASE-T/5GBASE-T/2.5GBASE-T/1000BASE-T/100BASE-TX, up to 15 KB for 5GBASE-T, and 10 KB for 2.5GBASE-T when the MAC interfaces is 10G. When using these large Ethernet packet sizes for 1000BASE-T/100BASE-TX, ensure there is a minimum IPG of 14 bytes between packets.

1.17 HiGig2™ Messages Support

The BCM84891L supports HiGig2™ messages for implementing flow control (SAFC and LLFC), utilizing symbols that are not in the Clause 49 symbol set as defined in IEEE 802.3.

Clause 49 says: All XGMII and 10GBASE-R control code values that do not appear in the table shall not be transmitted and shall be treated as an error if received. Therefore, when the HiGig2 is enabled by setting the DEVAD = 1 Register 0xA939 to value of 0x0183, the BCM84891L passes SAFC/LLFC messages.

1.18 Loopback Operation

The loopback modes are described here, and are illustrated in Figure 10.

1.18.1 XFI/10GBASE-KR System Loopback at PCS/PMA of 10GBASE-T/1000/100BASE-T

The XFI/10GBASE-KR System Loopback sends packets transmitted to the BCM84891L back to the switch/MAC. This loopback occurs in the 10G/1000/100BASE-T/line-side PCS unit. The XFI/10GBASE-KR interface signal, TDN/P[x] sends out the packet received on RDN/P[x]. The incoming data must be Ethernet-compliant.

1.18.1.1 Loopback at PCS of 10GBASE-T

Set 10G/5G/2.5GBASE-T Device = 3 PCS Control 1 Register (DEVAD = 3, Address = 0x0000) bit 14 to 1.

1.18.1.2 Loopback at PCS for 5GBASE-T

Use the Command Handler to set IEEE 802.3bz mode.

Set 10GBASE-T Device = 3 PCS Control 1 Register (DEVAD = 3, Address = 0x0000) bit 14 to 1.

1.18.1.3 Loopback at PCS for 2.5GBASE-T

Use the Command Handler to set IEEE 802.3bz mode.

Set 10GBASE-T Device = 3 PCS Control 1 Register (DEVAD = 3, Address = 0x0000) bit 14 to 1.

1.18.1.4 Loopback at PCS of 1000/100BASE-T

Write 0x4140 to Device = 7, register 0xFFE0.

1.18.1.5 Loopback at PCS of 100BASE-T

Write 0x7100 to Device = 7, register 0xFFE0.

NOTE: AUTONEG should be set in loopback mode.

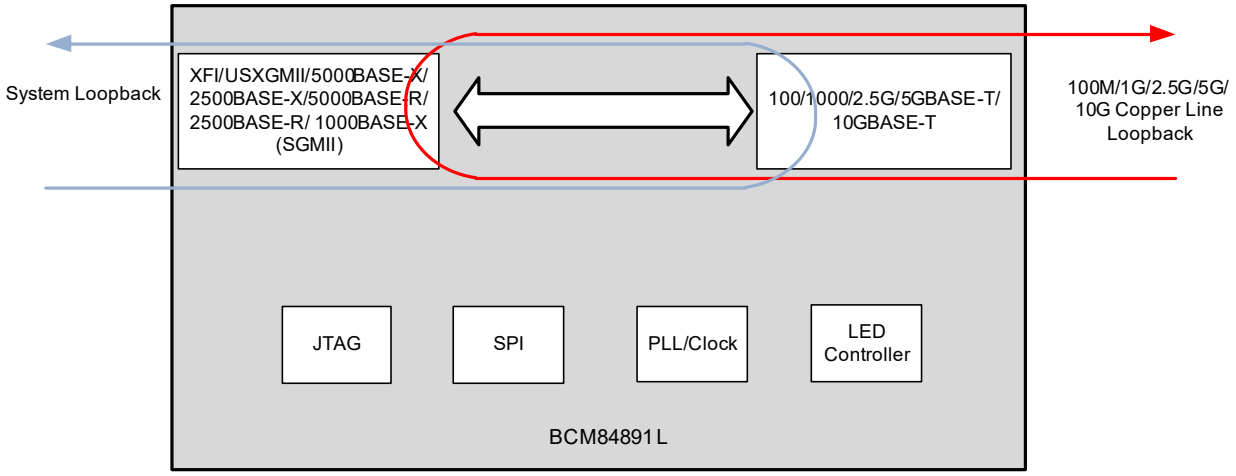
1.18.2 Copper (10G) Line Loopback at PMD/PCS of XFI/10GBASE-KR

The XFI/10GBASE-KR loopback enables the receive data path from the line-side unit through 64-bit/66-bit encoder looped back to the transmit path 64-bit/66-bit encoder, as shown in Figure 10.The data then passes to the line through the BCM84891L copper interface. The BCM84891L expects legal Ethernet packets to perform the loopback operations.

Set XFI DEVAD = 1, XFI 10GBASE-R PMD Control Register (DEVAD = 1, Address = 0x0000) bit 0 to 1 or XFI DEVAD = 3, XFI 10GBASE-R PCS Control 1 Register (DEVAD = 3, Address = 0x0000) bit 14 to 1.

NOTE: Prior to normal operation, perform a soft reset after the device is placed in loopback.

Figure 10: BCM84891L Loopback Modes Per-Port in XFI/10GBASE-KR-to-Copper Configuration



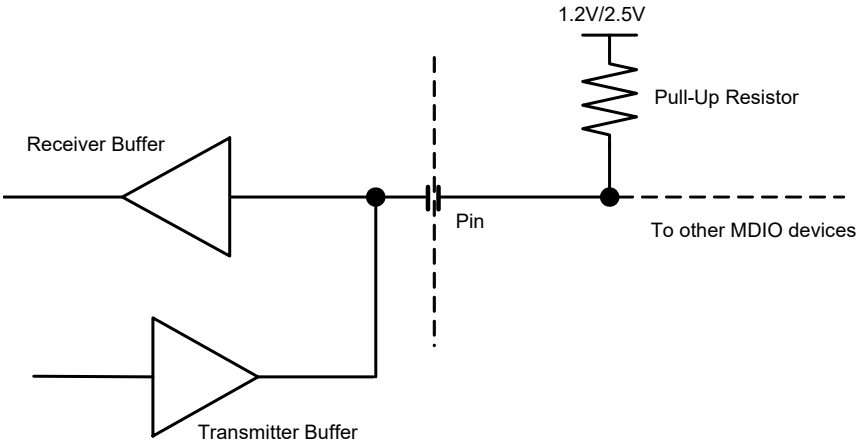
NOTE: Prior to normal operation, perform a soft reset after the device is placed in loopback.

1.19 Management Interface

The BCM84891L supports the IEEE 802.3 Clause 45 Station Management Interface. A 16-bit shift register receives data from the MDIO pin on the rising edge of the MDC clock. The frame format begins with a preamble for clock synchronization followed by the start-of-frame sequence. The read or write opcode, PRTAD, and DEVAD fields follow next. Depending on the read/write opcode, data is either received or transmitted by the BCM84891L. After the 16-bit data field is transferred, the MDIO signal is returned to a high-impedance state (idle).

During idle, MDC is not required to be active. A read operation configures the MDIO as an output. A write operation configures the MDIO as an input. Writes to an unsupported register address are ignored. The PRTAD field is configurable through the PRTAD pins. The maximum speed for the MDIO interface is 25 MHz and the MDIO interface supports 1.2V operation (see the figure below).

Figure 11: MDIO Interface



NOTE: To operate at maximum speed, a pull-push driver should be consider for station manager. Users can download the program code into the processor local memory through the MDIO interface by strapping the Config13 pin low.

1.20 TRD (MDI) Interface Pair Swapping

The BCM84891L supports TRD (MDI) pair swapping through the CONFIG5 strap pin or through the command handler to easily layout the routing of the signal between the BCM84891L balls and the Integrated Connector Module (ICM) pins. When CONFIG5 is strap low, the pair for the even ports are swapped and TRD (MDI) signals are line up with 1x8 ICM pins. When CONFIG5 is strap high, the TRD (MDI) pair signals line up with 1x1 ICM pin out. TRD (MDI) signals pair can be configured after the device is out of reset through the command handler function using CMD_SET_PAIR_SWAP/ CMD_GET_PAIR_SWAP commands. The table below provides the TRD (MDI) pin pair ordering.

Table 4: TRD (MDI) Interface Pair Swapping

Port Number	Balls	CONFIG5 = 1	CONFIG5 = 0
Port 0	M3	TRD[3]–	TRD[0]–
Port 0	N3	TRD[3]+	TRD[0]+
Port 0	M5	TRD[2]–	TRD[1]–
Port 0	N5	TRD[2]+	TRD[1]+
Port 0	M7	TRD[1]–	TRD[2]–
Port 0	N7	TRD[1]+	TRD[2]+
Port 0	M9	TRD[0]–	TRD[3]–
Port 0	N9	TRD[0]+	TRD[3]+

1.21 SPI Interface

An external SPIROM can be used to load the optimized code and configuration for the BCM84891L. This is accomplished by connecting pins SPI_CSB, SPI_SCK, SPI_OUT, and SPI_SOI to corresponding pins of an SPIROM.

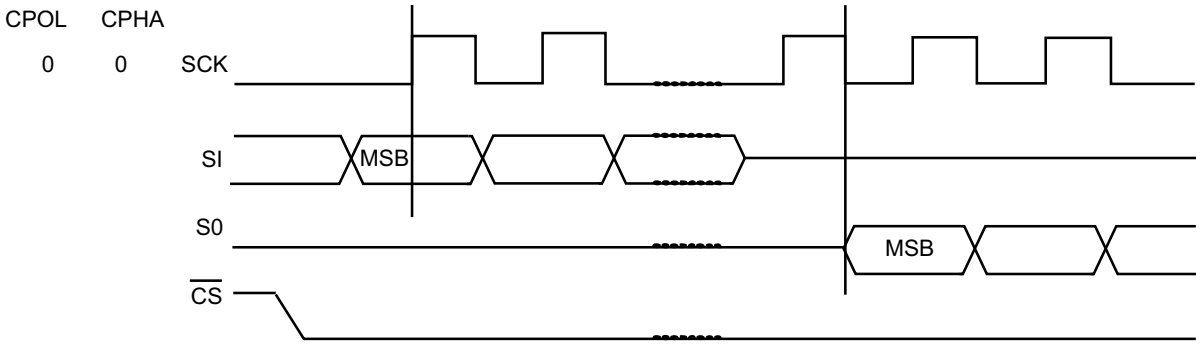
NOTE: The Config13 pin should be high to load the SPI EEPROM into the processor local memory. User can download the program code into the processor local memory through MDIO interface by strapping the Config13 pin low.

1.21.1 SPI Modes

These devices can drive the SPI peripheral running in the following mode:

CPOL = 0, CPHA = 0

Figure 12: Supported SPI Mode

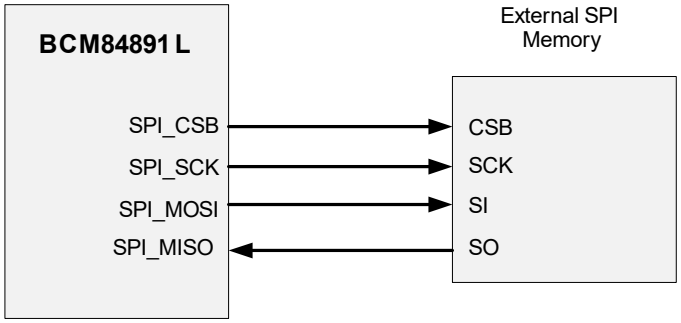


In this mode, output data (SI) is latched on the rising edge of SCK, and input data (SO) must be available from the falling edge of SCK.

1.21.2 Functional Description

The figure below shows a schematic diagram of the BCM84891L SPI serial interface.

Figure 13: SPI Serial Interface Block Diagram



The BCM84891L sends first a 8-bit opcode (0000 0011) that is decoded by the external SPI Memory as READ-specific instruction to be executed. All opcodes, array addresses, and data are transferred in an MSB-first-LSB-last fashion.

1.21.3 Read Data Bytes (READ)

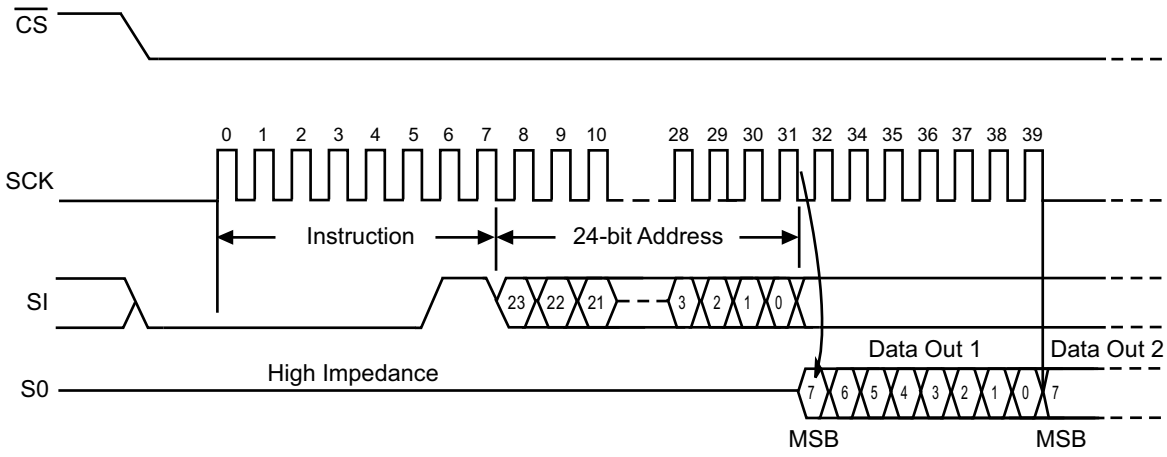
Reading the memory through the serial SPI link requires the following sequence:

1. After the CSB line is pulled low to select the device, the READ opcode is transmitted through the SI line, followed by the 3-byte address to be read (address bits A23 to A18 are Don't Care for a 1 Mb memory).
2. Upon completion, any data on the SI line is ignored.
3. The data (D7 to D0) at the specified address is then shifted out onto the SO line. Each bit is shifted out at a maximum SCK frequency of FSCK.

If only one byte is to be read, the CSB line should be driven high after the data comes out. The READ sequence can be continued, as the byte address is automatically incremented and data continues to shift out.

The instruction sequence is shown in the figure below.

Figure 14: READ Instruction Sequence



1.21.4 SPI Memory Power-Up Sequence

Usually, any external SPI Memory must not be selected at power-up or power-down (that is, CSB must follow the voltage applied on VCC) until VCC reaches the correct VCC (min) at power-up, and then for a further delay of CPU (VCC (min) to $\overline{CS}$ low).

To meet the CPU requirement, the BCM84891L has an internal timer of 21 ms that starts counting from the release of the reset.

After the timer is expired, the BCM84891L starts reading data from the external SPI Memory providing a clock of 6.25 MHz.

The SPI clock can be reconfigured by register or it can be automatically set by the first 32 bits read from the SPI memory to eventually meet the max clock rate of the external SPI memory used.

The SPI Master interface of BCM84891L supports up to 31.25 MHz operating clock rate.

1.22 MDIO Command Handler Function

The MDIO Command Handler function is an efficient and robust handshake process to provision and monitor features in the BCM84891L device that guarantees the feature is set properly.

The set of functions that require the MDIO Command Handler are listed in the table below. The corresponding command CODE value should be written in the Command Register CMD (address: 0x1E.0x4005). During 2-second training, the status returns CMD_SYSTEM_BUSY and the user must wait up to 2 seconds for the command to be executed.

Table 5: Features/Commands Using MDIO Command Handler Process

Feature/Command Name	Description	Command Code
CMD_GET_PAIR_SWAP	—	0x8000
CMD_SET_PAIR_SWAP	—	0x8001
Reserved	—	0x8002
Reserved	—	0x8003
CMD_GET_1588_ENABLE	—	0x8004
CMD_SET_1588_ENABLE	—	0x8005
GET_LIMITED_REACH_MODE_ENABLE	Gets limited reach mode setting.	0x8006
SET_LIMITED_REACH_MODE_ENABLE	Enables or disables limited reach mode setting.	0x8007
CMD_GET_EEE_MODE	—	0x8008
CMD_SET_EEE_MODE	—	0x8009
CMD_GET_EMI_MODE_ENABLE	—	0x800A
CMD_SET_EMI_MODE_ENABLE	—	0x800B
CMD_GET_SUB_LF_RF_STATUS	—	0x800D
GET_KR_MODE_ENABLE	Gets KR mode setting.	0x800E
SET_KR_MODE_ENABLE	Enables or disables KR mode setting.	0x800F
CMD_CLEAR_SUB_LF_RF	—	0x8010
CMD_SET_SUB_LF_RF	—	0x8011
READ_INDIRECT_GPHY_REG_BITS	Reads indirect GPHY register bit field.	0x8014
WRITE_INDIRECT_GPHY_REG_BITS	Writes indirect GPHY register bit field.	0x8015
GET_XFI_2P5G_5G_MODE	—	0X8016

Table 5: Features/Commands Using MDIO Command Handler Process (Continued)

Feature/Command Name	Description	Command Code
SET_XFI_2P5G_5G_MODE	—	0X8017
GET_TWO_PAIR_1G_MODE	—	0X8018
SET_TWO_PAIR_1G_MODE	—	0X8019
SET_EEE_STATISTICS	—	0X801A
GET_EEE_STATISTICS	—	0X801B
GET_JUMBO_PACKET	—	0X801D
SET_JUMBO_PACKET	—	0X801C
GET_PAUSE_FRAME_MODE	—	0x801F
SET_PAUSE_FRAME_MODE	—	0x8020
GET_802.3BZ_PRIORITY	—	0x8023
SET_802.3BZ_PRIORITY	—	0x8024
SET_USXGMII	—	0x8026
GET_USXGMII	—	0x8027
GET_XFI_TX_FILTERS	—	0x802B
SET_XFI_TX_FILTERS	—	0x802C
GET_XFI_POLARITY	—	0x802D
SET_XFI_POLARITY	—	0x802E
GET_CURRENT_VOLTAGE	—	0x802F
CMD_GET_SNR	—	0x8030
CMD_GET_CURRENT_TEMP	—	0x8031
CMD_SET_UPPER_TEMP_WARNING_LEVEL	—	0x8032
CMD_GET_UPPER_TEMP_WARNING_LEVEL	—	0x8033
CMD_SET_LOWER_TEMP_WARNING_LEVEL	—	0x8034
CMD_GET_LOWER_TEMP_WARNING_LEVEL	—	0x8035

To execute a feature, write the associated code (command CODE) in the CMD register.

The MDIO Command Handler uses six registers to interface with the user. The table below shows the six registers potentially used by this function.

Table 6: MDIO Command Handler Register Set

Register Name	Description	Address
CMD	Command	0x1E.0x4005
STATUS	Status of command	0x1E.0x4037
DATA1_REG	Data 1 register	0x1E.0x4038
DATA2_REG	Data 2 register	0x1E.0x4039
DATA3_REG	Data 3 register	0x1E.0x403A
DATA4_REG	Data 4 register	0x1E.0x403B
DATA5_REG	Data 5 register	0x1E.0x403C

From Figure 15, the STATUS register [STATUS (address: 0x1E.0x4037)] can report different types of status messages (codes). The status' names and values are shown in the table below.

Status register is a special bidirectional register reports the status and can be written by the user.

Table 7: STATUS Codes

STATUS Code Name	Set by	Description	Code Value
CMD_RECEIVED	FW	A command has been received.	0x0001
CMD_IN_PROGRESS	FW	A command is being serviced.	0x0002
CMD_COMPLETE_PASS/ CMD_OPEN_FOR_CMDS	FW	Last command has been executed successfully.	0x0004
CMD_COMPLETE_ERROR/ CMD_OPEN_FOR_CMDS	FW	Execution of the last command produced an error.	0x0008
CMD_SYSTEM_BUSY	FW	System is not ready to accept commands.	0xBBBB

1.22.1 MDIO Command Handler Theory of Operation

Once the system has booted up, the firmware initializes the STATUS register (in Table 7) to CMD_COMPLETE_PASS/ CMD_OPEN_FOR_CMDS and the CMD register to 0x0 as default condition (no operation at 0x0 value). User should poll the status register to check the availability of command handler. If the STATUS register is CMD_IN_PROGRESS or SYSTEM_BUSY, the user must wait for certain period of time and check again. If the STATUS register is not CMD_IN_PROGRESS or SYSTEM_BUSY _CMDS, the user can write the command to CMD register. If the CMD register bit 15 is written as 1, an interrupt is generated and firmware changes the STATUS register to CMD_RECEIVED (see Table 6 and Table 7), and it sends a message to the Service thread to execute the command.

When the Service thread receives the message to execute the user command, it calls the MDIO Command Handler function to process the command.

The MDIO Command Handler reads the command and pass the value of the command into a command array. This value is used as index into the array and returns a function pointer that executes the required command.

Each command function changes the STATUS register to CMD_IN_PROGRESS, and then processes the command. After completion, the command function returns CMD_COMPLETE_PASS/CMD_OPEN_CMDS or CMD_COMPLETE_ERROR/ CMD_OPEN_FOR_CMDS. The MDIO Command Handle changes the STATUS register to CMD_COMPLETE_PASS/ CMD_OPEN_FOR_CMDS or CMD_COMPLETE_ERROR/CMD_OPEN_FOR_CMDS so that the user can poll the status register and know when the command has completed and reads the register results, (see Table 5).

A graphical representation of the process for provisioning and monitoring features is shown in the next section.

1.22.2 Command Procedure

To use the MDIO Command Handler either for enabling/disabling a feature or to read the status/information on a feature, use the followings steps:

1. Poll the STATUS register to see whether the previous command is in progress or the system is busy (CMD_IN_PROGRESS or SYSTEM_BUSY). If previous command is in progress or system is busy, check again until the previous command finishes execution and the system is available for taking command.
2. If any parameters are required for the function, write them to the required DATA registers (see Section 1.23, Command Descriptions, for more information)
3. When the firmware is ready for commands, write the Command code/value from Table 5 to the CMD register.
4. Once the command has been written, poll the STATUS register to check whether the command has completed (CMD_COMPLETE_PASS/CMD_FOR_CMDS or CMD_COMPLETE_ERROR/CMD_OPEN_FOR_CMDS).

5. Once the command has completed, read the specified DATA registers (see Table 6) for any saved results for the command, if applicable (see Section 1.23, Command Descriptions, for more information).
6. For provisioning features that require altering port configuration parameters, restart auto-negotiation to reestablish link using the new parameters (for example, most provisioning processes require this step).

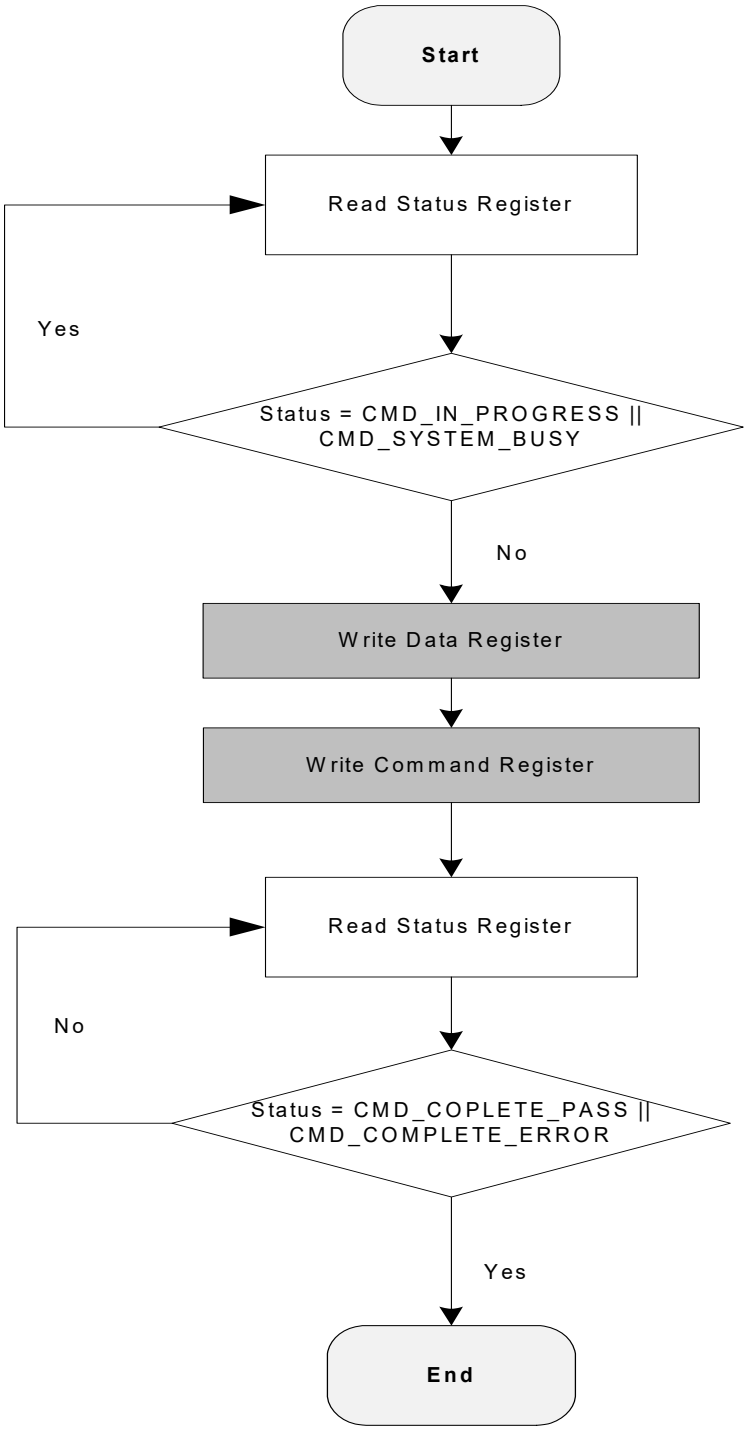
The feature provisioning and monitoring processes are shown in the next section.

NOTE: The recommended polling period for the status register is 100 ms. When a device is in the 10GBASE-T training phase, the command handler status register does not change for up to two seconds. Users should avoid issuing commands during training or start polling the status register after the link status is up.

1.22.3 Provisioning and Monitoring Sequences

The figure below provides steps for provisioning the device through the Command Handler.

Figure 15: Provisioning Process #1



1.23 Command Descriptions

1.23.1 Enable/Disable/View Commands

NOTE: The interpretation of the pair swap values for odd ports and even ports is different. Use the appropriate table below when reading or writing these registers.

1.23.1.1 CMD_ GET_PAIR_SWAP

Description: Gets pair swap values.	
Input Parameters: None.	**Return Results**: DATA1_REG = Forced/requested current swap pair value. DATA2_REG = Current swap pair value.

1.23.1.2 CMD_SET_PAIR_SWAP

Description: Sets pair swap values.	
Input Parameters: DATA2_REG = Swap pair value to be forced.	**Return Results**: None.
NOTE: CMD_SET_PAIR SWAP requires auto-negotiation to take place in order to take effect.	

1.23.1.3 Pair Swap Values for Odd Ports

Table 8: Pair Swap Values for Odd Ports

Bits	Description
Bits [15:8]	Reserved.
Bits [7:6]	PAIR_D_SEL: 00 = Pair A 01 = Pair B 10 = Pair C 11 = Pair D
Bits [5:4]	PAIR_C_SEL: 00 = Pair A 01 = Pair B 10 = Pair C 11 = Pair D
Bits [3:2]	PAIR_B_SEL: 00 = Pair A 01 = Pair B 10 = Pair C 11 = Pair D
Bits [1:0]	PAIR_A_SEL: 00 = Pair A 01 = Pair B 10 = Pair C 11 = Pair D

1.23.1.4 Pair Swap Values for Even Ports

Table 9: Pair Swap Values for Even Ports

Bits	Description
Bits [15:8]	Reserved.
Bits [7:6]	PAIR_A_SEL: 00 = Pair D 01 = Pair C 10 = Pair B 11 = Pair A
Bits [5:4]	PAIR_B_SEL: 00 = Pair D 01 = Pair C 10 = Pair B 11 = Pair A
Bits [3:2]	PAIR_C_SEL: 00 = Pair D 01 = Pair C 10 = Pair B 11 = Pair A
Bits [1:0]	PAIR_D_SEL: 00 = Pair D 01 = Pair C 10 = Pair B 11 = Pair A

1.23.1.5 CMD_ GET_1588_ENABLE

Description:	Returns current value set for internal variable used to enable/disable IEEE 1588 functionality.
Input Parameters: None.	**Return Results**: DATA1_REG = IEEE 1588 enable value.

1.23.1.6 CMD_SET_1588_ENABLE

Description:	Sets internal variable used to enable/disable IEEE 1588 functionality. Setting to 1 enables IEEE 1588. Setting to 0 disables IEEE 1588. Enable or disable IEEE 1588 functionality prior to link up. If enabling or disabling the IEEE 1588 functionality while the link is already up, bring the link down, then back up using an AUTONEG restart or similar mechanism.
Input Parameters: DATA1_REG = IEEE 1588 enable value.	**Return Results**: None.
NOTE: CMD_SET_1588_ENABLE requires auto-negotiation to take place to take effect.	

1.23.1.7 GET_LIMITED_REACH_MODE_ENABLE

Description:	Returns current value set for internal variable used to enable/disable limited reach mode functionality.
Input Parameters: None.	**Return Results**: DATA1: ■ 0 = Limited reach mode is disabled. ■ 1 = Limited reach mode is enabled. DATA2: Valid only when DATA1 = 1. ■ 0 = Limited reach based with standard TX power. ■ 1 = Limited reach based with low TX power. DATA3: Valid only when DATA1 = 1. ■ 0 = Currently is not linked in limited reach mode ■ 1 = Currently is linked in limited reach mode DATA4 to DATA5: Not used.

1.23.1.8 SET_LIMITED_REACH_MODE_ENABLE

Description:	Enables/disables limited reach mode functionality.
Input Parameters: DATA1: ■ 0 = Exit limited reach mode. ■ 1 = Enter limited reach mode. DATA2: ■ 0 = Limited reach mode with standard TX power. ■ 1 = Limited reach mode with low TX power. DATA3 to DATA5: Not used.	**Return Results**: None.

1.23.1.9 CMD_GET_EEE_MODE

Description: Gets AutogrEEEn parameters.

Input Parameters: None.

Return Results:

		5G	2.5G	1G/ 100M	10G
DATA1_REG	Bits	7:6	5:4	3:2	1:0
	EEE Disabled	0	0	0	0
	Native EEE	1	1	1	1
	AutogrEEEn Fixed Latency	2	2	2	2
	AutogrEEEn Variable Latency	3	3	N/A	3
DATA2_REG	AutogrEEEn High Threshold	0	0	N/A	0
DATA3_REG	AutogrEEEn Low Threshold	0x7A12	0x7A12	N/A	0x7A12
DATA4_REG	AutogrEEEn Latency	0x47E	0x47E	N/A	0x47E
DATA5_REG	Reserved	0	0	0	0

NOTE: Although the EEE modes can be different between each speed, the AutogrEEEn parameters for 2.5/5/10G in DATA2_REGs to DATA4_REGs are shared. The 1G/100M AutogrEEEn parameters are not programmable and are unaffected by the values in DATA2_REGs to DATA4_REGs.

DATA1_REG[15:8] = Reserved

Example: When DATA1_REG is 0x00B1, 5G EEE is fixed latency, 2.5G EEE is variable latency, 1G/100M does not advertise EEE, and 10G is native EEE mode. If the data rate is 10G, DATA2_REG through DATA4_REGs are ignored. If the data rate is 5G, DATA4_REG is ignored. If the data rate is 2.5G or 5G, the AutogrEEEn threshold is the same for both.

1.23.1.10 CMD_SET_EEE_MODE

Description: Configures IEEE-EEE and AutogrEEEn.

Input Parameters:

		5G	2.5G	1G/ 100M	10G
DATA1_REG	Bits	7:6	5:4	3:2	1:0
	EEE Disabled	0	0	0	0
	Native EEE	1	1	1	1
	AutogrEEEn Fixed Latency	2	2	2	2
	AutogrEEEn Variable Latency	3	3	N/A	3
DATA2_REG	AutogrEEEn High Threshold	0	0	N/A	0
DATA3_REG	AutogrEEEn Low Threshold	0x7A12	0x7A12	N/A	0x7A12
DATA4_REG	AutogrEEEn Latency	0x47E	0x47E	N/A	0x47E
DATA5_REG	Reserved	0	0	0	0

NOTE: Although the EEE modes can be different between each speed, the AutogrEEEn parameters for 2.5/5/10G in DATA2_REGs to DATA4_REGs are shared. The 1G/100M AutogrEEEn parameters are not programmable and are unaffected by the values in DATA2_REGs to DATA4_REGs.

DATA1_REG[15:8] = Reserved

Example: When DATA1_REG is 0x00B1, 5G EEE is fixed latency, 2.5G EEE is variable latency, 1G/100M does not advertise EEE, and 10G is native EEE mode. If the data rate is 10G, DATA2_REG to DATA4_REGs are ignored. If the data rate is 5G, DATA4_REG is ignored. If the data rate is 2.5G or 5G, the AutogrEEEn threshold is the same for both.

Return Results: None.

NOTE: CMD_SET_EEE_MODE requires auto-negotiation to take place to take effect.

1.23.1.11 CMD_ GET_EMI_MODE_ENABLE

Description: Gets SW Fast Retrain current enable status.

Input Parameters: None.

Return Results:
DATA1_REG = EMI cancellation value.
1 = Enabled.
0 = Disabled.

1.23.1.12 CMD_SET_EMI_MODE_ENABLE

Description:	Gets SW Fast Retrain current enable status.
Input Parameters: DATA1_REG = EMI enable value. 1 = Enable. 0 = Disable.	**Return Results**: None.
NOTE: CMD_SET_EMI_MODE_ENABLE requires auto-negotiation to take place to take effect.	

1.23.1.13 CMD_GET_SUB_LF_RF_STATUS

Description:	Gets current status on the substitution of FAULTS with IDLE going to the line direction.
Input Parameters: None.	**Return Results**: Status 1 = Substitution is enabled. 0 = Substitution is disabled.

1.23.1.14 CMD_CLEAR_SUB_LF_RF

Description:	Disables substitution of FAULTS with IDLE going to the line direction.
Input Parameters: 1 = Disable substitution.	**Return Results**: None.

1.23.1.15 CMD_SET_SUB_LF_RF

Description:	Enables substitution of FAULTS with IDLE going to the line direction.
Input Parameters: 1 = Enable substitution.	**Return Results**: None.

1.23.1.16 GET_KR_MODE_ENABLE

Description:	Gets KR mode status setting (enable/disable).
Input Parameters: None.	**Return Results**: DATA1: ■ 0 = BCM84891L KR mode is disabled ■ 1 = BCM84891L KR mode is enabled. DATA2 to 5: Reserved

1.23.1.17 SET_KR_MODE_ENABLE

Description:	Sets KR mode status setting (enable/disable).
Input Parameters: DATA1: ■ 0 = BCM84891L KR mode is disabled. ■ 1 = BCM84891L KR mode is enabled. DATA2 to 5: Reserved	**Return Results**: None.

1.23.1.18 GET_XFI_TX_FILTERS

Description:	Gets current XFI TX filter taps.
Input Parameters: DATA1: ■ 0 = XFIM. ■ 1 = XFIL.	**Return Results**: DATA2: ■ Bit [0:7] = Pre tap. ■ Bit [8:15] = Main tap. DATA3: ■ Bit [0:7] = Post1 tap. ■ Bit [8:15] = Post2 tap. DATA4: ■ Bit [0:7] = Post3 tap.

1.23.1.19 SET_XFI_TX_FILTERS

Description:	Sets XFI TX filter taps.
Input Parameters: DATA1: ■ 0 = XFIM. ■ 1 = XFIL. DATA2: ■ Bit [0:7] = Pre tap, ■ Bit [8:15] = Main tap. DATA3: ■ Bit [0:7] = Post1 tap, ■ Bit [8:15] = Post2 tap. DATA4: ■ Bit [0:7] = Post3 tap.	**Return Results**: None.

1.23.1.20 GET_XFI_POLARITY

Description:	Gets XFI polarity.
Input Parameters: DATA1: ■ 0 = XFIM. ■ 1 = XFIL.	**Return Results**: ■ DATA2: TX polarity. ■ DATA3: RX polarity.

1.23.1.21 SET_XFI_POLARITY

Description:	Sets XFI polarity.
Input Parameters: DATA1: ■ 0 = XFIM. ■ 1 = XFIL. DATA2: ■ TX polarity. DATA3: ■ RX polarity.	**Return Results**: None.

1.23.1.22 GET_CURRENT_VOLTAGE

Description:	Gets current voltage.
Input Parameters: None.	**Return Results**: DATA1 = For 1.0V measurement. DATA2 = For 1.0V measurement. DATA3 = For 1.88V measurement. DATA4 = Reserved.

1.23.1.23 CMD_GET_SNR

Description:	Gets SNR value.
Input Parameters: DATA1_REG = 0. User must write 0 every time executing this command.	**Return Results**: DATA2_REG = SNR for Channel A in dB DATA3_REG = SNR for Channel B in dB. DATA4_REG = SNR for Channel C in dB DATA5_REG = SNR for Channel D in dB

1.23.1.24 CMD_GET_CURRENT_TEMP

Description:	Returns the internally derived temperature of the die. DATA1_REG returns the temperature, when supported.
Input Parameters: None.	**Return Results**: DATA1_REG = Temperature value.

1.23.1.25 CMD_SET_UPPER_TEMP_WARNING_LEVEL

Description:	Sets the upper-bound of the temperature warning to the value in DATA1_REG.
Input Parameters: DATA1_REG = Temperature value.	**Return Results**: None.

1.23.1.26 CMD_GET_UPPER_TEMP_WARNING_LEVEL

Description:	Gets the upper-bound of the temperature warning and saves the value to DATA1_REG.
Input Parameters: None.	**Return Results**: DATA1_REG = Temperature value.

1.23.1.27 CMD_SET_LOWER_TEMP_WARNING_LEVEL

Description:	Sets the lower-bound of the temperature warning and saves the value to DATA1_REG.
Input Parameters: DATA1_REG = Temperature value.	**Return Results**: None.

1.23.1.28 CMD_GET_LOWER_TEMP_WARNING_LEVEL

Description:	Gets the lower bound of the temperature warning to the value in DATA1_REG.
Input Parameters: None.	**Return Results**: DATA1_REG = Temperature value.

1.23.1.29 READ_INDIRECT_GPHY_REG_BITS

Description:	Returns current value of indirect GPHY register.
Input Parameters: DATA1: Register group. 0x18 = Shadow 18 registers. 0x1C = Shadow 1C registers. 0xf = Expansion registers. Other = Invalid, returns 0. DATA2: Reserved. DATA3: Mask (Hex value) Number of bits to read. Example 1: 0xFFFF (read all 16 bits). Example 2: 0x3000 (read bit 12 and 13). DATA4: Shift (Dec value) Starting bit to read. Example 1: 0 (read starting from bit 0, based on the Mask value). Example 2: 12 (read starting from bit 12, based on the Mask value). DATA5: Value of bits based on the Mask and Shift (Hex value). Example for reading 0x1C shadow 0xA: Data1 (1e.4038) = 0x1c Data2 (1e.4039) = 0xA Data3 (1e.403A) = 0xffff Data4 (1e.403B) = 0 CMD (1e.4005) = 0x8014 Data5 (1e.403C) provides the 16 bits value of indirect register access of 0x1C shadow 0xA.	**Return Results**: DATA5 = Register bits value.

1.23.1.30 WRITE_INDIRECT_GPHY_REG_BITS

Description: Writes value to indirect GPHY register.	
Input Parameters: DATA1: Register group. 0x18 = Shadow 18 registers. 0x1C = Shadow 1C registers. 0xf = Expansion registers. Other = Invalid, do nothing. DATA2: Reserved. DATA3: Mask (Hex value) Number of bits to write. Example 1: 0xFFFF (write all 16 bits). Example 2: 0x3000 (write to bit 12 and 13). DATA4: Shift (Dec value) starting bit to write. Example 1: 0 (write starting from bit 0, based on the Mask value). Example 2: 12 (write starting from bit 12, based on the Mask value). DATA5: Value of bits to be written (Hex value). Example 1: 0xA5A5 (Value for all 16 bits). Example 2: 0x3 (set bit 12 and 13 to 1).	**Return Results**: None.

1.23.1.31 GET_802.3BZ_PRIORITY

Description: —	
Input Parameters: None.	**Return Results**: DATA1: 0 = Reserved DATA1: 1 = Priority protocol is to IEEE 802.3bz. DATA2: Current link frame type. ■ 0 = Reserved ■ 1 = IEEE 802.3bz ■ 2 = NBASE-T ■ 3 = Reserved DATA3 to DATA5: Reserved.

1.23.1.32 SET_802.3BZ_PRIORITY

Description: —	
Input Parameters: DATA1: 1 = Set IEEE 802.3bz to be the priority protocol to link.	**Return Results**: None.

1.23.1.33 GET_XFI_2P5G_5G_MODE

Description: —	
Input Parameters: None.	**Return Results**: DATA1: 0 = 10G idle stuffing mode for 2.5G. 1 = 2500BASE-X_5000BASE-X mode for 2.5G. 2 = 2500BASE-R_5000BASE-R mode for 2.5G. DATA2: 0 = 10G idle stuffing mode for 5G. 1 = 25000BASE-X_5000BASE-X mode for 5G. 2 = 2500BASE-R_5000BASE-R mode for 5G. DATA3 to DATA5: Not used.

1.23.1.34 SET_XFI_2P5G_5G_MODE

Description: —	
Input Parameters: DATA1: 0 = 10G idle stuffing mode for 2.5G. 1 = 2500BASE-X_5000BASE-X mode for 2.5G. 2 = 2500BASE-R_5000BASE-R mode for 2.5G. DATA2: 0 = 10G idle stuffing mode for 5G. 1 = 25000BASE-X_5000BASE-X mode for 5G. 2 = 2500BASE-R_5000BASE-R mode for 5G. DATA3 to DATA5: Not used.	**Return Results**: None.
NOTE: KR mode is not supported when 2500X or 5000X mode is enabled.	

1.23.1.35 GET_EEE_STATISTICS

Description: —	
Input Parameters: Counter selection: 0 = Select event counters. 1 = Select time duration.	**Return Results**: DATA2: TX (LOC) counters/time lower 16 bits. DATA3: TX (LOC) counters/time upper 16 bits. DATA4: RX (REM) counters/time lower 16 bits. DATA5: RX (REM) counters/time upper 16 bits.
NOTE: PHY selects 10G or 1G based on current link speed.	

1.23.1.36 GET_JUMBO_PACKET

Description: Gets jumbo packet status setting (enable/disable).	
Input Parameters: None.	**Return Results**: DATA1: Current jumbo packet enable status. ■ 0 = Jumbo packet is disabled. ■ 1 = Jumbo packet is enabled. DATA2 to 5: Not used.

1.23.1.37 SET_JUMBO_PACKET

Description:	Sets jumbo packet status setting (enable/disable).
Input Parameters: DATA1: Enable or disable jumbo packet. 0 = Disable jumbo packet. 1 = Enable jumbo packet. DATA2 to 5: Not used.	**Return Results**: None.

1.23.1.38 GET_PAUSE_FRAME_MODE

Description:	Gets the pause frame mode status (enable/disable).
Input Parameters: None.	**Return Results**: DATA1: Pause frame enable status. ■ 0 = No pause frame. ■ 1 = Pause frame is enabled. DATA2 to 5: Reserved.

1.23.1.39 SET_PAUSE_FRAME_MODE

Description:	Sets the pause frame mode status (enable/disable).
Input Parameters: DATA1: Pause frame enable status. ■ 0 = No pause frame. ■ 1 = Pause frame is enabled.	**Return Results**: None.

1.23.1.40 GET_USXGMII

Description:	Gets the USXGMII mode and AUTONEG function (enable/disable).
Input Parameters: None.	**Return Results**: DATA1: USXGMII enable status. ■ 0 = USXGMII is disabled. ■ 1 = USXGMII is enabled. DATA2: USXGMII AUTONEG enable status. ■ 0 = AUTONEG is disabled. ■ 1 = AUTONEG is enabled. DATA3 to DATA5: Reserved.

1.23.1.41 SET_USXGMII

Description:	Sets the USXGMII mode and AUTONEG function (enable/disable).
Input Parameters: DATA1: USXGMII enable status. ■ 0 = USXGMII is disabled. ■ 1 = USXGMII is enabled. DATA2: USXGMII AUTONEG enable status. ■ 0 = AUTONEG is disabled. ■ 1 = AUTONEG is enabled. DATA3 to DATA5: Reserved.	**Return Results**: None.

1.24 General-Purpose LED Programmability

The BCM84891L has five LED pins. These LED pins can be functionally programmed, and are referred to in this document as LED1 through LED5. control register words are provided to enable the selection of LED functions for each of the pins. These control words are located in register LED Control (DEVAD = 1, Address = 0xA83B). For each of the five programmable LEDs, their corresponding register bits, and default settings.

The LED sources are masked in the Control LEDx Mask register. LED mask bit should be set to 1 to allow the source to driver the LED pin. When multiple bits in the Control LEDx Mask register are set, the LED sources are OR'd together.

The LEDs are controlled by the LED Control (DEVAD = 1, Address = 0xA83B). The LED Control Source (DEVAD = 1, Address = 0xA83C) registers drives the LED signals on the pins when the mask associated with the LED is set to enable the bit.

In 10G mode, each LED is controlled separately by the individual bits of the PHYC_CTL_LED_CTL. The LEDx_OE_N enables the LEDx output. LEDx_CTL controls the mode of operation of LEDx.

- When set to 00, the LED is off.
- When set to 01, the LED blinks based on the selected source. The blink cycle is programmed by 10GBASE-T Control LEDx bit [3:0].
- When set to 10, the LED is ON based on the selected source registers.
- 11 is reserved.

Each of the five LEDs has a maskable source registers bit. See Table 10.

Activity LED can be enabled by unmasking bit 1 (for receiver activity) or/and bit 2 (for transmitter activity) in the LED associated Control LEDx Mask registers. The LED Control Source (DEVAD = 1, Address = 0xA83C) bit 1 provides receiver activity status, and bit 2 provides transmitter activity status. When both bits are set, the activity LEDs indicated activity of transmitter and receiver. To make the activity pulse visible to eye, the Stretch_En bit associate for the selected LED pin to use as activity LED signal should be set to 1.

NOTE: LED4 provides the link status. The firmware initializes the LED4 mask register DEVAD 1, 0xA835 to the default value of 0x0040 to enable the LED for link status. LED4 is under firmware control regardless of the Config 11 pins strapping.

NOTE: Use the read-modify-write operation when changing bits in the register LED Control (DEVAD = 1, Address = 0xA83B). LED 4 is set by the firmware to provide link status.

NOTE: Even though the LED control registers are named as 10GBASE-T LED, they apply to 1000BASE-T as well as 100BASE-TX mode.

Table 10: LEDs Maskable Source Registers

Source	Description
0	Reserved.
1	RX activity is on.
2	TX activity is on.
3:4	11 = Linked at 1000BASE-T. 10 = Linked at 100BASE-T. 01 = Reserved. 00 = Reserved.
5	Always set to 1.
6	Reserved.
7	1 = 10G copper link status is up. 0 = 10G copper link status is down.
8	Reserved.
9:15	Reserved.

Table 11: LEDs Maskable Source 2 Registers

Source	Description
0	Reserved.
1	Reserved.
2	1 = 2.5G link up. 0 = 2.5G link down.
3	1 = 5G link up. 0 = 5G link down.
4:15	Reserved.

The default firmware configuration provides the following behavior to the five LEDS for each port only when Config 11 is strap low and the LED function is predefined and configured by firmware.

10GBASE-T/5GBASE-T/2.5GBASE-T

- LED 1 ON = Master; OFF = Slave
- LED 2 BLINK = Training; ON = 5 or 2.5G link is up; OFF = 5 or 2.5G link is down
- LED 3 BLINK = TX/RX traffic activity; OFF = No traffic
- LED 4 ON = Copper link is up; OFF = Copper link is down
- LED 5 ON = 10G/5G/2.5G copper link is up; OFF = 10G/5G/2.5G copper link is down

1000/100BASE-T

- LED 1/LED2 ON/ON = Link at 1G; OFF/ON = Link at 100M
- LED 3 BLINK = TX/RX traffic activity; OFF = No traffic
- LED 4 ON = Copper link is up; OFF = copper link is down
- LED 5 is not used

1.25 Power Supplies

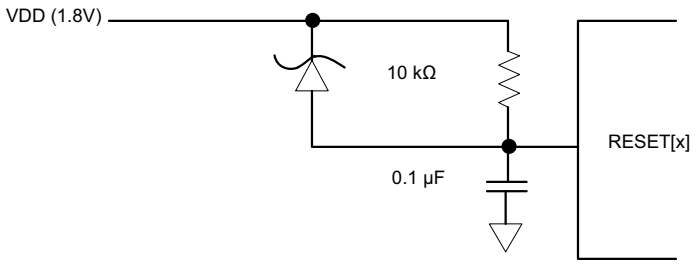
The analog core operates at 1.0V and 1.88V. The digital core section operates at +1.0V. The CMOS I/Os operate in two groups, with the MDIO group at 1.2V or 2.5V, and with all the digital group operating at 1.88V (except some I/Os are tolerant to 3.3V, see Table 206).

1.26 Reset

To issue a soft reset to the BCM84891L, the user must perform the following sequence:

1. Write DEVAD 0x1E register address 0x4191 = 0x0001.
2. Wait 200 µs.
3. Write DEVAD =1/3 0x0000 bit 15 = 1.
4. Check DEVAD = 1/3 for 0x2040 value by firmware to acknowledge of completion of soft reset operation.

Figure 16: External Reset



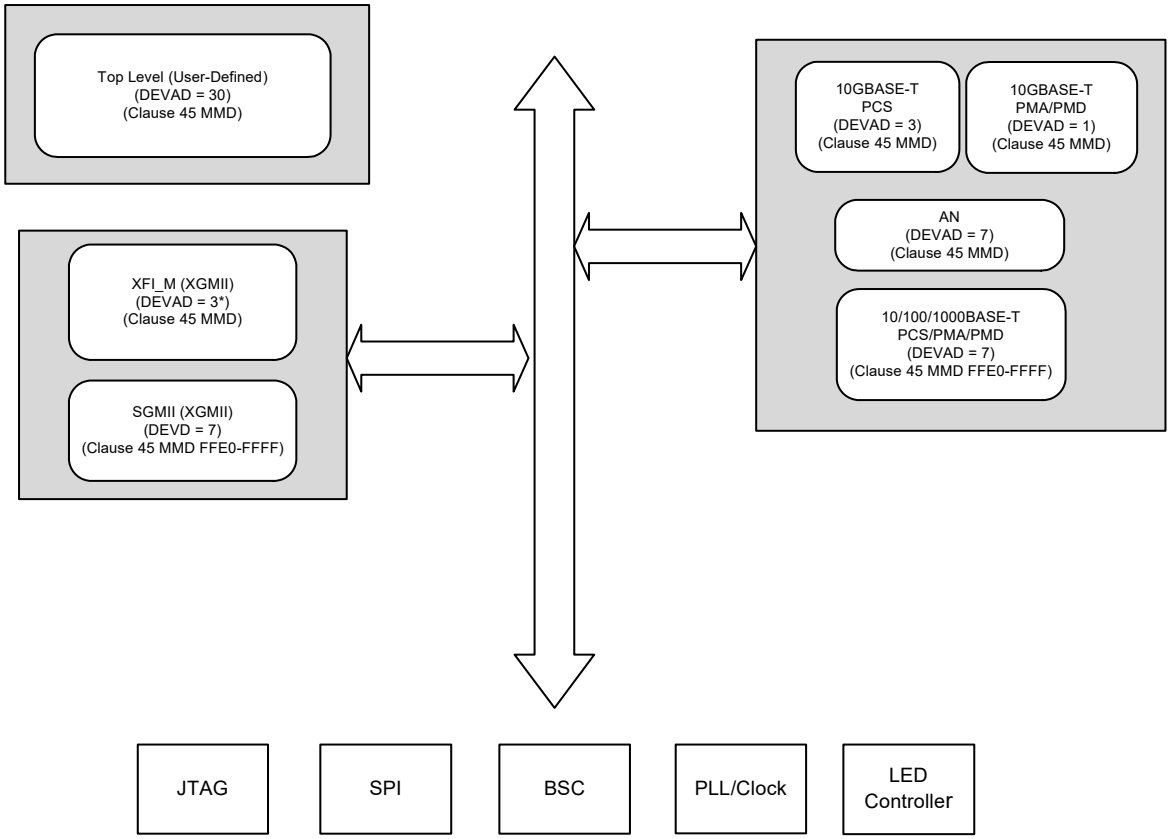
Chapter 2: Register Summary

2.1 Accessing Registers through MDC/MDIO Management Interfaces

2.1.1 Register Programming

The BCM84891L registers are accessed through serial interface MDC and MDIO pins with a unique PRTAD. Each BCM84891L port has a unique address based on the PRTAD[0:4] pins state. These pins are latched on the rising edge of the RESET_P01/P23 signal. Each time an MDIO write or read operation is executed, the BCM84891L compares the port address of the MDIO frame with its own port addresses. The requested operation is executed only when the MDIO frame address matches the port address of the BCM84891L.

Figure 17: BCM84891L Device Addresses



The BCM84891L operates under the IEEE 802.3 Clause 45 management access protocol. A clock must be provided to the BCM84891L at a rate of 0 MHz to 25 MHz through the MDC pins. The serial data is communicated on the MDIO pins. Every MDIO bit must have the same period as the MDC clock. The MDIO bits are latched on the rising edge of the MDC clock.

2.1.1.1 IEEE P802.3ae Extension Frame Register Access Clause 45 Mode

Table 12: IEEE P802.3ae MDIO Extension Frame Format (ST = 00)

Operation	PRE	ST	OP	PRTAD	DEVAD	TA	DATA	IDle	Direction
ADDRESS	1 ... 1	00	00	PPPPP	EEEEE	10	A ... A	Z	Driven to BCM84891L
READ	1 ... 1	00	11	PPPPP	EEEEE	ZZ Z0	Z ... Z D ... D	Z Z	Driven to BCM84891L Driven by BCM84891L
READ INCR.	1 ... 1	00	10	PPPPP	EEEEE	ZZ Z0	Z ... Z D ... D	Z Z	Driven to BCM84891L Driven by BCM84891L
WRITE	1 ... 1	00	01	PPPPP	EEEEE	10	D ... D	Z	Driven to BCM84891L

Preamble (PRE): Thirty-two consecutive 1 bits must be sent through the MDIO pin to the BCM84891L to signal the beginning of an instruction. Fewer than thirty-two 1 bits cause the remainder of the instruction to be ignored.

Start of Frame (ST): A 00 pattern indicates that the start of the instruction follows.

Operation Code (OP): A WRITE ADDRESS instruction is indicated by 00. A READ DATA instruction is indicated by 11. A READ DATA AND THEN INCREMENT ADDRESS instruction is indicated by a 10. A WRITE DATA instruction is indicated by 01.

Port Address (PRTAD): A 5-bit port address follows, with the most-significant bit (MSB) transmitted first.

Device Address (DEVAD): A 5-bit device address follows, with the MSB transmitted first.

Turnaround (TA): The next two bit times are used to avoid contention on the MDIO pin when a read operation is performed. For a write operation, 10 must be sent to the BCM84891L during these two bit times. For a read operation, the MDIO pin must be placed into high-impedance during these two bit times. The chip drives the MDIO pin to 0 during the second bit time.

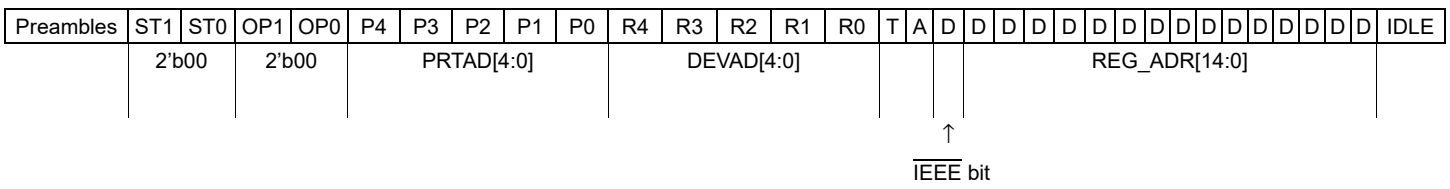
Data (DATA): The last 16 bits of the frame are the actual data bits (or address bits for ADDRESS WRITEs). For a write operation, these bits are sent to the BCM84891L transceiver, whereas, for a read operation, these bits are driven by the BCM84891L transceiver. In either case, the MSB is transmitted first.

When writing to the BCM84891L transceiver, the data field bits must be stable 10 ns before the rising-edge of MDC, and must be held valid for 10 ns after the rising edge of MDC. When reading from the BCM84891L transceiver, the data field bits are valid after the rising-edge of MDC until the next rising edge of MDC.

Idle (IDle): A high-impedance state of the MDIO line. The MDIO tristate driver is disabled, and the pull-up resistor pulls the MDIO line to logic 1.

The format of the IEEE P802.3ae Extension Frame is shown in the table below.

Table 13: Indirect Register Addressing for IEEE P802.3ae Extension Frame Mode (ST = 00)



In IEEE P802.3ae Extension Frame mode, to access a register, the register's block number (6 bits) and address (4 bits) must first be written to the Address register using a write with the Operation Code (OP) field set to 00. The IEEE registers and non-IEEE registers are accessed as follows:

IEEE Registers: There is a special block of registers for IEEE functions. This block is accessed whenever DATA bit 15 is low (0) during a write to the address register, regardless of the contents of the Block Address field.

Chip-specific Registers: To access the non-IEEE registers, data bit 15 must be high (1) during a write to the Address register.

2.2 Register Maps

The BCM84891L has integrated PMAPMD/PCS/AN for XFI/10GBASE-KR and PMAPMD/PCS/AN for 10G/1000/100BASE-T sublayers functions per-port. All BCM84891L MDIO registers are accessible through device addresses (DEVADs), per clause 45 of IEEE 802.3 IEEE standards. The BCM84891L XFI/10GBASE-KR interface for PMAPMD/PCS/AN (1, 3, 7) sublayer registers uses the same device address (DEVAD) as 10G/1000/100BASE-T PMAPMD/PCS/AN (1, 3, 7) sublayers for the line side. To select between two sets of common DEVAD sublayers, program a set of base-pointer registers before performing MDIO read/write operations and accessing the required MDIO register. After PHY is reset, these base pointer registers are initialized by firmware to point to 10G/1000/100BASE-T DEVAD for PMAPMD/PCS/AN (1, 3, 7) line-side interface sublayers as default.

The BCM84891L XFI/10GBASE-KR supports an additional device address (DEVAD) of zero (0) for accessing the XFI/10GBASE-KR 1000BASE-X registers for SGMII. Device address zero (0) is accessible through the base-pointer registers setting for the MAC side.

- Base-pointer mode MAC side: To access PMAPMD/PCS/AN for XFI/10GBASE-KR (DEVADs 1, 3, 7), use the following base-pointer registers.
  a. Write DEVAD = 30, Register 0x4110 = 0x2004
  b. Write DEVAD = 30, Register 0x4111 = 0x2004
  c. Write DEVAD = 30, Register 0x4113 = 0x2004
- Base-pointer mode line-side: To access PMD/PCS/AN for 10G/1000/100BASE-T (DEVADs 1, 3, 7), use the following base-pointer registers.
  d. Write DEVAD = 30, Register 0x4110 = 0x0001
  e. Write DEVAD = 30, Register 0x4111 = 0x0001
  f. Write DEVAD = 30, Register 0x4113 = 0x1002

CAUTION! If the base-pointers are not set correctly, the MDIO read or write operation is performed to a different MDIO register.

2.3 Register Notations

In the register description tables, the following notation in the R/W column describes the read or write ability:

- R/W = Read or write
- RO = Read only
- LH = Latched high
- LL = Latched low
- H = Fixed high
- L = Fixed low
- SC = Self-clearing
- CR = Clear on reset

Reserved bits must be written as the default value and ignored when read.

2.4 10GBASE-T Register

2.4.1 10GBASE-T Register Description (DEVAD = 1 PMA)

2.4.1.1 PMA/PMD Control 1 Register (DEVAD = 1, Address = 0x0000)

Table 14: PMA/PMD Control 1 Register (1.0x0000)

Bit	Name	R/W	Description	Default
15	RESET	SC	1 = PMA/PMD reset. 0 = Normal operation.	0
14	Reserved	R/W	Use read-modify-write to not change the current value during write. Ignore on read.	Undetermined
13	SPEED_SEL_0	R/W	Combined with bit 6 selects the speed. 6 13 1 1 = Bits 5:2 select speed 1 0 = 1000 Mb/s 0 1 = 100 Mb/s 0 0 = Reserved	0
12	Reserved	R/W	Use read-modify-write to not change the current value during write. Ignore on read.	Undetermined
11	LOW_PWR	R/W	1 = Low-power mode. 0 = Normal operation.	0
10:7	Reserved	R/W	Use read-modify-write to not change the current value during write. Ignore on read.	Undetermined
6	SPEED_SEL_1	R/W	See bit 13.	0

Table 14: PMA/PMD Control 1 Register (1.0x0000) (Continued)

Bit	Name	R/W	Description	Default
5:2	SPEED_SEL_10G	R/W	5 4 3 2 1 x x x = Reserved 0 1 1 1 = 5 Gb/s 0 1 1 0 = 2.5 Gb/s 0 1 0 1 = 400 Gb/s 0 1 0 0 = 25 Gb/s 0 0 1 1 = 100 Gb/s 0 0 1 0 = 40 Gb/s 0 0 0 1 = 10PASS-TS/2BASE-TL 0 0 0 0 = 10 Gb/s	0x0
1	Reserved	R/W	Use read-modify-write to not change the current value during write. Ignore on read.	Undetermined
0	LPBK	R/W	1 = Enable PMA/PMD loopback mode. 0 = Disable PMA/PMD loopback mode.	0

2.4.1.2 PMA/PMD Status 1 Register (DEVAD = 1, Address = 0x0001)

Table 15: PMA/PMD Status 1 Register (1.0x0001)

Bit	Name	R/W	Description	Default
15:8	Reserved	RO	Ignore on read.	Undetermined
7	FAULT	RO	1 = Fault condition detected. 0 = Fault condition not detected.	0
6:3	Reserved	RO	Ignore on read.	Undetermined
2	RCV_LINK_ST	LL	Receive link status 1 = PMA/PMD receive link up. 0 = PMA/PMD receive link down.	0
1	CAP_LOW_PWR	RO	Low-power ability 1 = PMA/PMD supports low-power mode. 0 = PMA/PMD does not support low-power mode.	1
0	Reserved	RO	Ignore on read.	Undetermined

2.4.1.3 PMA/PMD Device Identifier Part 0 (DEVAD = 1, Address = 0x0002)

Table 16: PMA/PMD Device Identifier Part 0 (1.0x0002)

Bit	Name	R/W	Description	Default
15:0	DEV_ID0	RO	Combined with PMA_DEV_ID1 forms the PMA/PMD device identifier.	0x3590

2.4.1.4 PMA/PMD Device Identifier Part 1 (DEVAD = 1, Address = 0x0003)

Table 17: PMA/PMD Device Identifier Part 1 (1.0x0003)

Bit	Name	R/W	Description	Default
15:0	DEV_ID1	RO	Combined with PMA_DEV_ID0 forms the PMA/PMD device identifier.	A0: 0x5080 B0: 0x5081

2.4.1.5 PMA/PMD Speed Ability (DEVAD = 1, Address = 0x0004)

Table 18: PMA/PMD Speed Ability (1.0x0004)

Bit	Name	R/W	Description	Default
15	Reserved	RO	Ignore on read.	Undetermined
14	CAP5G	RO	1 = PMA/PMD has 2.5G/5G extended abilities listed in register 1.0x0021. 0 = PMA/PMD does not have 2.5G/5G abilities. Reset value is 0x1.	0x1
13	CAP2p5G	RO	Reset value is 0x0.	0x0
10	CAP_40G_100G	RO	1 = PMA/PMD has 40G/100G extended abilities listed in register 1.0x0013. 0 = PMA/PMD does not have 40G/100G abilities. Reset value is 0x0.	0x0
9	CAP_P2MP	RO	1 = PMA/PMD has P2MP abilities listed in register 1.0x0012. 0 = PMA/PMD does not have P2MP abilities. Reset value is 0x0.	0x0
8	Reserved	RO	—	—
7	CAP_100B_TX	RO	1 = PMA/PMD can perform 100BASE-TX. 0 = PMA/PMD cannot perform 100BASE-TX. Reset value is 0x1.	0x1
6	CAP_10GB_KX	RO	1 = PMA/PMD can perform 10GBASE-KX. 0 = PMA/PMD cannot perform 10GBASE-KX. Reset value is 0x0.	0x0
5	CAP_100M	RO	100M capable 1 = PMA/PMD is capable of operating at 100 Mb/s. 0 = PMD/PMD is not capable of operating at 100 Mb/s.	1
4	CAP_1000M	RO	1000M capable 1 = PMA/PMD is capable of operating at 1000 Mb/s. 0 = PMD/PMD is not capable of operating at 1000 Mb/s.	1
3	Reserved	RO	Ignore on read.	Undetermined
2	CAP_10PASS_TS	RO	10PASS-TS capable 1 = PMA/PMD is capable of operating at 10PASS-TS. 0 = PMD/PMD is not capable of operating at 10PASS-TS.	0
1	CAP_2BASE_TL	RO	2BASE-TL capable 1 = PMA/PMD is capable of operating at 2BASE-TL. 0 = PMD/PMD is not capable of operating at 2BASE-TL.	0
0	CAP_10G	RO	10G capable 1 = PMA/PMD is capable of operating at 10 Gb/s. 0 = PMD/PMD is not capable of operating at 10 Gb/s.	1

2.4.1.6 Devices in Package Register Part 0 (DEVAD = 1, Address = 0x0005)

Table 19: Devices In Package Register Part 0 (1.0x0005)

Bit	Name	R/W	Description	Default
15:8	Reserved	RO	Ignore on read.	Undetermined
7	AUTONEG_PRE	RO	Auto-negotiation present. 1 = Auto-negotiation present in package. 0 = Auto-negotiation not present in package.	1
6	TC_PRE	RO	TC present. 1 = TC present in package. 0 = TC not present in package.	0
5	DTEXS_PRE	RO	Data Terminal Equipment (DTE) XS present. 1 = DTE XS present in package. 0 = DTE XS not present in package.	0
4	PHYXS_PRE	RO	PHY XS present. 1 = PHY XS present in package. 0 = PHY XS not present in package.	1
3	PCS_PRE	RO	PCS present. 1 = PCS present in package. 0 = PCS not present in package.	1
2	WIS_PRE	RO	WIS present. 1 = WIS present in package. 0 = WIS not present in package.	0
1	PMD_PRE	RO	PMD/PMA present. 1 = PMD/PMA present in package. 0 = PMD/PMA not present in package.	1
0	CLA22_PRE[a]	RO	Clause 22 registers present. 1 = Clause 22 registers present in package. 0 = Clause 22 registers not present in package.	1

a. Clause 22 registers are accessible through Clause 45.

2.4.1.7 Devices in Package Register Part 1 (DEVAD = 1, Address = 0x0006)

Table 20: Devices in Package Register Part 1 (1.0x0006)

Bit	Name	R/W	Description	Default
15	VENSP_DEV2_PRE	RO	Vendor-specific device 2 present. 1 = Vendor-specific device 2 present in package. 0 = Vendor-specific device 2 not present in package.	1
14	VENSP_DEV1_PRE	RO	Vendor-specific device 1 present. 1 = Vendor-specific device 1 present in package. 0 = Vendor-specific device 1 not present in package.	1
13	CLA22_EXT_PRE	RO	Clause 22 extension present. 1 = Clause 22 extension present in package. 0 = Clause 22 extension not present in package.	0
12:0	Reserved	RO	Ignore on read.	Undetermined

2.4.1.8 PMA/PMD Control 2 Register (DEVAD = 1, Address = 0x0007)

Table 21: PMA/PMD Control 2 Register (1.0x0007)

Bit	Name	R/W	Description	Default
15:6	Reserved	R/W	Use read-modify-write to not change the current value during write. Ignore on read.	Undetermined
5:0	TYPE_SEL	R/W	MA/PMD type selection: 5 4 3 2 1 0 1 1 0 0 0 1 = 5GBASE-T PMA type 1 1 0 0 0 0 = 2.5GBASE-T PMA type 0 0 1 1 1 1 = 10BASE-T PMA type 0 0 1 1 1 0 = 100BASE-T PMA/PMD type 0 0 1 1 0 1 = 10GBASE-KX PMA/PMD type 0 0 1 1 0 0 = 1000BASE-T PMA type 0 0 1 0 1 1 = 10GBASE-KR PMA/PMD type 0 0 1 0 1 0 = 10GBASE-KX4 PMA/PMD type 0 0 1 0 0 1 = 10GBASE-T PMA type 0 0 1 0 0 0 = 10GBASE-LRM PMA/PMD type 0 0 0 1 1 1 = 10GBASE-SR PMA/PMD type 0 0 0 1 1 0 = 10GBASE-LR PMA/PMD type 0 0 0 1 0 1 = 10GBASE-ER PMA/PMD type 0 0 0 1 0 0 = 10GBASE-LX4 PMA/PMD type 0 0 0 0 1 1 = 10GBASE-SW PMA/PMD type 0 0 0 0 1 0 = 10GBASE-LW PMA/PMD type 0 0 0 0 0 1 = 10GBASE-EW PMA/PMD type 0 0 0 0 0 0 = 10GBASE-CX4 PMA/PMD type Reset value is 0x9.	0x9

2.4.1.9 10G PMA/PMD Status 2 Register (DEVAD = 1, Address = 0x0008)

Table 22: 10G PMA/PMD Status 2 Register (1.0x0008)

Bit	Name	R/W	Description	Default
15:14	DEV_PRE	RO	Device present 1 0 = Device responding at this address. 1 1 = No device responding at this address. 0 1 = No device responding at this address. 0 0 = No device responding at this address. Reset value is 2.	2
13	CAP_TRAN_FALT	RO	Transmit fault ability. 1 = PMA/PMD can detect a fault condition on the transmit path. 0 = PMA/PMD cannot detect a fault condition on the transmit path.	0
12	CAP_RCV_FALT	RO	Receive fault ability 1 = PMA/PMD can detect a fault condition on the receive path. 0 = PMA/PMD cannot detect a fault condition on the receive path.	1

Table 22: 10G PMA/PMD Status 2 Register (1.0x0008) (Continued)

Bit	Name	R/W	Description	Default
11	TRAN_FALT	RO	Transmit fault If no ability, should be reserved. 1 = Fault condition on transmit path. 0 = No fault condition on transmit path.	0
10	RCV_FALT	LH	Receive fault 1 = Fault condition on receive path 0 = No fault condition on receive path	1
9	CAP_EXT	RO	Extended abilities 1 = PMA/PMD has the extended abilities listed in register 1.0x000B. 0 = PMA/PMD does not have extended abilities.	1
8	CAP_TRAN_DIS	RO	PMD transmit disable abilities 1 = PMD can disable the transmit path. 0 = PMD cannot disable the transmit path.	1
7	CAP_10G_SR	RO	10GBASE_SR ability 1 = PMA/PMD can perform 10GBASE-SR. 0 = PMA/PMD cannot perform 10GBASE-SR.	0
6	CAP_10G_LR	RO	10GBASE_LR ability 1 = PMA/PMD can perform 10GBASE-LR. 0 = PMA/PMD cannot perform 10GBASE-LR.	0
5	CAP_10G_ER	RO	10GBASE_ER ability 1 = PMA/PMD can perform 10GBASE-ER. 0 = PMA/PMD cannot perform 10GBASE-ER.	0
4	CAP_10G_LX4	RO	10GBASE_LX4 ability 1 = PMA/PMD can perform 10GBASE-LX4. 0 = PMA/PMD cannot perform 10GBASE-LX4.	0
3	CAP_10G_SW	RO	10GBASE_SW ability 1 = PMA/PMD can perform 10GBASE-SW. 0 = PMA/PMD cannot perform 10GBASE-SW.	0
2	CAP_10G_LW	RO	10GBASE_LW ability 1 = PMA/PMD can perform 10GBASE-LW. 0 = PMA/PMD cannot perform 10GBASE-LW.	0
1	CAP_10G_EW	RO	10GBASE_EW ability 1 = PMA/PMD can perform 10GBASE-EW. 0 = PMA/PMD cannot perform 10GBASE-EW.	0
0	CAP_LPBK	RO	PMA loopback ability 1 = PMA can perform loopbacks. 0 = PMA cannot perform loopbacks.	1

2.4.1.10 10G PMA/PMD Transmit Disable (DEVAD = 1, Address = 0x0009)

Table 23: 10G PMA/PMD Transmit Disable (1.0x0009)

Bit	Name	R/W	Description	Default
15:5	Reserved	R/W	Use read-modify-write to not change the current value during write. Ignore on read.	Undetermined
4	TRAN_DIS4	R/W	PMD transmit disable 4 1 = Disable output on transmit lane 4. 0 = Enable output on transmit lane 4.	0
3	TRAN_DIS3	R/W	PMD transmit disable 3 1 = Disable output on transmit lane 3. 0 = Enable output on transmit lane 3.	0
2	TRAN_DIS2	R/W	PMD transmit disable 2 1 = Disable output on transmit lane 2. 0 = Enable output on transmit lane 2.	0
1	TRAN_DIS1	R/W	PMD transmit disable 1 1 = Disable output on transmit lane 1. 0 = Enable output on transmit lane 1.	0
0	GLB_TRAN_DIS	R/W	Global PMD transmit disable 1 = Disable transmit output. 0 = Enable transmit output.	0

2.4.1.11 10G PMD Receive Signal Detect (DEVAD = 1, Address = 0x000A)

Table 24: 10G PMD Receive Signal Detect (1.0x000A)

Bit	Name	R/W	Description	Default
15:5	Reserved	RO	Ignore on read.	Undetermined
4	RCV_DET4	RO	PMD receive signal detect 4 1 = Signal detected on receive lane 4. 0 = Signal not detected on receive lane 4.	0
3	RCV_DET3	RO	PMD receive signal detect 3 1 = Signal detected on receive lane 3. 0 = Signal not detected on receive lane 3.	0
2	RCV_DET2	RO	PMD receive signal detect 2 1 = Signal detected on receive lane 2. 0 = Signal not detected on receive lane 2.	0
1	RCV_DET1	RO	PMD receive signal detect 1 1 = Signal detected on receive lane 1. 0 = Signal not detected on receive lane 1.	0
0	GLB_RCV_DET	RO	Global PMD receive signal detect 1 = Signal detected on receive. 0 = Signal not detected on receive.	0

2.4.1.12 10G PMA/PMD Extended Ability (DEVAD = 1, Address = 0x000B)

Table 25: 10G PMA/PMD Extended Ability (1.0x000B)

Bit	Name	R/W	Description	Default
15	Reserved	RO	Ignore on read.	Undetermined
14	CAP_2P5G_5G	RO	1 = PMA/PMD has 2.5G/5G extended abilities listed in register 1.21. 0 = PMA/PMD does not have 2.5G/5G abilities. Reset value is 0x1.	0x1
13:8	Reserved	RO	Ignore on read.	Undetermined
7	CAP_100B_TX	RO	100BASE_TX ability 1 = PMA/PMD can perform 100BASE-TX. 0 = PMA/PMD cannot perform 100BASE-TX.	1
6	Reserved	RO	Ignore on read.	Undetermined
5	CAP_1000B_T	RO	1000BASE_T ability 0 = PMA/PMD can perform 1000BASE-T. 1 = PMA/PMD cannot perform 1000BASE-T.	1
4:3	Reserved	RO	Ignore on read.	Undetermined
2	CAP_10GB_T	RO	10GBASE_T ability 1 = PMA/PMD can perform 10GBASE-T. 0 = PMA/PMD cannot perform 10GBASE-T.	10
1	Reserved	RO	Ignore on read.	Undetermined
0	CAP_10GB_CX4	RO	10GBASE_CX4 ability 1 = PMA/PMD can perform 10GBASE-CX4. 0 = PMA/PMD cannot perform 10GBASE-CX4.	0

2.4.1.13 PMA/PMD Package Identifier (DEVAD = 1, Address = 0x000E)

Table 26: PMA/PMD Package Identifier (1.0x000E)

Bit	Name	R/W	Description	Default
15:0	PKG_ID_0	RO	PMA/PMD package identifier part 0.	0

2.4.1.14 PMA/PMD Package Identifier (DEVAD = 1, Address = 0x000F)

Table 27: PMA/PMD Package Identifier (1.0x000F)

Bit	Name	R/W	Description	Default
15:0	PKG_ID_1	RO	PMA/PMD package identifier part 1.	0

2.4.1.15 10GBASE-T Status (DEVAD = 1, Address = 0x0081)

Table 28: 10GBASE-T Status (1.0x0081)

Bit	Name	R/W	Description	Default
15:1	Reserved	RO	Ignore on read.	Undetermined
0	LP_INFO_VAL	RO	LP information valid 1 = Link partner information is valid. 0 = Link partner information is invalid.	0

2.4.1.16 PMD_IEEE_EXT_AB_2P5G_5G to 2.5G/5G PMA/PMD Extended Ability (DEVAD =1, Address =0x0015)

Table 29: PMD_IEEE_EXT_AB_2P5G_5G to 2.5G/5G PMA/PMD Extended Ability (1.0x0015)

Bit	Name	R/W	Description	Default
15:6	Reserved	RSVD	Reserved bits write has no effect and read always returns 0.	Undetermined
5:2	SPARE	RO	Spare for New Ability.	0x0
1	CAP_5GB_T	RO	1 = PMA/PMD can perform 5GBASE-T. 0 = PMA/PMD cannot perform 5GBASE-T.	0x1
0	CAP_2P5GB_T	RO	1 = PMA/PMD can perform 2.5GBASE-T. 0 = PPMA/PMD cannot perform 2.5GBASE-T.	0x1

2.4.1.17 10GBASE-T Pair Swap and Polarity (DEVAD = 1, Address = 0x0082)

Table 30: 10GBASE-T Pair Swap and Polarity (1.0x0082)

Bit	Name	R/W	Description	Default
15:12	Reserved	RO	Ignore on read.	Undetermined
11	PAIR_D_POL	RO	Pair D polarity 1 = Polarity of pair D is reversed. 0 = Polarity of pair D is not reversed.	0
10	PAIR_C_POL	RO	Pair c polarity 1 = Polarity of pair C is reversed. 0 = Polarity of pair C is not reversed.	0
9	PAIR_B_POL	RO	Pair B polarity 1 = Polarity of pair B is reversed. 0 = Polarity of pair B is not reversed.	0
8	PAIR_A_POL	RO	Pair A polarity 1 = Polarity of pair A is reversed. 0 = Polarity of pair A is not reversed.	0
7:2	Reserved	RO	Ignore on read.	Undetermined
1:0	MDI_XCON	RO	MDI/MD-X connection 1 0 1 1 = No crossover 1 0 = Pair A/B crossover only 0 1 = Pair C/D crossover only 0 0 = Pair A/B and pair C/D crossover Reset value is 3.	3

2.4.1.18 10GBASE-T TX Power Backoff and PHY Limited Reach Setting (DEVAD = 1, Address = 0x0083)

Table 31: 10GBASE-T TX Power Backoff and PHY Limited Reach Setting (1.0x0083)

Bit	Name	R/W	Description	Default
15:13	LP_TX_PWRBK_SET	RO	Link partner TX power backoff setting: 15 14 13 1 1 1 = 14 dB 1 1 0 = 12 dB 1 0 1 = 10 dB 1 0 0 = 8 dB 0 1 1 = 6 dB 0 1 0 = 4 dB 0 0 1 = 2 dB 0 0 0 = 0 dB Reset value is 2.	2
12:10	TX_PWRBK_SET	RO	TX power backoff setting: 12 11 10 1 1 1 = 14 dB 1 1 0 = 12 dB 1 0 1 = 10 dB 1 0 0 = 8 dB 0 1 1 = 6 dB 0 1 0 = 4 dB 0 0 1 = 2 dB 0 0 0 = 0 dB Reset value is 2.	2
9:1	Reserved	RO	Ignore on read.	Undetermined
0	SHORT_RCH_MODE	R/W	Limited reach mode 1 = PHY is operating in limited reach mode. 0 = PHY is not operating in limited reach mode.	0

2.4.1.19 10GBASE-T Test Mode (DEVAD = 1, Address = 0x0084)

Table 32: 10GBASE-T Test Mode (1.0x0084)

Bit	Name	R/W	Description	Default
15:13	TST_MODE_CTL	R/W	Test mode control (when combined with bits 9:8 below) 15 14 13 9 8 0 0 0 0 1 = Test mode 9 0 0 0 1 0 = Test mode 8 1 1 1 0 0 = Test mode 7 1 1 0 0 0 = Test mode 6 1 0 1 0 0 = Test mode 5 1 0 0 0 0 = Test mode 4 0 1 1 0 0 = Test mode 3 0 1 0 0 0 = Test mode 2 0 0 1 0 0 = Test mode 1 0 0 0 0 0 = Normal operation	x0
12:10	TRN_TEST_FREQ	R/W	Transmitter test frequencies 12 11 10 1 1 1 = Reserved 1 1 0 = Dual tone 5 1 0 1 = Dual tone 4 1 0 0 = Dual tone 3 0 1 1 = Reserved 0 1 0 = Dual tone 2 0 0 1 = Dual tone 1 0 0 0 = Reserved	0
9:8	EEE_TST_MODE_CTL	R/W	Combined with bits 15:12, see description.	00
7:0	Reserved	R/W	Use read-modify-write to not change the current value during write. Ignore on read.	Undetermined

2.4.1.20 10GBASE-T SNR Operating Margin CH A (DEVAD = 1, Address = 0x0085)

Table 33: 10GBASE-T SNR Operating Margin CH A (1.0x0085)

Bit	Name	R/W	Description	Default
15:0	SNR_A	RO	This register contains the current SNR operating margin measured at the slicer input for channel A for the 10G/BASE-T PMA. It is reported with 0.1 dB of resolution to an accuracy of 0.5 dB within the range of –12.7 dB to 12.7 dB. The number is in offset two's complement notation, with 0.0 dB represented by 0x8000.	0x8000

2.4.1.21 10GBASE-T SNR Operating Margin CH B (DEVAD = 1, Address = 0x0086)

Table 34: 10GBASE-T SNR Operating Margin CH B (1.0x0086)

Bit	Name	R/W	Description	Default
15:0	SNR_B	RO	This register contains the current SNR operating margin measured at the slicer input for channel B for the 10G/BASE-T PMA. It is reported with 0.1 dB of resolution to an accuracy of 0.5 dB within the range of –12.7 dB to 12.7 dB. The number is in offset two's complement notation, with 0.0 dB represented by 0x8000.	0x8000

2.4.1.22 10GBASE-T SNR Operating Margin CH C (DEVAD = 1, Address = 0x0087)

Table 35: 10GBASE-T SNR Operating Margin CH C (1.0x0087)

Bit	Name	R/W	Description	Default
15:0	SNR_C	RO	This register contains the current SNR operating margin measured at the slicer input for channel C for the 10G/BASE-T PMA. It is reported with 0.1 dB of resolution to an accuracy of 0.5 dB within the range of –12.7 dB to 12.7 dB. The number is in offset two's complement notation, with 0.0 dB represented by 0x8000.	0x8000

2.4.1.23 10GBASE-T SNR Operating Margin CH D (DEVAD = 1, Address = 0x0088)

Table 36: 10GBASE-T SNR Operating Margin CH D (1.0x0088)

Bit	Name	R/W	Description	Default
15:0	SNR_D	RO	This register contains the current SNR operating margin measured at the slicer input for channel D for the 10G/BASE-T PMA. It is reported with 0.1 dB of resolution to an accuracy of 0.5 dB within the range of –12.7 dB to 12.7 dB. The number is in offset two's complement notation, with 0.0 dB represented by 0x8000.	0x8000

2.4.1.24 10GBASE-T SNR Minimum Margin CH A (DEVAD = 1, Address = 0x0089)

Table 37: 10GBASE-T SNR Minimum Margin CH A (1.0x0089)

Bit	Name	R/W	Description	Default
15:0	MIN_MARGIN_A	RO	The minimum margin channel A register contains a latched copy of the lowest value observed in the SNR operating margin channel A register (1.133) since the last read. It is reported in units of 0.1 dB to an accuracy of 0.5 dB within the range of –12.7 dB to 12.7 dB. The number is in offset two's complement notation, with 0.0 dB represented by 0x8000.	0x8000

2.4.1.25 10GBASE-T SNR Minimum Margin CH B (DEVAD = 1, Address = 0x008A)

Table 38: 10GBASE-T SNR Minimum Margin CH B (1.0x008A)

Bit	Name	R/W	Description	Default
15:0	MIN_MARGIN_B	RO	The minimum margin channel B register contains a latched copy of the lowest value observed in the SNR operating margin channel A register (1.133) since the last read. It is reported in units of 0.1 dB to an accuracy of 0.5 dB within the range of –12.7 dB to 12.7 dB. The number is in offset two's complement notation, with 0.0 dB represented by 0x8000.	0x8000

2.4.1.26 10GBASE-T SNR Minimum Margin CH C (DEVAD = 1, Address = 0x008B)

Table 39: 10GBASE-T SNR Minimum Margin CH C (1.0x008B)

Bit	Name	R/W	Description	Default
15:0	MIN_MARGIN_C	RO	The minimum margin channel C register contains a latched copy of the lowest value observed in the SNR operating margin channel A register (1.133) since the last read. It is reported in units of 0.1 dB to an accuracy of 0.5 dB within the range of –12.7 dB to 12.7 dB. The number is in offset two's complement notation, with 0.0 dB represented by 0x8000.	0x8000

2.4.1.27 10GBASE-T SNR Minimum Margin CH D (DEVAD = 1, Address = 0x008C)

Table 40: 10GBASE-T SNR Minimum Margin CH D (1.0x008C)

Bit	Name	R/W	Description	Default
15:0	MIN_MARGIN_D	RO	The minimum margin channel D register contains a latched copy of the lowest value observed in the SNR operating margin channel A register (1.133) since the last read. It is reported in units of 0.1 dB to an accuracy of 0.5 dB within the range of –12.7 dB to 12.7 dB. The number is in offset two's complement notation, with 0.0 dB represented by 0x8000.	0x8000

2.4.1.28 10GBASE-T RX Signal Power CH A (DEVAD = 1, Address = 0x008D)

Table 41: 10GBASE-T RX Signal Power CH A (1.0x008D)

Bit	Name	R/W	Description	Default
15:0	RX_SIG_POWER_A	RO	The RX signal power channel A register is read only and contains the receive signal power measured at the MDI during training as described in 55.4.3.1. It is reported in units of 0.1 dB to an accuracy of 0.5 dB within the range of –20 dBm to 5.5 dBm. The number is in offset two's complement notation, with 0.0 dB represented by 0x8000.	0x8000

2.4.1.29 10GBASE-T RX Signal Power CH B (DEVAD = 1, Address = 0x008E)

Table 42: 10GBASE-T RX Signal Power CH A (1.0x008E)

Bit	Name	R/W	Description	Default
15:0	RX_SIG_POWER_B	RO	The RX signal power channel B register is read only and contains the receive signal power measured at the MDI during training as described in 55.4.3.1. It is reported in units of 0.1 dB to an accuracy of 0.5 dB within the range of –20 dBm to 5.5 dBm. The number is in offset two's complement notation, with 0.0 dB represented by 0x8000.	0x8000

2.4.1.30 10GBASE-T RX Signal Power CH C (DEVAD = 1, Address = 0x008F)

Table 43: 10GBASE-T RX Signal Power CH C (1.0x008F)

Bit	Name	R/W	Description	Default
15:0	RX_SIG_POWER_C	RO	The RX signal power channel C register is read only and contains the receive signal power measured at the MDI during training as described in 55.4.3.1. It is reported in units of 0.1 dB to an accuracy of 0.5 dB within the range of –20 dBm to 5.5 dBm. The number is in offset two's complement notation, with 0.0 dB represented by 0x8000.	0x8000

2.4.1.31 10GBASE-T RX Signal Power CH D (DEVAD = 1, Address = 0x0090)

Table 44: 10GBASE-T RX Signal Power CH D (1.0x0090)

Bit	Name	R/W	Description	Default
15:0	RX_SIG_POWER_D	RO	The RX signal power channel D register is read only and contains the receive signal power measured at the MDI during training as described in 55.4.3.1. It is reported in units of 0.1 dB to an accuracy of 0.5 dB within the range of –20 dBm to 5.5 dBm. The number is in offset two's complement notation, with 0.0 dB represented by 0x8000.	0x8000

2.4.1.32 10GBASE-T Skew Delay Part 0 (DEVAD = 1, Address = 0x0091)

Table 45: 10GBASE-T Skew Delay Part 0 (1.0x0091)

Bit	Name	R/W	Description	Default
15	Reserved	RO	Ignore on read.	Undetermined
14:8	SKW_DLY_B	RO	It reports the current skew delay on pair B with respect to physical pair A. It is reported with 1.25 ns resolution to an accuracy of 2.5 ns. The number reported is in two's complement notation with positive values representing delay and negative values representing advance with respect to physical pair A. If the delay exceed the maximum amount that can be represented by the range (–80 ns to +78.75 ns), the field displays the maximum respective value. The value is updated at least once per second.	0
7:0	Reserved	RO	Ignore on read.	Undetermined

2.4.1.33 10GBASE-T Skew Delay Part 1 (DEVAD = 1, Address = 0x0092)

Table 46: 10GBASE-T Skew Delay Part 1 (1.0x0092)

Bit	Name	R/W	Description	Default
15	Reserved	RO	Ignore on read.	Undetermined
14:8	SKW_DLY_D	RO	It reports the current skew delay on pair D with respect to physical pair A. It is reported with 1.25 ns resolution to an accuracy of 2.5 ns. The number reported is in two's complement notation with positive values representing delay and negative values representing advance with respect to physical pair A. If the delay exceed the maximum amount that can be represented by the range (–80 ns to +78.75 ns), the field displays the maximum respective value. The value is updated at least once per second.	0
7	Reserved	RO	Ignore on read.	Undetermined
6:0	SKW_DLY_C	RO	It reports the current skew delay on pair C with respect to physical pair A. It is reported with 1.25 ns resolution to an accuracy of 2.5 ns. The number reported is in two's complement notation with positive values representing delay and negative values representing advance with respect to physical pair A. If the delay exceed the maximum amount that can be represented by the range (–80 ns to +78.75 ns), the field displays the maximum respective value. The value is updated at least once per second.	0

2.4.1.34 IEEE Fast Retrain Register (DEVAD = 1, Address = 0x0093)

Table 47: IEEE Fast Retrain Register (1.0x0093)

Bit	Name	R/W	Description	Default
15:11	FR_RX_CNT	RO	Fast Retrain RX Count Counts the number of fast retrains requested by the link partner. Saturates at 31. Reset to 0 when read.	0x0
10:6	FR_TX_CNT	RO	Fast Retrain TX Count Counts the number of fast retrains requested by the local device. Saturates at 31. Reset to 0 when read.	0x0
5	Reserved	RO	Ignore on read.	Undetermined
4	FR_ABILITY	RO	Fast Retrain Ability 1 = Fast retrain capability is supported. 0 = Fast retrain capability is not supported.	0
3	FR_NEGOTIATED	RO	Fast Retrain Negotiated. 1 = Fast retrain capability was negotiated. 0 = Fast retrain capability was not negotiated.	0
2:1	FR_SIGTYPE	R/W	Fast Retrain Signal Type Selects signal that is sent by the PCS RX to the MAC during Fast Retrain 11 = Reserved 10 = PHY signals Link Interruption during fast retrain 01 = PHY signals Local Fault during fast retrain 00 = PHY signals IDLE during fast retrain	00
0	FR_EN	R/W	Fast Retrain Enable 1 = Fast Retrain capability is enabled. 0 = Fast Retrain capability is disabled.	Set by firmware

2.4.1.35 Download Processor Control (DEVAD = 1, Address = 0xA817)

Table 48: Download Processor Control (DEVAD = 1, Address = 0xA817)

Bit	Name	R/W	Description	Default
15:0	DOWNLOAD PROCESSOR CONTROL	R/W	Download processor control register	0

2.4.1.36 Download Status (DEVAD = 1, Address = 0xA818)

Table 49: Download Status (DEVAD = 1, Address = 0xA818)

Bit	Name	R/W	Description	Default
15:0	DOWNLOAD STATUS	R/W	Download Status. When bit 0 is 1, the operation is complete. When bit 0 is 0, wait for the operation to complete.	0

2.4.1.37 Download Address Low (DEVAD = 1, Address = 0xA819)

Table 50: Download Address Low (DEVAD = 1, Address = 0xA819)

Bit	Name	R/W	Description	Default
15:0	DOWNLOAD ADDRESS LOW CONTROL	R/W	Download address low control register	0

2.4.1.38 Download Address High (DEVAD = 1, Address = 0xA81A)

Table 51: Download Address High (DEVAD = 1, Address = 0xA81A)

Bit	Name	R/W	Description	Default
15:0	DOWNLOAD ADDRESS HIGH CONTROL	R/W	Download address high control register	0

2.4.1.39 Download Data Low (DEVAD = 1, Address = 0xA81B)

Table 52: Download Data Low (DEVAD = 1, Address = 0xA81B)

Bit	Name	R/W	Description	Default
15:0	DOWNLOAD DATA HIGH CONTROL	R/W	Download data low control register	0

2.4.1.40 Download Data High (DEVAD = 1, Address = 0xA81C)

Table 53: Download Data High (DEVAD = 1, Address = 0xA81C)

Bit	Name	R/W	Description	Default
15:0	DOWNLOAD DATA HIGH CONTROL	R/W	Download data high control register	0

2.4.1.41 CTL LED1 MASK LOW (DEVAD = 1, Address = 0xA82C)

Table 54: CTL LED1 MASK LOW (1.0xA82C)

Bit	Name	R/W	Description	Default
15	LED_MASK15	R/W	1 = Enable the LED source 15	0
14	LED_MASK14	R/W	1 = Enable the LED source 14	0
13	LED_MASK13	R/W	1 = Enable the LED source 13	0

Table 54: CTL LED1 MASK LOW (1.0xA82C) (Continued)

Bit	Name	R/W	Description	Default
12	LED_MASK12	R/W	1 = Enable the LED source 12	0
11	LED_MASK11	R/W	1 = Enable the LED source 11	0
10	LED_MASK10	R/W	1 = Enable the LED source 10	0
9	LED_MASK9	R/W	1 = Enable the LED source 9	0
8	LED_MASK8	R/W	1 = Enable the LED source 8	0
7	LED_MASK7	R/W	1 = Enable the LED source 7	0
6	LED_MASK6	R/W	1 = Enable the LED source 6	0
5	LED_MASK5	R/W	1 = Enable the LED source 5	0
4	LED_MASK4	R/W	1 = Enable the LED source 4	0
3	LED_MASK3	R/W	1 = Enable the LED source 3	0
2	LED_MASK2	R/W	1 = Enable the LED source 2	0
1	LED_MASK1	R/W	1 = Enable the LED source 1	0
0	LED_MASK0	R/W	1 = Enable the LED source 0	0

2.4.1.42 CTL LED1 MASK EXT (DEVAD = 1, Address = 0xA8EF)

Table 55: CTL LED1 MASK EXT (1.0xA8EF)

Bit	Name	R/W	Description	Default
47	LED_MASK47	R/W	1 = Enable the LED source ext. 47	0
46	LED_MASK46	R/W	1 = Enable the LED source ext. 46	0
45	LED_MASK45	R/W	1 = Enable the LED source ext. 45	0
44	LED_MASK44	R/W	1 = Enable the LED source ext. 44	0
43	LED_MASK43	R/W	1 = Enable the LED source ext. 43	0
42	LED_MASK42	R/W	1 = Enable the LED source ext. 42	0
41	LED_MASK41	R/W	1 = Enable the LED source ext. 41	0
40	LED_MASK40	R/W	1 = Enable the LED source ext. 40	0
39	LED_MASK39	R/W	1 = Enable the LED source ext. 39	0
38	LED_MASK38	R/W	1 = Enable the LED source ext. 38	0
37	LED_MASK37	R/W	1 = Enable the LED source ext. 37	0
36	LED_MASK36	R/W	1 = Enable the LED source ext. 36	0
35	LED_MASK35	R/W	1 = Enable the LED source ext. 35	0
34	LED_MASK34	R/W	1 = Enable the LED source ext. 34	0
33	LED_MASK33	R/W	1 = Enable the LED source ext. 33	0
32	LED_MASK32	R/W	1 = Enable the LED source ext. 32	0

2.4.1.43 CTL LED1 BLINK (DEVAD = 1, Address = 0xA82E)

Table 56: CTL LED0 BLINK (1.0xA82E)

Bit	Name	R/W	Description	Default
15:4	Reserved	R/W	Use read-modify-write to not change the current value during write. Ignore on read.	Undetermined
3:0	LED_BLINK_CYCLE_CNT	R/W	LED blink cycle count of the number of slow clock cycles. Defines for how many slow clock cycles the LED is ON/OFF.	0x4h

2.4.1.44 CTL LED2 MASK LOW (DEVAD = 1, Address = 0xA82F)

Table 57: CTL LED2 MASK LOW (1.0xA82F)

Bit	Name	R/W	Description	Default
15	LED_MASK15	R/W	1 = Enable the LED source 15	0
14	LED_MASK14	R/W	1 = Enable the LED source 14	0
13	LED_MASK13	R/W	1 = Enable the LED source 13	0
12	LED_MASK12	R/W	1 = Enable the LED source 12	0
11	LED_MASK11	R/W	1 = Enable the LED source 11	0
10	LED_MASK10	R/W	1 = Enable the LED source 10	0
9	LED_MASK9	R/W	1 = Enable the LED source 9	0
8	LED_MASK8	R/W	1 = Enable the LED source 8	0
7	LED_MASK7	R/W	1 = Enable the LED source 7	0
6	LED_MASK6	R/W	1 = Enable the LED source 6	0
5	LED_MASK5	R/W	1 = Enable the LED source 5	0
4	LED_MASK4	R/W	1 = Enable the LED source 4	0
3	LED_MASK3	R/W	1 = Enable the LED source 3	0
2	LED_MASK2	R/W	1 = Enable the LED source 2	0
1	LED_MASK1	R/W	1 = Enable the LED source 1	0
0	LED_MASK0	R/W	1 = Enable the LED source 0	0

2.4.1.45 CTL LED2 MASK EXT (DEVAD = 1, Address = 0xA8F0)

Table 58: CTL LED2 MASK EXT (1.0xA8F0)

Bit	Name	R/W	Description	Default
47	LED_MASK47	R/W	1 = Enable the LED source ext. 47	0
46	LED_MASK46	R/W	1 = Enable the LED source ext. 46	0
45	LED_MASK45	R/W	1 = Enable the LED source ext. 45	0
44	LED_MASK44	R/W	1 = Enable the LED source ext. 44	0
43	LED_MASK43	R/W	1 = Enable the LED source ext. 43	0
42	LED_MASK42	R/W	1 = Enable the LED source ext. 42	0
41	LED_MASK41	R/W	1 = Enable the LED source ext. 41	0
40	LED_MASK40	R/W	1 = Enable the LED source ext. 40	0
39	LED_MASK39	R/W	1 = Enable the LED source ext. 39	0
38	LED_MASK38	R/W	1 = Enable the LED source ext. 38	0
37	LED_MASK37	R/W	1 = Enable the LED source ext. 37	0
36	LED_MASK36	R/W	1 = Enable the LED source ext. 36	0
35	LED_MASK35	R/W	1 = Enable the LED source ext. 35	0
34	LED_MASK34	R/W	1 = Enable the LED source ext. 34	0
33	LED_MASK33	R/W	1 = Enable the LED source ext. 33	0
32	LED_MASK32	R/W	1 = Enable the LED source ext. 32	0

2.4.1.46 CTL LED2 BLINK (DEVAD = 1, Address = 0xA831)

Table 59: CTL LED0 BLINK (1.0xA831)

Bit	Name	R/W	Description	Default
15:4	Reserved	R/W	Use read-modify-write to not change the current value during write. Ignore on read.	Undetermined
3:0	LED_BLINK_CYCLE_CNT	R/W	LED blink cycle count of the number of slow clock cycles. Defines for how many slow clock cycles the LED is ON/OFF.	0x4h

2.4.1.47 CTL LED3 MASK LOW (DEVAD = 1, Address = 0xA832)

Table 60: CTL LED3 MASK LOW (1.0xA832)

Bit	Name	R/W	Description	Default
15	LED_MASK15	R/W	1 = Enable the LED source 15	0
14	LED_MASK14	R/W	1 = Enable the LED source 14	0
13	LED_MASK13	R/W	1 = Enable the LED source 13	0
12	LED_MASK12	R/W	1 = Enable the LED source 12	0
11	LED_MASK11	R/W	1 = Enable the LED source 11	0
10	LED_MASK10	R/W	1 = Enable the LED source 10	0
9	LED_MASK9	R/W	1 = Enable the LED source 9	0
8	LED_MASK8	R/W	1 = Enable the LED source 8	0
7	LED_MASK7	R/W	1 = Enable the LED source 7	0
6	LED_MASK6	R/W	1 = Enable the LED source 6	0
5	LED_MASK5	R/W	1 = Enable the LED source 5	0
4	LED_MASK4	R/W	1 = Enable the LED source 4	0
3	LED_MASK3	R/W	1 = Enable the LED source 3	0
2	LED_MASK2	R/W	1 = Enable the LED source 2	0
1	LED_MASK1	R/W	1 = Enable the LED source 1	0
0	LED_MASK0	R/W	1 = Enable the LED source 0	0

2.4.1.48 CTL LED3 MASK EXT (DEVAD = 1, Address = 0xA8F1)

Table 61: CTL LED3 MASK EXT (1.0xA8F1)

Bit	Name	R/W	Description	Default
47	LED_MASK47	R/W	1 = Enable the LED source ext. 47	0
46	LED_MASK46	R/W	1 = Enable the LED source ext. 46	0
45	LED_MASK45	R/W	1 = Enable the LED source ext. 45	0
44	LED_MASK44	R/W	1 = Enable the LED source ext. 44	0
43	LED_MASK43	R/W	1 = Enable the LED source ext. 43	0
42	LED_MASK42	R/W	1 = Enable the LED source ext. 42	0
41	LED_MASK41	R/W	1 = Enable the LED source ext. 41	0
40	LED_MASK40	R/W	1 = Enable the LED source ext. 40	0
39	LED_MASK39	R/W	1 = Enable the LED source ext. 39	0
38	LED_MASK38	R/W	1 = Enable the LED source ext. 38	0
37	LED_MASK37	R/W	1 = Enable the LED source ext. 37	0

Table 61: CTL LED3 MASK EXT (1.0xA8F1) (Continued)

Bit	Name	R/W	Description	Default
36	LED_MASK36	R/W	1 = Enable the LED source ext. 36	0
35	LED_MASK35	R/W	1 = Enable the LED source ext. 35	0
34	LED_MASK34	R/W	1 = Enable the LED source ext. 34	0
33	LED_MASK33	R/W	1 = Enable the LED source ext. 33	0
32	LED_MASK32	R/W	1 = Enable the LED source ext. 32	0

2.4.1.49 CTL LED3 BLINK (DEVAD = 1, Address = 0xA834)

Table 62: CTL LED3 BLINK (1.0xA834)

Bit	Name	R/W	Description	Default
15:4	Reserved	R/W	Use read-modify-write to not change the current value during write. Ignore on read.	Undetermined
3:0	LED_BLINK_CYCLE_CNT	R/W	LED blink cycle count of the number of slow clock cycles. Defines for how many slow clock cycles the LED is ON/OFF.	0x4h

2.4.1.50 CTL LED4 MASK LOW (DEVAD = 1, Address = 0xA835)

Table 63: CTL LED4 MASK LOW (1.0xA835)

Bit	Name	R/W	Description	Default
15	LED_MASK15	R/W	1 = Enable the LED source 15	0
14	LED_MASK14	R/W	1 = Enable the LED source 14	0
13	LED_MASK13	R/W	1 = Enable the LED source 13	0
12	LED_MASK12	R/W	1 = Enable the LED source 12	0
11	LED_MASK11	R/W	1 = Enable the LED source 11	0
10	LED_MASK10	R/W	1 = Enable the LED source 10	0
9	LED_MASK9	R/W	1 = Enable the LED source 9	0
8	LED_MASK8	R/W	1 = Enable the LED source 8	0
7	LED_MASK7	R/W	1 = Enable the LED source 7	0
6	LED_MASK6	R/W	1 = Enable the LED source 6	0
5	LED_MASK5	R/W	1 = Enable the LED source 5	0
4	LED_MASK4	R/W	1 = Enable the LED source 4	0
3	LED_MASK3	R/W	1 = Enable the LED source 3	0
2	LED_MASK2	R/W	1 = Enable the LED source 2	0
1	LED_MASK1	R/W	1 = Enable the LED source 1	0
0	LED_MASK0	R/W	1 = Enable the LED source 0	0

2.4.1.51 CTL LED4 MASK EXT (DEVAD = 1, Address = 0xA8F2)

Table 64: CTL LED4 MASK EXT (1.0xA8F2)

Bit	Name	R/W	Description	Default
47	LED_MASK47	R/W	1 = Enable the LED source ext. 47	0
46	LED_MASK46	R/W	1 = Enable the LED source ext. 46	0
45	LED_MASK45	R/W	1 = Enable the LED source ext. 45	0
44	LED_MASK44	R/W	1 = Enable the LED source ext. 44	0
43	LED_MASK43	R/W	1 = Enable the LED source ext. 43	0
42	LED_MASK42	R/W	1 = Enable the LED source ext. 42	0
41	LED_MASK41	R/W	1 = Enable the LED source ext. 41	0
40	LED_MASK40	R/W	1 = Enable the LED source ext. 40	0
39	LED_MASK39	R/W	1 = Enable the LED source ext. 39	0
38	LED_MASK38	R/W	1 = Enable the LED source ext. 38	0
37	LED_MASK37	R/W	1 = Enable the LED source ext. 37	0
36	LED_MASK36	R/W	1 = Enable the LED source ext. 36	0
35	LED_MASK35	R/W	1 = Enable the LED source ext. 35	0
34	LED_MASK34	R/W	1 = Enable the LED source ext. 34	0
33	LED_MASK33	R/W	1 = Enable the LED source ext. 33	0
32	LED_MASK32	R/W	1 = Enable the LED source ext. 32	0

2.4.1.52 CTL LED4 BLINK (DEVAD = 1, Address = 0xA837)

Table 65: CTL LED4 BLINK (1.0xA837)

Bit	Name	R/W	Description	Default
15:4	Reserved	R/W	Use read-modify-write to not change the current value during write. Ignore on read.	Undetermined
3:0	LED_BLINK_CYCLE_ CNT	R/W	LED blink cycle count of the number of slow clock cycles. Defines for how many slow clock cycles the LED is ON/OFF.	0x4h

2.4.1.53 CTL LED5 MASK LOW (DEVAD = 1, Address = 0xA838)

Table 66: CTL LED5 MASK LOW (1.0xA838)

Bit	Name	R/W	Description	Default
15	LED_MASK15	R/W	1 = Enable the LED source 15	0
14	LED_MASK14	R/W	1 = Enable the LED source 14	0
13	LED_MASK13	R/W	1 = Enable the LED source 13	0
12	LED_MASK12	R/W	1 = Enable the LED source 12	0
11	LED_MASK11	R/W	1 = Enable the LED source 11	0
10	LED_MASK10	R/W	1 = Enable the LED source 10	0
9	LED_MASK9	R/W	1 = Enable the LED source 9	0
8	LED_MASK8	R/W	1 = Enable the LED source 8	0
7	LED_MASK7	R/W	1 = Enable the LED source 7	0
6	LED_MASK6	R/W	1 = Enable the LED source 6	0
5	LED_MASK5	R/W	1 = Enable the LED source 5	0

Table 66: CTL LED5 MASK LOW (1.0xA838) (Continued)

Bit	Name	R/W	Description	Default
4	LED_MASK4	R/W	1 = Enable the LED source 4	0
3	LED_MASK3	R/W	1 = Enable the LED source 3	0
2	LED_MASK2	R/W	1 = Enable the LED source 2	0
1	LED_MASK1	R/W	1 = Enable the LED source 1	0
0	LED_MASK0	R/W	1 = Enable the LED source 0	0

2.4.1.54 CTRL LED5 MASK EXT (DEVAD = 1, Address = 0xA8F3)

Table 67: CTRL LED5 MASK EXT (1.0xA8F3)

Bit	Name	R/W	Description	Default
47	LED_MASK47	R/W	1 = Enable the LED source ext. 47	0
46	LED_MASK46	R/W	1 = Enable the LED source ext. 46	0
45	LED_MASK45	R/W	1 = Enable the LED source ext. 45	0
44	LED_MASK44	R/W	1 = Enable the LED source ext. 44	0
43	LED_MASK43	R/W	1 = Enable the LED source ext. 43	0
42	LED_MASK42	R/W	1 = Enable the LED source ext. 42	0
41	LED_MASK41	R/W	1 = Enable the LED source ext. 41	0
40	LED_MASK40	R/W	1 = Enable the LED source ext. 40	0
39	LED_MASK39	R/W	1 = Enable the LED source ext. 39	0
38	LED_MASK38	R/W	1 = Enable the LED source ext. 38	0
37	LED_MASK37	R/W	1 = Enable the LED source ext. 37	0
36	LED_MASK36	R/W	1 = Enable the LED source ext. 36	0
35	LED_MASK35	R/W	1 = Enable the LED source ext. 35	0
34	LED_MASK34	R/W	1 = Enable the LED source ext. 34	0
33	LED_MASK33	R/W	1 = Enable the LED source ext. 33	0
32	LED_MASK32	R/W	1 = Enable the LED source ext. 32	0

2.4.1.55 CTL LED5 BLINK (DEVAD = 1, Address = 0xA83A)

Table 68: CTL LED5 BLINK (1.0xA83A)

Bit	Name	R/W	Description	Default
15:4	Reserved	R/W	Use read-modify-write to not change the current value during write. Ignore on read.	Undetermined
3:0	LED_BLINK_CYCLE_CNT	R/W	LED blink cycle count of the number of slow clock cycles. Defines for how many slow clock cycles the LED is ON/OFF.	0x4h

2.4.1.56 PHYC_CTL_SLOW_CLK_CNT_HIGH (DEVAD = 1, Address = 0xA82B)

Table 69: PHYC_CTL_SLOW_CLK_CNT_HIGH (DEVAD = 1, Address = 0xA82B)

Bit	Name	R/W	Description	Default
15:8	Reserved	R/W	Reserved bits write has no effect and read always returns 0.	Undetermined
7:0	SLOW_CLK_CNT_HIGH	R/W	The high 8 bits of the number of 10 ns cycles to generate a slow clock for LED. The period of the slow clock is (2^{SLOW_CLK_CNT_HIGH, SLOW_CLK_CNT_LOW} + 1) × 10 ns.	0xFF

2.4.1.57 PHYC_CTL_SLOW_CLK_CNT_LOW (DEVAD = 1, Address = 0xA82A)

Table 70: PHYC_CTL_SLOW_CLK_CNT_LOW (DEVAD = 1, Address = 0xA82A)

Bit	Name	R/W	Description	Default
15:0	SLOW_CLK_CNT_LOW	R/W	The lower 16 bits of the number of 10 ns cycles to generate a slow clock for LED.	0xFFFF

2.4.1.58 LED Control (DEVAD = 1, Address = 0xA83B)

Table 71: LED Control (1.0xA83B)

Bit	Name	R/W	Description	Default
15	Reserved	R/W	Use read-modify-write to not change the current value during write. Ignore on read.	Undetermined
14	LED5_OE_N	R/W	1 = Disable LED5 output. 0 = Enable LED5 output.	1
13:12	LED5_CTL	R/W	Control LED function. 00 = LED off. 01 = LED blink based on the source. 10 = LED ON based on the source. 11 = Open-drain.	0
11	LED4_OE_N	R/W	1 = Disable LED4 output. 0 = Enable LED4 output.	1
10:9	LED4_CTL	R/W	Control LED function. 00 = LED off. 01 = LED blink based on the source. 10 = LED ON based on the source. 11 = Open-drain.	0
8	LED3_OE_N	R/W	1 = Disable LED3 output. 0 = Enable LED3 output.	1
7:6	LED3_CTL	R/W	Control LED function. 00 = LED off. 01 = LED blink based on the source. 10 = LED ON based on the source. 11 = Open-drain.	0
5	LED2_OE_N	R/W	1 = Disable LED2 output. 0 = Enable LED2 output.	1

Table 71: LED Control (1.0xA83B) (Continued)

Bit	Name	R/W	Description	Default
4:3	LED2_CTL	R/W	Control LED function. 00 = LED off. 01 = LED blink based on the source. 10 = LED ON based on the source. 11 = Open-drain.	0
2	LED1_OE_N	R/W	1 = Disable LED1 output. 0 = Enable LED1 output.	1
1:0	LED1_CTL	R/W	Control LED function. 00 = LED off. 01 = LED blink based on the source. 10 = LED ON based on the source. 11 = Open-drain.	0

2.4.1.59 LED Control Source (DEVAD = 1, Address = 0xA83C)

Table 72: LED Control Source (1.0xA83C)

Bit	Name	R/W	Description	Default
15	Reserved	RO	Ignore on read.	Undetermined
14	Reserved	RO	Ignore on read.	Undetermined
13	Reserved	RO	Ignore on read.	Undetermined
12	Reserved	RO	Ignore on read.	Undetermined
11	Reserved	RO	Ignore on read.	Undetermined
10	Reserved	RO	Ignore on read.	Undetermined
9	Reserved	RO	Ignore on read.	Undetermined
8	Reserved	RO	Ignore on read.	Undetermined
7	LINK_10G_XGPHY	RO	1 = 10G copper link is up. 0 = 10G copper link is down.	0
6	Reserved	RO	Ignore on read.	Undetermined
5	LED_ON	RO	Set to 1.	0
4:3	Link Status[1:0]	RO	11 = Linked at 1G. 10 = Linked at 100M. 01 = Reserved. 00 = Reserved.	0
2	TX ACTIVITY	RO	TX activity is on.	0
1	RX ACTIVITY	RO	RX activity is on.	0
0	Reserved	RO	Ignore on read.	Undetermined

2.4.1.60 LED Control Source High (DEVAD = 1, Address = 0xA83D) 15867339858

Table 73: LED Control Source High (1.0xA83D)

Bit	Name	R/W	Description	Default
15	Reserved	RO	Ignore on read.	Undetermined
14	Reserved	RO	Ignore on read.	Undetermined
13	Reserved	RO	Ignore on read.	Undetermined
12	Reserved	RO	Ignore on read.	Undetermined
11	Reserved	RO	Ignore on read.	Undetermined
10	Reserved	RO	Ignore on read.	Undetermined
9	Reserved	RO	Ignore on read.	Undetermined
8	Reserved	RO	Ignore on read.	Undetermined
7	Reserved	RO	Ignore on read.	Undetermined
6	Reserved	RO	Ignore on read.	Undetermined
5	Reserved	RO	Ignore on read.	Undetermined
4	Reserved	RO	Ignore on read.	Undetermined
3	5G link	RO	1 = 5G link up. 0 = 5G link down.	0
2	2.5G link	RO	1 = 2.5G link up. 0 = 2.5G link down.	0
1	Reserved	RO	Ignore on read.	Undetermined
0	Reserved	RO	Ignore on read.	Undetermined

2.4.1.61 LED Control 1 (DEVAD = 1, Address = 0xA8EC)

NOTE:

- Be sure to use read-modify-write when setting stretch LED bit registers.
- Use bit registers 5 to 9 to make the LED activity status visible.

Table 74: LED Control 1 (1.0xA8EC)

Bit Field	Field Name	R/W	Description	Default
15	ALLOW GPHY ACTIVITY	R/W	0 = Blocks the GPHY RX and TX activity signals from the LED's. 1 = Allows the GPHY RX and TX activity signals to be inputs to the LED's. This bit gates the GPHY hardware activity signal to source register (1.0xA83C) bits 1 and 2.	0
14:10	Reserved	R/W	Use read-modify-write to not change the current value during write. Ignore on read.	Undetermined
9	LED5_STRETCH_EN	R/W	0 = No stretch. 1 = Stretch the source signal based on blink cycle.	0
8	LED4_STRETCH_EN	R/W	0 = No stretch. 1 = Stretch the source signal based on blink cycle.	0
7	LED3_STRETCH_EN	R/W	0 = No stretch. 1 = Stretch the source signal based on blink cycle.	0
6	LED2_STRETCH_EN	R/W	0 = No stretch. 1 = Stretch the source signal based on blink cycle.	0

Table 74: LED Control 1 (1.0xA8EC) (Continued)

Bit Field	Field Name	R/W	Description	Default
5	LED1_STRETCH_EN	R/W	0 = No stretch. 1 = Stretch the source signal based on blink cycle.	0
4:0	Reserved	R/W	Use read-modify-write to not change the current value during write. Ignore on read.	Undetermined

2.4.1.62 10GBASE-T Tone Frequency (DEVAD = 1, Address = 0xA89E)

Table 75: 10GBASE-T Tone Frequency (1.0xA89E)

Bit	Name	R/W	Description	Default
15:0	TONE_FREQUENCY	RO	This frequency, expressed in MHz, is the main/strongest frequency of the interference signal that produced the last retrain.	0

2.4.1.63 10GBASE-T Number of Retrain (DEVAD = 1, Address = 0xA89F)

Table 76: 10GBASE-T Number of Retrain (1.0xA89F)

Bit	Name	R/W	Description	Default
15:0	NUMBER_OF_RETRAIN	RO	The number of retrains after reset. Subsequent auto-negotiation exchanges do not alter this counter.	0

2.4.1.64 10GBASE-T Number of Linkdown (DEVAD = 1, Address = 0xA8A0)

Table 77: 10GBASE-T Number of Link Down (1.0xA8A0)

Bit	Name	R/W	Description	Default
15:0	NUMBER_LINK_DOWN	RO	The number of linkdown episodes that occurred after reset. Subsequent auto-negotiation exchanges do not alter this counter.	0

2.4.1.65 10GBASE-T Number of Successful EMI Retrain (DEVAD = 1, Address = 0xA8A9)

Table 78: 10GBASE-T Number of Successful EMI Retrain (1.0xA8A9)

Bit	Name	R/W	Description	Default
15:0	Number Success Retrain	RO	The number of successful Fast Retrain occurrences.	0

2.4.1.66 MDI Differential Level on Pair A (DEVAD = 1, Address = 0xA8AA)

Table 79: MDI Differential Level on Pair A (1.00xA8AA)

Bit	Name	R/W	Description	Default
15:0	MDI	RO	Estimated level of narrowband differential 0x0 interference reported in µV as measured at the MDI interface for Pair A during the last retrain event.	0

2.4.1.67 MDI Differential Level on Pair B (DEVAD = 1, Address = 0xA8AB)

Table 80: MDI Differential Level on Pair B (1.0xA8AB)

Bit	Name	R/W	Description	Default
15:0	MDI	RO	Estimated level of narrowband differential 0x0 interference reported in µV as measured at the MDI interface for Pair B during the last retrain event.	0

2.4.1.68 MDI Differential Level on Pair C (DEVAD = 1, Address = 0xA8AC)

Table 81: MDI Differential Level on Pair C (1.0xA8AC)

Bit	Name	R/W	Description	Default
15:0	MDI	RO	Estimated level of narrowband differential 0x0 interference reported in µV as measured at the MDI interface for Pair C during the last retrain event.	0

2.4.1.69 MDI Differential Level on Pair D (DEVAD = 1, Address = 0xA8AD)

Table 82: MDI Differential Level on Pair D (1.0xA8AD)

Bit	Name	R/W	Description	Default
15:0	MDI	RO	Estimated level of narrowband differential 0x0 interference reported in µV as measured at the MDI interface for Pair D during the last retrain event.	0

2.4.2 AutogrEEEn Register Description (DEVAD = 1)

2.4.2.1 AutogrEEEn Control 1 Register (DEVAD = 1, Address = 0xA88A)

Table 83: AutogrEEEn Control 1 Register (1.0xA88A)

Bit	Name	R/W	Description	Default
15:3	Reserved	R/W	Use read-modify-write to not change the current value during write. Ignore on read.	Undetermined
8	RX_AUTOG_LPI_EN		1 = Receive AutogrEEEn LPI is enabled. 0 = Receive AutogrEEEn LPI is disabled.	0
7	Reserved	R/W	Use read-modify-write to not change the current value during write. Ignore on read.	Undetermined
6:4	ENC_LPI_EXT_VAL	R/W	The number of frames to extend clock gating for refresh for the out put interface after refresh is complete	0x1
3	TX_AI_RST	R/W	Transmit AutogrEEEn Reset 1 = Exit from AutogrEEEn w/o LPI and discard data in buffer. 0 = Normal operation	0
2	TX_AI_LAT_MODE	R/W	0 = Reserved. 1 = Constant latency.	0
1	TX AI_LPI MODE	R/W	1 = Transmit AutogrEEEn LPI is enabled. 0 = Transmit AutogrEEEn LPI is disabled.	0
0	AI LPI EN	R/W	1 = Transmit AutogrEEEn-state-mach-ready mode is enabled. 0 = Transmit AutogrEEEn-state-mach-ready mode is disabled.	0

2.4.2.2 AutogrEEEn Threshold High Register (DEVAD = 1, Address = 0xA88C)

Table 84: AutogrEEEn Threshold High Register (1.0xA88C)

Bit	Name	R/W	Description	Default
15:0	TX_AUTOG_LPI_THRS_H	R/W	AutogrEEEn threshold high.	00h

2.4.2.3 AutogrEEEn Threshold Low Register (DEVAD = 1, Address = 0xA88D)

Table 85: AutogrEEEn Threshold Low Register (1.0xA88D).

Bit	Name	R/W	Description	Default
15:0	TX_AUTOG_LPI_THRS_L	R/W	AutogrEEEn threshold low.	00h

2.4.2.4 AutogrEEEn Constant Latency Register (DEVAD = 1, Address = 0xA88E)

Table 86: AutogrEEEn Constant Latency Register (1.0xA88E)

Bit	Name	R/W	Description	Default
15:11	Reserved	R/W	Use read-modify-write to not change the current value during write. Ignore on read.	Undetermined
10:0	TX_AUTOG_CONS_ LATENCY	R/W	Transmit AutogrEEEn constant latency value.	0x47E

2.4.3 Fast Retrain Register Description (DEVAD = 1)

2.4.3.1 Fast Retrain PMD IEEE Status Register (DEVAD = 1, Address = 0xA92B)

Table 87: Fast Retrain Status Register (1.0xA92B)

Bit	Name	R/W	Description	Default
15:5	Reserved	RO	Ignore on read.	Undetermined
4	FR_ABILITY	R/W	Fast Retrain Ability Maps to register 1.0x93[4]. 1 = Fast Retrain Capability is supported. 0 = Fast Retrain Capability is not supported.	1
3	FR_NEGOTIATED	R/W	Fast Retrain Negotiated. Maps to register 1.0x93[3]. 1 = Fast retrain capability was negotiated. 0 = Fast retrain capability was not negotiated.	0
2:0	Reserved	RO	Ignore on read.	Undetermined

2.4.3.2 HiGig2 Enable Register (DEVAD = 1, Address = 0xA939)

Table 88: HiGig2 Enable Register (0xA939)

Bit	Name	R/W	Description	Default
15	PCS_MIN_IPG_DEL_EN	R/W	Enable PCS to delete the only IDLE column in IPG for clock compensation.	0
14:10	Reserved	RO	Ignore on read.	Undetermined
9	PCS_RX_MSG_LEN_32B	R/W	Enable 32-byte HiGig™ Messages on the PCS_RX.	0
8	PCS_RX_HIGIG_TS_EN	R/W	Enable TS code on the PCS_RX.	0
7	PCS_RX_HIGIG_EN	R/W	Enable HiGig mode in PCS_RX.	0
6:3	Reserved	RO	Ignore on read.	Undetermined
2	PCS_TX_MSG_LEN_32B	R/W	Enable 32-byte HiGig Messages on the PCS_TX.	0
1	PCS_TX_HIGIG_TS_EN	R/W	Enable TS code on the PCS_TX.	0
0	PCS_TX_HIGIG_EN	R/W	Enable HiGig mode in PCS_TX.	0

2.4.4 10GBASE-T Register Description (DEVAD = 3, PCS)

2.4.4.1 PCS Control 1 Register (DEVAD = 3, Address = 0x0000)

Table 89: PCS Control 1 Register (3.0x0000)

Bit	Name	R/W	Description	Default
15	RESET	SC	1 = PCS reset. 0 = Normal operation.	0
14	PCS_LPBK	R/W	1 = Enable PCS loopback mode. 0 = Disable PCS loopback mode.	0
13	SPEED_SEL_0	RO	Combined with bit 6 selects the speed. 13 6 1 1 = 10 Gb/s Other = Reserved	1
12	Reserved	R/W	Use read-modify-write to not change the current value during write. Ignore on read.	Undetermined
11	LOW_PWR	R/W	1 = Low-power mode. 0 = Normal operation.	0
10	Clock stoppable	R/W	1 = Clock stoppable during LPI. 0 = Clock not stoppable.	0
9:7	Reserved	R/W	Use read-modify-write to not change the current value during write. Ignore on read.	Undetermined
6	SPEED_SEL_1	RO	See bit 13.	1

Table 89: PCS Control 1 Register (3.0x0000) (Continued)

Bit	Name	R/W	Description	Default
5:2	SPEED_SEL_10G	R/W	5 4 3 2 1 1 x x = Reserved 1 0 1 x = Reserved 1 0 0 1 = Reserved 1 0 0 0 = 5 Gb/s 0 1 1 1 = 2.5 Gb/s 0 1 1 0 = Reserved 0 1 0 1 = reserved 0 1 0 0 = Reserved 0 0 1 1 = Reserved 0 0 1 0 = 10/1 Gb/s 0 0 0 1 = Reserved 0 0 0 0 = 10 Gb/s	0x0
1:0	Reserved	R/W	Use read-modify-write to not change the current value during write. Ignore on read.	Undetermined

2.4.4.2 PCS Status 1 Register (DEVAD = 3, Address = 0x0001)

Table 90: PCS Status 1 Register (3.0x0001)

Bit	Name	R/W	Description	Default
15:12	Reserved	RO	Ignore on read.	Undetermined
11	TX LP idle received	RO/LH	1 = TX PCS has received LP idle. 0 = LP Idle not received.	0
10	RX LP idle received	RO/LH	1 = RX PCS has received LP idle. 0 = LP Idle not received.	0
9	TX LP idle indication	RO	1 = TX PPCS is currently receiving LP idle. 0 = PCS is not currently receiving LP idle.	0
8	RX LP idle indication	RO	1 = RX PCS is currently receiving LP idle. 0 = No fault condition detected.	0
7	FAULT	RO	1 = Fault condition detected 0 = Fault condition not detected	0
6:3	Reserved	RO	Ignore on read.	Undetermined
2	PCS_RCV_LINK_ST	RO/LL	PCS receive link status: 1 = PCS receive linkup. 0 = PCS receive link down.	0
1	LOW_PWR_AB	RO	Low-power ability: 1 = PCS supports low-power mode. 0 = PCS does not support low-power mode.	1
0	Reserved	RO	Ignore on read.	Undetermined

2.4.4.3 PCS Device Identifier Part 0 (DEVAD = 3, Address = 0x0002)

Table 91: PCS Device Identifier Part 0 (3.0x0002)

Bit	Name	R/W	Description	Default
15:0	DEV_ID0	RO	Combined with PCS_DEV_ID1 forms the PCS device identifier.	0x3590

2.4.4.4 PCS Device Identifier Part 1 (DEVAD = 3, Address = 0x0003)

Table 92: PCS Device Identifier Part 1 (3.0x0003)

Bit	Name	R/W	Description	Default
15:0	DEV_ID1	RO	Combined with PCS_DEV_ID0 forms the PCS device identifier.	A0: 0x5080 B0: 0x5081

2.4.4.5 PCS Speed Ability (DEVAD = 3, Address = 0x0004)

Table 93: PCS Speed Ability (3.0x0004)

Bit	Name	R/W	Description	Default
15:8	Reserved	RO	Ignore on read.	Undetermined
7	CAP_5G	RO	5G capable. 1 = PCS is capable of operating at 5 Gb/s. 0 = PCS is not capable of operating at 5 Gb/s. Reset value is 0x1.	0x1
6	CAP_2P5G	RO	2.5G capable. 1 = PCS is capable of operating at 2.5 Gb/s. 0 = PCS is not capable of operating at 2.5 Gb/s. Reset value is 0x1.	0x1
1	CAP_10P2B	RO	2BASE-TL capable 1 = PCS is capable of operating at 10P/2B PCS. 0 = PCS/PCS is not capable of operating at 10P/2B PCS.	0
0	CAP_10G	RO	10G capable 1 = PCS is capable of operating at 10 Gb/s. 0 = PCS is not capable of operating at 10 Gb/s.	1

2.4.4.6 Devices 0 Package Register (DEVAD = 3, Address = 0x0005)

Table 94: Devices 0 Package Register Part 0 (3.0x0005)

Bit	Name	R/W	Description	Default
15:8	Reserved	RO	Ignore on read.	Undetermined
7	AUTONEG_PRE	RO	Auto-Negotiation present: 1 = Auto-Negotiation present in package. 0 = Auto-Negotiation not present in package.	1
6	TC_PRE	RO	TC present: 1 = TC present in package. 0 = TC not present in package.	0

Table 94: Devices 0 Package Register Part 0 (3.0x0005) (Continued)

Bit	Name	R/W	Description	Default
5	DTEXS_PRE	RO	DTE XS present: 1 = DTE XS present in package. 0 = DTE XS not present in package.	0
4	PHYXS_PRE	RO	PHY XS present: 1 = PHY XS present in package. 0 = PHY XS not present in package.	1
3	PCS_PRE	RO	PCS present: 1 = PCS present in package. 0 = PCS not present in package.	1
2	WIS_PRE	RO	WIS present: 1 = WIS present in package. 0 = WIS not present in package.	0
1	PMD_PRE	RO	PMD/PMA present: 1 = PMD/PMA present in package. 0 = PMD/PMA not present in package.	1
0	CLA22_PRE[a]	RO	Clause 22 registers present: 1 = Clause 22 registers present in package. 0 = Clause 22 registers not present in package.	1

a. Clause 22 registers are accessible through Clause 45.

2.4.4.7 Devices 1 Package Register (DEVAD = 3, Address = 0x0006)

Table 95: Devices 1 Package Register (3.0x0006)

Bit	Name	R/W	Description	Default
15	VENSP_DEV2_PRE	RO	Vendor-specific device 2 present: 1 = Vendor-specific device 2 present in package. 0 = Vendor-specific device 2 not present in package.	1
14	VENSP_DEV1_PRE	RO	Vendor-specific device 1 present: 1 = Vendor-specific device 1 present in package. 0 = Vendor-specific device 1 not present in package.	1
13	CLA22_EXT_PRE	RO	Clause 22 extension present: 1 = Clause 22 extension present in package. 0 = Clause 22 extension not present in package.	0
12:0	Reserved	RO	Ignore on read.	Undetermined

2.4.4.8 PCS Control 2 Register (DEVAD = 3, Address = 0x0007)

Table 96: PCS Control 2 Register (3.0x0007)

Bit	Name	R/W	Description	Default
15:2	Reserved	RO	Ignore on read.	Undetermined
1:0	TYPE_SEL	RO	PCS type selection: 3 2 1 0 1 0 x x = Reserved 1 0 1 1 = Select 5GBASE-T PCS type 1 0 1 0 = Select 2.5GBASE-T PCS type 0 1 0 1 = Reserved 0 1 0 0 = Reserved 0 0 1 1 = Select 10GBASE-T PCS type 0 0 1 0 = Select 10GBASE-W PCS type 0 0 0 1 = Select 10GBASE-X PCS type 0 0 0 0 = Select 10GBASE-R PCS type Reset value is 0x3.	0x3

2.4.4.9 10G PCS Status 2 Register (DEVAD = 3, Address = 0x0008)

Table 97: 10G PCS Status 2 Register (3.0x0008)

Bit	Name	R/W	Description	Default
15:14	DEV_PRE	RO	Device present: 15 14 1 0 = Device responding at this address. 1 1 = No device responding at this address. 0 1 = No device responding at this address. 0 0 = No device responding at this address. Reset value is 2.	2
13	CAP_5G_T	RO	5GBASE_T ability. 1 = PCS can perform 5GBASE-T. 0 = PCS cannot perform 5GBASE-T. Reset value is 0x1.	0x1
12	CAP_2P5G_T		2.5GBASE_T ability. 1 = PCS can perform 2.5GBASE-T. 0 = PCS cannot perform 2.5GBASE-T. Reset value is 0x1.	0x1
11	TRAN_FALT	RO	Transmit fault: If no ability, should be reserved. 1 = Fault condition on transmit path. 0 = No fault condition on transmit path.	0
10	RCV_FALT	LH	Receive fault: 1 = Fault condition on receive path. 0 = No fault condition on receive path	0
9:4	Reserved	RO	Ignore on read.	Undetermined

Table 97: 10G PCS Status 2 Register (3.0x0008) (Continued)

Bit	Name	R/W	Description	Default
3	CAP_10G_T	RO	10GBASE_T ability: 1 = PCS can perform 10GBASE-T. 0 = PCS cannot perform 10GBASE-T.	1
2	CAP_10G_W	RO	10GBASE_W ability: 1 = PCS can perform 10GBASE-W. 0 = PCS cannot perform 10GBASE-W.	0
1	CAP_10G_X	RO	10GBASE_X ability: 1 = PCS can perform 10GBASE-X. 0 = PCS cannot perform 10GBASE-X.	0
0	CAP_10G_R	RO	10GBASE_X ability: 1 = PCS can perform 10GBASE-R. 0 = PCS cannot perform 10GBASE-R.	0

2.4.4.10 PCS Package Identifier 0 (DEVAD = 3, Address = 0x000E)

Table 98: PCS Package Identifier 0 (3.0x000E)

Bit	Name	R/W	Description	Default
15:0	PKG_ID_0	RO	PCS package identifier part 0	0

2.4.4.11 PCS Package Identifier 1 (DEVAD = 3, Address = 0x000F)

Table 99: PCS Package Identifier 1 (3.0x000F)

Bit	Name	R/W	Description	Default
15:0	PKG_ID_1	RO	PCS package identifier part 1	0

2.4.4.12 EEE Capability Register (DEVAD = 3, Address = 0x0014)

Table 100: 10GBASE_T PCS Status 1 (3.0x0014)

Bit	Name	R/W	Description	Default
15:7	Reserved	RO	Ignore on read.	Undetermined
6	10GBASE-KER	RO	1 = EEE is supported for 10GBASE-KR. 0 = EEE is not supported for 10GBASE-KR.	0
5	10GBASE-KX4	RO	1 = EEE is supported for 10GBASE-KX4. 0 = EEE is not supported for 10GBASE-KX4.	0
4	10GBASE-KX EEE	RO	1 = EEE is supported for 10GBASE-KX. 0 = EEE is not supported for 10GBASE-KX.	0
3	10GBASE-T EEE	RO	1 = EEE is supported for 10GBASE-T. 0 = EEE is not supported for 10GBASE-T.	10
2	1000BASE-T EEE	RO	1 = EEE is supported for 1000BASE-T. 0 = EEE is not supported for 1000BASE-T.	0
1	100BASE-TX EEE	RO	1 = EEE is supported for 100BASE-TX. 0 = EEE is not supported for 100BASE-TX.	0
0	Reserved	RO	Ignore on read.	Undetermined

2.4.4.13 10GBASE_T PCS_EEE_WAKE_ERR_CNT Register (DEVAD = 3, Address = 0x0016)

Table 101: 10GBASE_T PCS_EEE_WAKE_ERR_CNT Register (DEVAD = 3, Address = 0x0016)

Bit	Name	R/W	Description	Default
15:0	EEE_WAKE_ERR_CNT	RO	This register is used by PHY types that support EEE to count wake-time faults (WTF) where the PHY fails to complete its normal wake sequence within the time required for the specific PHY type. The definition of the WTF event to be counted is defined for each PHY and may occur during a refresh or a wakeup as defined by the PHY. This counter shall be reset to all zeros when the EEE wake error counter is read by the management function or upon execution of the PCS reset. This counter shall be held at all ones in the case of overflow.	0

2.4.4.14 10GBASE_T PCS Status 1 (DEVAD = 3, Address = 0x0020)

Table 102: 10GBASE_T PCS Status 1 (3.0x0020)

Bit	Name	R/W	Description	Default
15:13	Reserved	RO	Ignore on read.	Undetermined
12	RCV_LINK_STS	RO	10GBASE-T receive link status: 1 = 10GBASE-R or 10GBASE-T PCS receive linkup. 0 = 10GBASE-R or 10GBASE-T PCS receive linkdown.	0
11:3	Reserved	RO	Ignore on read.	Undetermined
2	PRBS31_CAP	RO	PRBS31 pattern testing ability: 1 = PCS can support PRBS31 pattern testing. 0 = PCS cannot support PRBS31 pattern testing.	0
1	HBER	RO	PCS high BER: 1 = PCS reporting a high BER. 0 = PCS not reporting a high BER.	0
0	BLK_LOCK	RO	PCS block lock: 1 = PCS locked to received blocks. 0 = PCS not locked to received blocks.	0

2.4.4.15 10GBASE_T PCS Status 2 (DEVAD = 3, Address = 0x0021) 15867339858

Table 103: 10GBASE_T PCS Status 2 (3.0x0021)

Bit	Name	R/W	Description	Default
15	BLK_LOCK_L	LL	Latched low block lock: 1 = PCS locked to received blocks. 0 = PCS not locked to received blocks.	0
14	HBER_L	LH	Latched high BER: 1 = PCS reporting a high BER. 0 = PCS not reporting a high BER.	1
13:8	BER	RO	BER counter: This is the same as LFER_COUNT. It saturates at 0x3F. Clear by read of this register or every 125 µs.	0
7:0	ERR_BLK_CNT	RO	Errored blocks counter: Saturates at 0xFF. Clear by read of this register.	0

2.5 AN Registers Descriptions (DEVAD = 7, AN)

2.5.1 10GBASE-T AN Control Register (DEVAD = 7, Address = 0x0000)

Table 104: 10GBASE-T AN Control Register (7.0x0000)

Bit	Name	R/W	Description	Default
15	RESET	SC	Reset.	0
14	RESERVED	R/W	Use read-modify-write to not change the current value during write. Ignore on read.	Undetermined
13	EXTENDED_NP_CTRL	R/W	Extended next page control.	1
12	AN_ENABLE	R/W	Auto-negotiation enable.	1
11:10	RESERVED	R/W	Use read-modify-write to not change the current value during write. Ignore on read.	Undetermined
9	RESTART_AN_ENABLE	SC	Restart auto-negotiation enable.	0
8:0	RESERVED	R/W	Use read-modify-write to not change the current value during write. Ignore on read.	Undetermined

2.5.2 10GBASE-T AN Status Register (DEVAD = 7, Address = 0x0001)

Table 105: 10GBASE-T AN Status Register (7.0x0001)

Bit	Name	R/W	Description	Default
15:10	RESERVED	RO	Ignore on read.	Undetermined
9	PARALLEL_DETECTION_FAULT	RO	1 = A fault has been detected through the parallel detection function. 0 = A fault has not been detected through the parallel detection function	0
7	EXTENDED_NP_STAT	RO	Extended next page status	0
6	PAGE_RECEIVED	LH	Page received	0
5	AUTONEG_COMPLETE	RO	Auto-negotiation complete.	0
4	REMOTE_FAULT	LH	Remote fault.	0

Table 105: 10GBASE-T AN Status Register (7.0x0001) (Continued)

Bit	Name	R/W	Description	Default
3	AUTONEG_ABILITY	RO	Auto-negotiation ability.	0
2	LINK_STATUS	RO	Link status.	0
1	RESERVED	RO	Ignore on read.	Undetermined
0	LP_AUTONEG_ABILITY	RO	Link partner AN ability.	0

2.5.3 10GBASE-T AN Device ID 1 Register (DEVAD = 7, Address = 0x0002)

Table 106: 10GBASE-T AN Device ID-1 Register (7.0x0002)

Bit	Name	R/W	Description	Default
15:0	AUTONEG_DEV_ID_1	R0	Auto-negotiation device identifier bits 15 to 0.	0x3590

2.5.4 10GBASE-T AN Device ID 2 Register (DEVAD = 7, Address = 0x0003)

Table 107: 10GBASE-T AN Device ID-2 Register (7.0x0003)

Bit	Name	R/W	Description	Default
15:0	AUTONEG_DEV_ID_2	R0	Auto-negotiation device identifier bits 31 to 16.	A0: 0x5080 B0: 0x5081

2.5.5 10GBASE-T AN Device In Package 0 Register (DEVAD = 7, Address = 0x0005)

Table 108: 10GBASE-T AN Device In Package 0 Register (7.0x0005)

Bit	Name	R/W	Description	Default
15:0	AUTONEG_DEV_INPKG_0	R0	Auto-negotiation device in package identifier bits 15 to 0.	0x0000

2.5.6 10GBASE-T AN Device In Package 1 Register (DEVAD = 7, Address = 0x0006)

Table 109: 10GBASE-T AN Device In Package 1 Register (7.0x0006)

Bit	Name	R/W	Description	Default
15:0	AUTONEG_DEV_INPKG_1	R0	Auto-negotiation device in package identifier bits 31 to 16.	0x0000

2.5.7 10GBASE-T AN Package ID 0 Register (DEVAD = 7, Address = 0x000E)

Table 110: 10GBASE-T AN Package ID 0 Register (7.0x000E)

Bit	Name	R/W	Description	Default
15:0	AUTONEG_PCKG_ID_0	R0	Auto-negotiation device in package identifier bits 15 to 0.	0x0000

2.5.8 10GBASE-T AN Package ID 1 Register (DEVAD = 7, Address = 0x000F)

Table 111: 10GBASE-T AN Package ID 1 Register (7.0x000F)

Bit	Name	R/W	Description	Default
15:0	AUTONEG_PCKG_ID_1	R0	Auto-negotiation device in package identifier bits 31 to 16.	0x0000

2.5.9 10GBASE-T AN Advertisement 1 Register (DEVAD = 7, Address = 0x0010)

Table 112: 10GBASE-T AN Advertisement 1 Register (7.0x0010)

Bit	Name	R/W	Description	Default
15	NEXT_PAGE	R/W	Next page	0
14	ACKNOWLEDGE	RO	Acknowledge	0
13	REMOTE_FAULT	R/W	Remote Fault	0
12	XNP	R/W	Next page	1
11:5	TECHNOLOGY ABILITY FIELD	R/W	Technology ability field	0
4:0	SELECTOR	R/W	Selector field	0x0

2.5.10 10GBASE-T AN LP BASE Page Ability 1 Register (DEVAD = 7, Address = 0x0013)

Table 113: 10GBASE-T AN LP BASE Page Ability 1 Register (7.0x0013)

Bit	Name	R/W	Description	Default
15	Next page	R/W	Next page	0
14	Acknowledge	RO	Acknowledge	0
13	Remote fault	R/W	Remote fault	0
12	Extended next page ability	R/W	1 = Extended next page capable. 0 = Is not extended next page capable.	0
11:5	Technology ability field	R/W	Technology ability field	0
4:0	Selector field	R/W	Selector field	0

2.5.11 10GBASE-T AN XNP Transmit 1 Register (DEVAD = 7, Address = 0x0016)

Table 114: 10GBASE-T AN XNP Transmit 1 Register (7.0x0016)

Bit	Name	R/W	Description	Default
15	Next Page	R/W	Next Page	0
14	RSVD	R0	Ignore on read	0
13	MSG	R/W	Message	0
12	Ack2	R/W	Acknowledge 2	0
11	Tog	RO	Toggle	0
10:0	UN_CODE_FIELD	R/W	Unformatted code Field	0

2.5.12 10GBASE-T AN XNP Transmit 2 Register (DEVAD = 7, Address = 0x0017)

Table 115: 10GBASE-T AN XNP Transmit 2 Register (7.0x0017)

Bit	Name	R/W	Description	Default
15:0[a]	MSG_UNFRMT_CODE_26_11	R/W	Message unformatted code	0

a. The extended Unformatted Code Field is a 32-bit or 43-bit wide field.

2.5.13 10GBASE-T AN XNP Transmit 3 Register (DEVAD = 7, Address = 0x0018)

Table 116: 10GBASE-T AN XNP Transmit 3 Register (7.0x0018)

Bit	Name	R/W	Description	Default
15:0[a]	MSG_UNFRMT_CODE_42_27	R/W	Message unformatted code	0

a. The extended Unformatted Code Field is a 32-bit or 43-bit wide field.

2.5.14 10GBASE-T AN LP XNP Ability 1 Register (DEVAD = 7, Address = 0x0019)

Table 117: 10GBASE-T AN LP XNP Ability 1 Register (7.0x0019)

Bit	Name	R/W	Description	Default
15	NEXT_PAGE	R0	Next page	0
14	ACKNOWLEDGE	R0	Acknowledge	0
13	MESSAGE_PAGE	R0	Message page	0
12	ACKNOWLEDGE_2	R0	Acknowledge 2	0
11	TOGGLE	R0	Toggle	00
10:0	MSG_UNFRMT_CODE_10_0	R0	Message unformatted code	0x0

2.5.15 10GBASE-T AN LP XNP Ability 2 Register (DEVAD = 7, Address = 0x001A)

Table 118: 10GBASE-T AN LP XNP Ability 2 Register (7.0x001A)

Bit	Name	R/W	Description	Default
15:0[a]	MSG_UNFRMT_CODE_26_11	R/W	Message unformatted code	0

a. The extended Unformatted Code Field is a 32-bit or 43-bit wide field.

2.5.16 10GBASE-T AN LP XNP Ability 3 Register (DEVAD = 7, Address = 0x001B)

Table 119: 10GBASE-T AN LP XNP Ability 3 Register (7.0x001B)

Bit	Name	R/W	Description	Default
15:0[a]	MSG_UNFRMT_CODE_42_27	R/W	Message unformatted code	0

a. The extended Unformatted Code Field is a 32-bit or 43-bit wide field.

2.5.17 10GBASE-T AN Control (DEVAD = 7, Address = 0x0020)

Table 120: 10GBASE-T AN Control (7.0x0020)

Bit	Name	R/W	Description	Default
15	MASTER_SLAVE_MAN_CONFIG_EN	R/W	1 = Enable Master-Slave manual configuration. 0 = Disable Master-Slave manual configuration.	0
14	MASTER_SLAVE_CONFIG_VAL	R/W	1 = Configure PHY as Master. 0 = Configure PHY as Slave.	0
13	PORT_TYPE	R/W	1 = Multiport device. 0 = Single-port device.	0
12	10GBASE_T_ABILITY	R/W	1 = Advertise PHY as 10GBASE-T capable. 0 = Do not advertise the PHY as 10GBASE-T capable.	10
11:9	RESERVED	RO	Ignore on read.	Undetermined
8	LD_PHY_5GBASE_T_ABLE	R/W	1 = Advertise PHY as 5GBASE-T capable. 0 = Do not advertise PHY as 5GBASE-T capable. Reset value is 0x0.	0x0
7	LD_PHY_2P5GBASE_T_ABLE	R/W	1 = Advertise PHY as 2.5GBASE-T capable. 0 = Do not advertise PHY as 2.5GBASE-T capable Reset value is 0x0.	0x0
6	LD_FAST_RETRAIN_CAPABLE_5G	R/W	1 = Advertise PHY as capable of fast retrain in 5GBASE-T mode. 0 = Do not advertise PHY as capable of fast retrain in 5GBASE-T mode. Reset value is 0x0.	0x0
5	LD_FAST_RETRAIN_CAPABLE_2P5G	R/W	1 = Advertise PHY as capable of fast retrain in 2.5GBASE-T mode. 0 = Do not advertise PHY as capable of fast retrain in 2.5GBASE-T mode. Reset value is 0x0.	0x0
4:3	RESERVED	RO	Ignore on read.	Undetermined
2	LD_PMA_TRAIN_RESET_REQ	R/W	1 = Local device requests that link partner reset PMA training PRBS every frame. 0 = Local device requests that link partner run PMA training PRBS continuously.	1
1	RESERVED	RO	Ignore on read.	Undetermined
0	LD_LOOP_TIMING_ABILITY	RO LH	1 = Advertise PHY as capable of loop timing. 0 = Do not advertise PHY as capable of loop timing.	1

2.5.18 10GBASE-T AN Status (DEVAD = 7, Address = 0x0021)

Table 121: 10GBASE-T AN Status (7.0x0021)

Bit	Name	R/W	Description	Default
15	MASTER_SLAVE_CONFIG_FAULT	RO LH SC	1 = Master-Slave configuration fault detect. 0 = No Master-Slave configuration fault detected.	0h
14	MASTER_SLAVE_CONFIG_RES	RO	1 = Local PHY configuration resolved to Master. 0 = Local PHY configuration resolved to Slave.	0
13	LOCAL_RX_STAT	RO	1 = Local receiver OK. 0 = Local receiver not OK.	0

Table 121: 10GBASE-T AN Status (7.0x0021) (Continued)

Bit	Name	R/W	Description	Default
12	REMOTE_RX_STAT	RO	1 = Remote receiver OK. 0 = Remote receiver not OK.	0
11	LP_10GBASE_T_ CAPABILITY	RO	1 = Link partner can operate as 10GBASE-T. 0 = Link partner cannot operate as 10GBSE-T. This bit is guaranteed to be valid only when the Page received bit (Device 7 register 0x0001 bit 6) has been set to 1.	0
10	LP_LOOP_TIMING_ABILITY	RO	1 = Link partner is capable of loop timing. 0 = Link partner is not capable of loop timing.	0
9	LP_PMA_TRAIN_RESET_ REQ	RO	1 = Link partner requests that local device reset PMA training PRBS every frame. 0 = Link partner requests that local device run PMA training PRBS continuously.	0
8:7	RESERVED	RO	Ignore on read.	Undetermined
6	LP_PHY_5GBASE_T_ABLE	RO	1 = Link partner can operate as 5GBASE-T. 0 = Link partner cannot operate as 5GBASE-T. Reset value is 0x0.	0x0
5	LP_PHY_2P5GBASE_T_ ABLE	RO	1 = Link partner can operate as 2.5GBASE-T. 0 = Link partner cannot operate as 2.5GBASE-T. Reset value is 0x0.	0x0
4	LP_FAST_RETRAIN_ CAPABLE_5G	RO	1 = Link partner advertises PHY as capable of fast retrain in 5GBASE-T mode. 0 = Link partner does not advertise PHY as capable of fast retrain in 5GBASE-T. Reset value is 0x0.	0x0
3	LP_FAST_RETRAIN_ CAPABLE_2P5G	RO	1 = Link partner advertise PHY as capable of fast retrain in 2.5GBASE-T mode. 0 = Link partner does not advertise PHY as capable of fast retrain in 2.5GBASE-T. Reset value is 0x0.	0x0
2	Reserved	RSVD	Reserved bit write has no effect and read always returns 0.	–
1	LP_FAST_RETRAIN_ CAPABLE_10G	RO	1 = Link partner advertises PHY as capable of fast retrain in 10GBASE-T mode. 0 = Link partner does not advertise PHY as capable of fast retrain in 10GBASE-T. Reset value is 0x0.	0x0
0	Reserved	RSVD	Reserved bit write has no effect and read always returns 0.	–

2.5.19 EEE Advertisement Register (DEVAD = 7, Address = 0x003C)

Table 122: EEE Advertisement Register (7.0x003C)

Bit	Name	R/W	Description	Default
15:7	RESERVED	RO	Ignore on read.	Undetermined
6	10GBASE-KR EEE	R/W	1 = EEE is supported for 10GBASE-KR. 0 = EEE is not supported for 10GBASE-KR.	0

Table 122: EEE Advertisement Register (7.0x003C) (Continued)

Bit	Name	R/W	Description	Default
5	10GBASE-KX4 EEE	R/W	1 = EEE is supported for 10GBASE-KX4. 0 = EEE is not supported for 10GBASE-KX4.	0
4	100BASE-KX EEE	R/W	1 = EEE is supported for 100BASE-KX. 0 = EEE is not supported for 100BASE-KX.	0
3	10GBASE-T EEE	R/W	1 = EEE is supported for 10GBASE-TX. 0 = EEE is not supported for 10GBASE-TX.	1
2	1000BASE-T EEE	R/W	1 = EEE is supported for 1000BASE-T. 0 = EEE is not supported for 1000BASE-T.	1
1	100BASE-TX EEE	R/W	1 = EEE is supported for 100BASE-TX. 0 = EEE is not supported for 100BASE-TX.	1
0	RESERVED	RO	Ignore on read.	Undetermined

2.5.20 EEE Advertisement 2 Register (DEVAD = 7, Address = 0x003E)

Table 123: EEE Advertisement 2 Register (7.0x003E)

Bit	Name	R/W	Description	Default
15:2	Reserved	RSVD	Reserved bits write has no effect and read always returns 0.	Undetermined
1	PHY_5GBASE_T_ EEE	RW	1 = Advertise that the 5GBASE-T has EEE capability. 0 = Do not advertise that the 5GBASE-T has EEE capability. Reset value is 0x0.	0x0
0	PHY_2P5GBASE_T_ EEE	RW	1 = Advertise that the 2.5GBASE-T has EEE capability. 0 = Do not advertise that the 2.5GBASE-T has EEE capability. Reset value is 0x0.	0x0

2.5.21 EEE Link Partner Advertisement 2 Register (DEVAD = 7, Address = 0x003F)

Table 124: EEE Link Partner Advertisement 2 Register (7.0x003F)

Bit	Name	R/W	Description	Default
15:2	Reserved	RSVD	Reserved bits write has no effect and read always returns 0.	–
1	LP_PHY_5GBASE_T_EEE	RO	1 = Link partner advertises that the 5GBASE-T has EEE capability. 0 = Link partner does not advertise that the 5GBASE-T has EEE capability. Reset value is 0x0.	0x0
0	LP_PHY_2P5GBASE_T_E EE	RO	1 = Link partner advertise that the 2.5GBASE-T has EEE capability. 0 = Link partner does not advertise that the 2.5GBASE-T has EEE capability. Reset value is 0x0.	0x0

2.5.22 Multi-GBASET AN Control 2 Register (DEVAD = 7, Address = 0x0040)

Table 125: Multi-GBASET AN Control 2 Register (7.0x0040)

Bit	Name	R/W	Description	Default
15:4	Reserved	RSVD	Reserved bits write has no effect and read always returns 0.	–
3	LD_2P5GBASE_T_ THP_BYPASS_ REQUEST	RW	1 = Local device requests link partner to initially reset THP during fast retrain. 0 = Local device requests link partner not to initially reset THP during fast retrain. Reset value is 0x0.	0x0
2	LD_5GBASE_T_ THP_BYPASS_ REQUEST	RW	1 = Local device requests link partner to initially reset THP during fast retrain. 0= Local device requests link partner not to initially reset THP during fast retrain. Reset value is 0x0.	0x0
1:0	Reserved	RSVD	Reserved bits write has no effect and read always returns 0.	—

2.5.23 Multi-GBASET AN Status 2 Register (DEVAD = 7, Address = 0x0041)

Table 126: Multi-GBASET AN Status 2 Register (7.0x0041)

Bit	Name	R/W	Description	Default
15:4	Reserved	RSVD	Reserved bits write has no effect and read always returns 0.	—
3	LP_2P5GBASE_T_ THP_BYPASS_ REQUEST	RO	1 = Link partner requests local device to initially reset THP during fast retrain. 0= Link partner requests local device not to initially reset THP during fast retrain. Reset value is 0x0.	0x0
2	LP_5GBASE_T_THP_BYPASS_REQUEST	RO	1 = Link partner requests local device to initially reset THP during fast retrain 0= Link partner requests local device not to initially reset THP during fast retrain. Reset value is 0x0.	0x0
1:0	Reserved	RSVD	Reserved bits write has no effect and read always returns 0.	—

2.5.24 EEE Link Partner Advertisement Register (DEVAD = 7, Address = 0x003D)

Table 127: EEE Link Partner Advertisement Register (7.0x003D)

Bit	Name	R/W	Description	Default
15:7	RESERVED	RO	Ignore on read.	Undetermined
6	10GBASE-KR EEE	RO	1 = EEE is supported for 10GBASE-KR. 0 = EEE is not supported for 10GBASE-KR.	0
5	10GBASE-KX4 EEE	RO	1 = EEE is supported for 10GBASE-KX4. 0 = EEE is not supported for 10GBASE-KX4.	0
4	100BASE-KX EEE	RO	1 = EEE is supported for 100BASE-KX. 0 = EEE is not supported for 100BASE-KX.	0
3	10GBASE-T EEE	RO	1 = EEE is supported for 10GBASE-TX. 0 = EEE is not supported for 10GBASE-TX.	10

Table 127: EEE Link Partner Advertisement Register (7.0x003D) (Continued)

Bit	Name	R/W	Description	Default
2	1000BASE-T EEE	RO	1 = EEE is supported for 1000BASE-T. 0 = EEE is not supported for 1000BASE-T.	0
1	100BASE-TX EEE	RO	1 = EEE is supported for 100BASE-TX. 0 = EEE is not supported for 100BASE-TX.	0
0	RESERVED	RO	Ignore on read.	Undetermined

2.6 1000BASE-T/100BASE-TX Registers Descriptions (DEVAD = 7, PCS, PMA)

2.6.1 1000BASE-T/100BASE-TX MII Control (DEVAD = 7, Address = 0xFFE0)

Table 128: 1000BASE-T/100BASE-TX MII Control Register (7.0xFFE0)

Bit	Name	R/W	Description	Default
15	Reset	R/W SC	Write 1 to reset the BCM84891L by software control. This bit self-clears after the reset process is complete and does not need to be cleared using a second MII write. Writes to other register bits have no effect until the reset process is completed, which requires approximately 2.0 µs. Writing 0 to this bit has no effect. When bit is read during the reset process, a 1 is returned; otherwise, a 0 is returned. 1 = PHY reset. 0 = Normal operation. **NOTE:** Do not use this bit to reset PHY, since it causes a conflict with this firmware.	0
14	Internal Loopback	R/W	This bit places the BCM84891L into internal loopback mode. Loopback mode can be cleared by writing 0 to bit 14 of the MII Control register or by resetting the chip. When this bit is read and the chip is in loopback mode, a 1 is returned; otherwise, a 0 is returned. 1 = Loopback mode. 0 = Normal operation.	0
13	Speed Selection (LSB)	R/W	When auto-negotiation is disabled, bits 6 and 13 of the MII Control register can be used to manually select the speed of operation. When bit 6 is set and bit 13 is cleared, 1000BASE-T operation is selected. When bit 6 is cleared and bit 13 is set, 100BASE-TX operation is selected. Setting both bits is not permitted. When read, these bits return the last value written. Bits [6,13]: 11 = Reserved. 10 = 1000 Mb/s. 01 = 100 Mb/s. 00 = Reserved.	1

Table 128: 1000BASE-T/100BASE-TX MII Control Register (7.0xFFE0) (Continued)

Bit	Name	R/W	Description	Default
12	Auto-negotiation Enable	R/W	When set, the mode of operation is controlled by auto-negotiation. When cleared, the mode of operation is determined by the manual speed, duplex mode, and master/slave configuration bits. When read with auto-negotiation enabled, a 1 is returned; otherwise, a 0 is returned. 1 = Auto-negotiation enabled. 0 = Auto-negotiation disabled.	1
11	Power Down	R/W	When this bit is set, the BCM84891L is placed into low-power standby mode. At the default, the SerDes interface is powered down when the device is in copper mode, and vice versa, except in media converter or SGMII modes, where both media are powered on. **NOTE:** When auto-medium mode detection is enabled, the power bit of register 00h bit 11 is controlled by the internal state machine to power-down the interface when it is selected. A 1 should not be written to this bit. 1 = Power-down. 0 = Normal operation.	0
10	Isolate	R/W	Set to isolate the BCM84891L from the MAC interface. All MAC interface outputs are tristated, and all MAC interface inputs are ignored. Because the management interface is still active, isolate mode can be cleared by writing 0 to bit 10 of the MII Control register or by resetting the chip. When this bit is read and the chip is in isolate mode, a 1 is returned; otherwise, a 0 is returned. This default of this bit is 0. 1 = Electrically isolate PHY. 0 = Normal operation.	1 = When phya + phyanumb = 00000, else 0
9	Restart Auto-negotiation	R/W SC	Setting bit 9 forces the auto-negotiation process to be restarted, regardless of the current state of the auto-negotiation state machine. When auto-negotiation is enabled, setting this bit restarts the auto-negotiation process. Clearing this bit has no effect. This bit is self-clearing. After the auto-negotiation process has restarted, it returns 0. 1 = Restarting auto-negotiation. 0 = Auto-negotiation restart complete.	0
8	Duplex Mode	R/W	When auto-negotiation is disabled, duplex mode of can be controlled by writing to this bit. Setting this bit forces the BCM84891L into full-duplex operation; clearing this bit forces the BCM84891L into half-duplex operation. When this bit is read, it returns the last value written. 1 = Full-duplex. 0 = Half-duplex.	1
7	Collision Test Enable	R/W	Set to enter collision test mode. In this mode, the COL pin is asserted whenever the TX_EN pin is driven high. Collision test mode can be cleared by writing 0 to bit 7 of the MII Control register or by resetting the chip. When this bit is read and the chip is in collision test mode, a 1 is returned; otherwise, a 0 is returned. 1 = Enable the collision test mode. 0 = Disable the collision test mode.	0

Table 128: 1000BASE-T/100BASE-TX MII Control Register (7.0xFFE0) (Continued)

Bit	Name	R/W	Description	Default
6	Speed Selection (MSB)	R/W	When auto-negotiation is disabled, bits 6 and 13 can be used to manually select the speed of operation. When bit 6 is set and bit 13 is cleared, 1000BASE-T operation is selected. When bit 6 is cleared and bit 13 is set, 100BASE-TX operation is selected. Setting both bits is not permitted. When read, these bits return the last value written.	1
5:0	Reserved	R/W	Use read-modify-write to not change the current value during write. Ignore on read.	Undetermined

2.6.2 1000BASE-T/100BASE-TX MII Status (DEVAD = 7, Address = 0xFFE1)

Table 129: 1000BASE-T/100BASE-TX MII Status Register (7.0xFFE1)

Bit	Name	R/W	Description	Default
15	100BASE-T4 Capable	RO L	The BCM84891L is not capable of 100BASE-T4 operation and returns 0 when this bit is read. 1 = 100BASE-T4 capable. 0 = Not 100BASE-T4 capable.	0
14	100BASE-X Full-duplex Capable	RO H	The BCM84891L is capable of 100BASE-TX full-duplex operation and returns 1 when this bit is read. 1 = 100BASE-X full-duplex capable. 0 = Not 100BASE-X full-duplex capable.	1
13	100BASE-X Half-duplex Capable	RO H	The BCM84891L is capable of 100BASE-X half-duplex operation and returns 1 this bit is read. 1 = 100BASE-X half-duplex capable. 0 = Not 100BASE-X half-duplex capable.	1
12:11	Reserved	RO	Ignore on read.	Undetermined
10	100BASE-T2 Full-duplex Capable	RO L	The BCM84891L is not capable of 100BASE-T2 full-duplex operation and returns 0 when this bit is read. 1 = 100BASE-T2 full-duplex capable. 0 = Not 100BASE-T2 full-duplex capable.	0
9	100BASE-T2 Half-duplex Capable	RO L	The BCM84891L is not capable of 100BASE-T2 half-duplex operation and returns 0 when this bit is read. 1 = 100BASE-T2 half-duplex capable. 0 = Not 100BASE-T2 half-duplex capable.	0
8	Extended Status	RO H	The BCM84891L contains IEEE Extended Status register at address 0Fh and returns 1 when this bit is read. 1 = Extended status information in register 0Fh. 0 = No extended status information in register 0Fh.	1
7	Reserved	RO	Ignore on read.	Undetermined
6	Management Frames Preamble Suppression	RO H	The BCM84891L accepts MII management frames whether or not they are preceded by the preamble pattern. **NOTE:** Preamble is still required on the first read or write. 1 = Preamble can be suppressed. 0 = Preamble always required.	1

Table 129: 1000BASE-T/100BASE-TX MII Status Register (7.0xFFE1) (Continued)

Bit	Name	R/W	Description	Default
5	Auto-negotiation Complete	RO	The BCM84891L returns 1 in this bit when auto-negotiation has completed and the contents of registers 4, 5, and 6 are valid. This bit returns 0 while auto-negotiation is in progress. 1 = Auto-negotiation complete. 0 = Auto-negotiation in progress.	0
4	Remote Fault	RO LH	The BCM84891L returns 1 in this bit when its link partner has signaled a remote fault condition. When a remote fault occurs, the bit is set and remains so until the remote fault condition has been cleared and the register is read. 1 = Remote fault detected. 0 = No remote fault detected.	0
3	Auto-negotiation Ability	RO H	Even if auto-negotiation has been disabled, the BCM84891L can perform IEEE auto-negotiation and returns 1 when this bit is read. 1 = Auto-negotiation capable. 0 = Not auto-negotiation capable.	1
2	Link Status	RO LL	The BCM84891L returns 1 in this bit when the link monitor is in the link pass state (indicating that a valid link has been established), otherwise it returns 0. When a link failure occurs, the Link Status bit is latched to 0 and remains so until the bit is read and the BCM84891L is in the link pass state. 1 = Link is up (Link Pass state). 0 = Link is down (Link Fail state).	0
1	Jabber Detect	RO LH	Jabber detection is performed within the PHY and the result is latched into this bit. When a jabber condition has been detected, the BCM84891L returns 1 in this bit. The bit is cleared with a read. 1 = Jabber condition detected. 0 = No jabber condition detected.	0
0	Extended Capability	RO H	The BCM84891L supports Extended Capability registers and returns 1 when this bit is read. 1 = Extended register capabilities. 0 = No extended register capabilities.	1

2.6.3 1000BASE-T/100BASE-TX PHY Identifier (DEVAD = 7, Address = 0xFFE2, Address = 0xFFE3)

The table below shows the result of concatenating these values to form the PHY identifiers for the BCM84891L.

Table 130: 1000BASE-T/100BASE-TX PHY ID Register (7.0xFFE2, 7.0xFFE3)

Bit	Name	R/W	Description	Default
15:0	Address 02: ID MSBs	RO	16 MSBs of PHY Identifier	0x3590
15:0	Address 03: ID LSBs	RO	16 LSBs of PHY Identifier	A0: 0x5080 B0: 0x5081

2.6.4 Copper Auto-Negotiation Advertisement (DEVAD = 7, Address = 0xFFE4)

Table 131: Copper Auto-Negotiation Advert. Register (7.0xFFE4)

Bit	Name	R/W	Description	Default
15	Next Page	R/W	1 = Next page ability supported. 0 = Next page ability not supported.	0
14	Reserved	R/W	Use read-modify-write to not change the current value during write. Ignore on read.	Undetermined
13	Remote Fault	R/W	1 = Advertise remote fault detected. 0 = Advertise no remote fault detected.	0
12	Reserved Technology	RO	Write as 0, ignore on read.	1
11	Asymmetric Pause	R/W	1 = Advertise asymmetric pause. 0 = Advertise no asymmetric pause.	0
10	Pause Capable	R/W	1 = Capable of full-duplex pause operation. 0 = Not capable of pause operation.	0
9	100BASE-T4 Capable	R/W	1 = 100BASE-T4 capable. 0 = Not 100BASE-T4 capable.	0
8	100BASE-TX Full-duplex Capable	R/W	1 = 100BASE-TX full-duplex capable. 0 = Not 100BASE-TX full-duplex capable.	Set by hardware
7	100BASE-TX Half-duplex Capable	R/W	1 = 100BASE-TX half-duplex capable. 0 = Not 100BASE-TX half-duplex capable.	Set by hardware
6:5	Reserved	R/W	Ignore on read.	Undetermined
4:0	Selector Field	R/W	00001 indicates IEEE 802.3 CSMA/CD.	00001

2.6.4.1 Next Page

Bit 15 of the 1000BASE-T/100BASE-TX Auto-negotiation Advertisement register must be set when the management software wants to control Next Page exchange. When this bit is cleared, Next Page exchange is controlled automatically by the BCM84891L. When this bit is cleared and the BCM84891L is not advertising 1000BASE-T capability, no Next Page exchange occurs.

2.6.4.2 Remote Fault

Setting bit 13 of the 1000BASE-T/100BASE-TX Auto-negotiation Advertisement register sends a remote fault indication to the link partner during auto-negotiation. Writing 0 to this bit clears the Remote Fault transmission bit. This bit returns 1 when advertising remote fault; otherwise, it returns 0.

2.6.4.3 Reserved Technology

Bit 12 of the 1000BASE-T/100BASE-TX/Auto-negotiation Advertisement register is reserved for future versions of the auto-negotiation standard, and must always be written as 1.

2.6.4.4 Asymmetric Pause

When bit 11 of the 1000BASE-T/100BASE-TX Auto-negotiation Advertisement register is set, the BCM84891L advertises that an asymmetric pause is preferred. When the bit is cleared, the BCM84891L advertises that asymmetric pause is not needed. This bit returns 1 when advertising an asymmetric pause, otherwise it returns 0. When advertising asymmetric pause, bit 10 of the 1000BASE-T/100BASE-TX Auto-negotiation Advertisement register indicates the preferred direction of the pause operation. Setting bit 10 indicates that the pause frames flow toward the BCM84891L. Clearing bit 10 indicates that pause frames flow toward the link partner.

2.6.4.5 Pause Capable

When bit 10 of the 1000BASE-T/100BASE-TX Auto-negotiation Advertisement register is set, the BCM84891L advertises full-duplex pause capability. When the bit is cleared, the BCM84891L advertises no pause capability. This bit returns 1, when advertising pause capability; otherwise, it returns 0.

2.6.4.6 100BASE-T4 Capable

The BCM84891L does not support 100BASE-T4 capability. Do not write 1 to bit 9 of the 1000BASE-T/100BASE-TX Auto-negotiation Advertisement register.

2.6.4.7 100BASE-TX Full-Duplex Capable

When bit 8 of the 1000BASE-T/100BASE-TX Auto-negotiation Advertisement register is set, the BCM84891L advertises 100BASE-TX full-duplex capability. When the bit is cleared, the BCM84891L advertises no 100BASE-TX full-duplex capability. This bit returns 1 when advertising 100BASE-TX full-duplex capability; otherwise, it returns 0.

2.6.4.8 100BASE-TX Half-Duplex Capable

When bit 7 of the 1000BASE-T/100BASE-TX Auto-negotiation Advertisement register is set, the BCM84891L advertises 100BASE-TX half-duplex capability. When the bit is cleared, the BCM84891L advertises no 100BASE-TX half-duplex capability. This bit returns 1 when advertising 100BASE-TX half-duplex capability; otherwise, it returns 0.

2.6.4.9 Selector Field

Bits [4:0] of the 1000BASE-T/100BASE-TX Auto-negotiation Advertisement register indicate the protocol type. The value 00001 indicates that the BCM84891L belongs to the IEEE 802.3 class of PHY transceivers.

2.6.5 Copper Auto-Negotiation Link Partner Ability (DEVAD = 7, Address = 0xFFE5)

Table 132: Copper Auto-Negotiation Link Partner Ability Register (7.0xFFE5)

Bit	Name	R/W	Description	Default
15	Next Page	RO	1 = Link partner has Next Page ability. 0 = Link partner does not have Next Page ability.	0
14	Acknowledge	RO	1 = Link partner has received link code word. 0 = Link partner has not received link code word.	0
13	Remote Fault	RO	1 = Link partner has detected remote fault. 0 = Link partner has not detected remote fault.	0

Table 132: Copper Auto-Negotiation Link Partner Ability Register (7.0xFFE5) (Continued) 15867339858

Bit	Name	R/W	Description	Default
12	Reserved Technology	RO	Write as 0, ignore during a read.	0
11	Asymmetric Pause	RO	1 = Link partner wants asymmetric pause. 0 = Link partner does not want asymmetric pause.	0
10	Pause Capable	RO	1 = Link partner is capable of pause operation. 0 = Link partner is not capable of pause operation.	0
9	100BASE-T4 Capable	RO	1 = Link partner is 100BASE-T4 capable. 0 = Link partner is not 100BASE-T4 capable.	0
8	100BASE-TX Full-duplex Capable	RO	1 = Link partner is 100BASE-TX full-duplex capable. 0 = Link partner is not 100BASE-TX full-duplex capable.	0
7	100BASE-TX Half-duplex Capable	RO	1 = Link partner is 100BASE-TX half-duplex capable. 0 = Link partner not 100BASE-TX half-duplex capable.	0
6:5	Reserved	RO	Ignore on read.	Undetermined
4:0	Protocol Selector Field	RO	Link partner protocol selector field.	00000

NOTE: As indicated by bit 5 of the 1000BASE-T/100BASE-TX MII Status register, the values contained in the 1000BASE-T/100BASE-TX Auto-negotiation Link Partner Ability register are only guaranteed to be valid after auto-negotiation has successfully completed.

2.6.5.1 Next Page

The BCM84891L returns 1 in bit 15 of the 1000BASE-T/100BASE-TX Link Partner Ability register when the link partner wants to transmit Next Page information.

2.6.5.2 Acknowledge

The BCM84891L returns 1 in bit 14 of the 1000BASE-T/100BASE-TX Link Partner Ability register when the link partner has acknowledged reception of the link code word; otherwise, it returns 0.

2.6.5.3 Remote Fault

The BCM84891L returns 1 in bit 13 of the 1000BASE-T/100BASE-TX Link Partner Ability register when the link partner has advertised detection of a remote fault; otherwise, it returns 0.

2.6.5.4 Reserved Technology

Bit 12 of the 1000BASE-T/100BASE-TX Link Partner Ability register is reserved for future versions of the auto-negotiation standard and must be ignored when read.

2.6.5.5 Asymmetric Pause

The BCM84891L returns 1 in bit 11 of the 1000BASE-T/100BASE-TX Link Partner Ability register when the link partner has advertised an asymmetric pause; otherwise, it returns 0.

2.6.5.6 Pause Capable

The BCM84891L returns 1 in bit 10 of the 1000BASE-T/100BASE-TX Link Partner Ability register when the link partner has advertised Pause Capability; otherwise, it returns 0.

2.6.5.7 100BASE-T4 Capable

The BCM84891L returns 1 in bit 9 of the 1000BASE-T/100BASE-TX Link Partner Ability register when the link partner has advertised 100BASE-T4 capability; otherwise, it returns 0.

2.6.5.8 100BASE-TX Full-Duplex Capable

The BCM84891L returns 1 in bit 8 of the 1000BASE-T/100BASE-TX Link Partner Ability register when the link partner has advertised 100BASE-TX full-duplex capability; otherwise, it returns 0.

2.6.5.9 100BASE-TX Half-Duplex Capable

The BCM84891L returns 1 in bit 7 of the 1000BASE-T/100BASE-TX Link Partner Ability register when the link partner has advertised 100BASE-TX half-duplex capability; otherwise, it returns 0.

2.6.5.10 Protocol Selector Field

Bits [4:0] of the 1000BASE-T/100BASE-TX Link Partner Ability register return the value of the link partner's advertised Protocol Selector field.

2.6.6 Copper Auto-Negotiation Expansion (DEVAD = 7, Address = 0xFFE6)

Table 133: Copper Auto-Negotiation Expansion Register (7.0xFFE6)

Bit	Name	R/W	Description	Default
15:5	Reserved	RO	Ignore on read.	Undetermined
4	Parallel Detection Fault	RO LH	When a parallel detection fault has occurred in the auto-negotiation state machine, this register returns 1. When a parallel detection fault occurs, this bit is latched at 1 and remains so until the register is read. If a parallel detection fault has not occurred since the last time it was read, this bit returns 0. 1 = Parallel link fault detected. 0 = Parallel link fault not detected.	0
3	Link Partner Next Page Ability	RO	The BCM84891L returns a 1 when the link partner must transmit Next Page information; otherwise, it returns 0. This bit is a copy of bit 15 in the 1000BASE-T/100BASE-TX Link Partner Ability register. 1 = Link partner has Next Page capability. 0 = Link partner does not have Next Page capability.	0
2	Next Page Capable	RO LH	When this bit is read, the BCM84891L supports Next Page capability and returns 1. 1 = BCM84891L is Next Page capable. 0 = BCM84891L is not Next Page capable.	1

Table 133: Copper Auto-Negotiation Expansion Register (7.0xFFE6) (Continued)

Bit	Name	R/W	Description	Default
1	Page Received	RO LH	The BCM84891L returns 1 when a new link code word has been received from the link partner since the last time this register was read; otherwise, it returns 0. 1 = New page has been received from link partner. 0 = New page has not been received.	0
0	Link Partner Auto-negotiation Ability	RO	When the link partner shows auto-negotiation capability, the BCM84891L returns 1. Before any auto-negotiation information is exchanged or if the link partner does not comply with IEEE auto-negotiation, the bit returns 0. 1 = Link partner has auto-negotiation capability. 0 = Link partner does not have auto-negotiation.	0

2.6.7 Copper Next Page Transmit (DEVAD = 7, Address = 0xFFE7)

Table 134: Copper Next Page Transmit Register (7.0xFFE7)

Bit	Name	R/W	Description	Default
15	Next Page	R/W	1 = Additional next pages follow. 0 = Sending last next page.	0
14	Reserved	RO	Ignore on read.	Undetermined
13	Message Page	R/W	1 = Formatted page. 0 = Unformatted page.	1
12	Acknowledge2	R/W	1 = Complies with message. 0 = Cannot comply with message.	0
11	Toggle	RO	Toggles between exchanges of different next pages.	0
10:0	Message/Unformatted Code Field	R/W	Next page message code or unformatted data.	001h

2.6.7.1 Next Page

Bit 15 of the 1000BASE-T/100BASE-TX Next Page Transmit register must be set to indicate that more Next Pages are to be sent. This bit must be cleared to indicate that this is the last Next Page to be transmitted. When this bit is read, it returns the last value written.

2.6.7.2 Message Page

Bit 13 of the 1000BASE-T/100BASE-TX Next Page Transmit register must be set to indicate that a formatted message page is being sent. This bit must be cleared to indicate that an unformatted page is being sent. When this bit is read, it returns the last value written.

2.6.7.3 Acknowledge2

When this bit is set, the BCM84891L indicates compliance with the Next Page request. When this bit is cleared, the BCM84891L indicates that it cannot comply with the Next Page request. When this bit is read, it returns the last value written.

NOTE: This bit is not used with 1000BASE-T next pages.

2.6.7.4 Toggle

This bit toggles between different Next Page exchanges to ensure a functional synchronization to the link partner.

2.6.7.5 Message/Unformatted Code Field

These 11 bits make up the message code defined by IEEE 802.3, Clause 28, Annex C, when sending formatted pages. When sending unformatted Next Pages, these 11 bits contain an arbitrary data value.

2.6.8 Copper Link Partner Received Next Page (DEVAD = 7, Address = 0xFFE8)

Table 135: Copper Link Partner Received Next Page Register (7.0xFFE8)

Bit	Name	R/W	Description	Default
15	Next Page	RO	When the link partner has indicated that more Next Pages are to be sent, this bit returns 1. This bit returns 0 when the link partner indicates that this is the last Next Page to be transmitted. 1 = Additional next pages follow. 0 = Sending last Next Page.	0
14	Acknowledge	RO	Returns 1 to indicate that the link partner has received and acknowledged a Next Page. Returns 0 until the link partner has acknowledged the page. 1 = Acknowledge. 0 = No acknowledge.	0
13	Message Page	RO	Returns 1 to indicate that the link partner has sent a formatted message page. This bit returns 0 when the link partner has sent an unformatted page. 1 = Formatted page. 0 = Unformatted page.	0
12	Acknowledge2	RO	When the link partner has indicated compliance with the Next Page request, this bit returns 1. When the link partner has indicated that it cannot comply with the Next Page request, this bit returns 0. 1 = Complies with message. 0 = Cannot comply with message. **NOTE:** This bit is not used with 1000BASE-T Next Pages.	0
11	Toggle	RO	To ensure a functional synchronization to the BCM84891L transceiver, the link partner toggles this bit between different Next Page exchanges.	0
10:0	Message Code field	RO	These bits make up the message code defined by IEEE 802.3, Clause 28, Annex C, when the link partner has sent a formatted page. When the link partner has sent unformatted next pages, these bits contain an arbitrary data value.	000h

2.6.9 1000BASE-T Control (DEVAD = 7, Address = 0xFFE9)

Table 136: 1000BASE-T Control Register (7.0xFFE9)

Bit	Name	R/W	Description	Default
15:13	Test Mode	R/W	These bits place the BCM84891L in one of four transmit test modes defined in IEEE 802.3ab. When read, these bits return the last value written. 1XX = Test mode 4: Transmitter distortion test. 011 = Test mode 3: Slave transmit jitter test. 010 = Test mode 2: Master transmit jitter test. 001 = Test mode 1: Transmit waveform test. 000 = Normal operation.	000
12	Master/Slave Configuration Enable	R/W	When set, master/slave mode is configured using the manual master/slave configuration value. When cleared, master/slave mode is configured using the automatic resolution function. This bit returns 1 when manual master/slave configuration is enabled; otherwise, it returns 0. 1 = Enable master/slave manual configuration value. 0 = Automatic master/slave configuration.	MANMS
11	Master/Slave Configuration Value	R/W	When set, bit 11 of the 1000BASE-T Control register determines the master/slave mode of operation and the BCM84891L is configured as the master. When cleared, the BCM84891L is configured as the slave. When read, this bit returns the last value written. 1 = Configure PHY as master. 0 = Configure PHY as slave.	HUB
10	Repeater/DTE	R/W	When set, the BCM84891L advertises that it is a repeater or switch device port. When cleared, the BCM84891L advertises that it is a DTE port. The advertised value is used in the automatic master/slave configuration resolution. The link partner, which advertises repeater mode, is configured to master if the opposing link partner advertises data terminal equipment (DTE); otherwise, this bit has no effect. This bit returns 1 when advertising repeater/switch mode; otherwise, it returns 0. 1 = Repeater/switch device port. 0 = DTE device.	HUB
9	Advertise 1000BASE-T Full-duplex Capability	R/W	When set, the BCM84891L advertises 1000BASE-T full-duplex capability. When cleared, the BCM84891L advertises no 1000BASE-T full-duplex capability. This bit returns 1 when advertising 1000BASE-T full-duplex capability; otherwise, it returns 0. 1 = Advertise 1000BASE-T full-duplex capability. 0 = Advertise no 1000BASE-T full-duplex capability.	AUTONEG-Speed (2)
8	Advertise 1000BASE-T Half-duplex Capability	R/W	When set, the BCM84891L advertises 1000BASE-T half-duplex capability. When cleared, the BCM84891L advertises no 1000BASE-T half-duplex capability. This bit returns 1 when advertising 1000BASE-T half-duplex capability; otherwise, it returns 0. 1 = Advertise 1000BASE-T half-duplex capability. 0 = Advertise no 1000BASE-T half-duplex capability.	ADV-HDX and AUTONEG-Speed(2)
7:0	Reserved	RO	Ignore on read.	Undetermined

2.6.10 1000BASE-T Status (DEVAD = 7, Address = 0xFFEA)

Table 137: 1000BASE-T Status Register (7.0xFFEA)

Bit	Name	R/W	Description	Default
15	Master/Slave Configuration Fault	RO LH	1 = Master/slave configuration fault detected. 0 = No master/slave configuration fault detected.	0
14	Master/Slave Configuration Resolution	RO	1 = Local transmitter is master. 0 = Local transmitter is slave.	0
13	Local Receiver Status	RO	1 = Local receiver OK. 0 = Local receiver not OK.	0
12	Remote Receiver Status	RO	1 = Remote receiver OK. 0 = Remote receiver not OK.	0
11	Link Partner 1000BASE-T Full-duplex Capability	RO	1 = Link partner is 1000BASE-T full-duplex capable. 0 = Link partner not 1000BASE-T full-duplex capable.	0
10	Link Partner 1000BASE-T Half-duplex Capability	RO	1 = Link partner is 1000BASE-T half-duplex capable. 0 = Link partner not 1000BASE-T half-duplex capable.	0
9:8	Reserved	RO	Ignore on read.	Undetermined
7:0	Idle Error Count	RO CR	The BCM84891L counts the number of idle errors received while the local receiver status is OK. These bits return the number of idle errors counted since the last register read. The counter freezes at the maximum value (FFh) to prevent overflow.	00h

NOTE: As indicated by bit 5 of the MII Status register, the values contained in bits 14, 11, and 10 of the 1000BASE-T Status register are guaranteed to be valid only after auto-negotiation has successfully completed.

2.6.10.1 Master/Slave Configuration Fault

When a master/slave configuration fault has occurred during auto-negotiation, the BCM84891L returns 1 in bit 15 of the 1000BASE-T Status register. When a configuration fault occurs, the bit is latched at 1 and remains so until either the register is read, auto-negotiation is restarted by writing bit 9 in the MII Control register, or auto-negotiation completes successfully with no master/slave configuration fault.

2.6.10.2 Master/Slave Configuration Resolution

When the BCM84891L transceiver has been configured as the master, it returns 1 in bit 14 of the 1000BASE-T Status register. When the BCM84891L transceiver has been configured as the slave, it returns 0.

2.6.10.3 Local Receiver Status

The BCM84891L transceiver returns 1 in bit 13 of the 1000BASE-T Status register when the local receiver status is OK; otherwise, it returns 0.

2.6.10.4 Remote Receiver Status

The BCM84891L returns 1 in bit 12 of the 1000BASE-T Status register when the remote receiver status is OK; otherwise, it returns 0.

2.6.10.5 1000BASE-T Full-Duplex Capability

The BCM84891L returns 1 in bit 11 of the 1000BASE-T Status register when the link partner has advertised 1000BASE-T full-duplex capability; otherwise, it returns 0.

2.6.10.6 1000BASE-T Half-Duplex Capability

The BCM84891L returns 1 in bit 10 of the 1000BASE-T Status register when the link partner has advertised 1000BASE-T half-duplex capability; otherwise, it returns 0.

2.6.11 1000BASE-T/100BASE-TX IEEE Extended Status (DEVAD = 7, Address = 0xFFEF)

Table 138: 1000BASE-T/100BASE-TX IEEE Extended Status Register (7.0xFFEF)

Bit	Name	R/W	Description	Default
15	1000BASE-X Full-duplex Capable	RO L	1 = 1000BASE-X full-duplex capable. 0 = Not 1000BASE-X full-duplex capable.	0
14	1000BASE-X Half-duplex Capable	RO L	1 = 1000BASE-X half-duplex capable. 0 = Not 1000BASE-X half-duplex capable.	0
13	1000BASE-T Full-duplex Capable	RO H	1 = 1000BASE-T full-duplex capable. 0 = Not 1000BASE-T full-duplex capable.	1
12	1000BASE-T Half-duplex Capable	RO H	1 = 1000BASE-T half-duplex capable. 0 = Not 1000BASE-T half-duplex capable.	1
11:0	Reserved	RO	Ignore on read.	Undetermined

2.6.11.1 1000BASE-X Full-Duplex Capable

The BCM84891L is not capable of 1000BASE-X full-duplex operation and returns 0 when bit 15 of the 1000BASE-T/100BASE-TX IEEE Extended Status register is read.

2.6.11.2 1000BASE-X Half-Duplex Capable

The BCM84891L is not capable of 1000BASE-X half-duplex operation and returns 0 when bit 14 of the 1000BASE-T/100BASE-TX IEEE Extended Status register is read.

2.6.11.3 1000BASE-T Full-Duplex Capable

The BCM84891L is capable of 1000BASE-T full-duplex operation and returns 1 when bit 13 of the 1000BASE-T/100BASE-TX IEEE Extended Status register is read.

2.6.11.4 1000BASE-T Half-Duplex Capable

The BCM84891L is capable of 1000BASE-T half-duplex operation and returns 1 when bit 12 of the 1000BASE-T/100BASE-TX IEEE Extended Status register is read.

2.6.12 1000BASE-T/100BASE-TX PHY Extended Control (DEVAD = 7, Address = 0xFFF0)

Table 139: 1000BASE-T/100BASE-TX PHY Extended Control Register (7.0xFFF0)

Bit	Name	R/W	Description	Default
15	Reserved	R/W	Use read-modify-write to not change the current value during write. Ignore on read.	Undetermined
14	Disable Automatic MDI Crossover	R/W	1 = Automatic MDI crossover disabled. 0 = Automatic MDI crossover enabled.	0
13	Transmit Disable	R/W	1 = Transmitter outputs disabled. 0 = Normal operation.	0
12	Reserved	R/W	Use read-modify-write to not change the current value during write. Ignore on read.	Undetermined
11	Reserved	R/W	Use read-modify-write to not change the current value during write. Ignore on read.	Undetermined
10	Bypass 4B/5B Encoder/ Decoder (100BASE-TX)	R/W	1 = Transmit and receive 5B codes over MII pins. 0 = Normal MII.	0
9	Bypass Scrambler/ Descrambler (100BASE-TX)	R/W	1 = Scrambler and descrambler disabled. 0 = scrambler and descrambler enabled.	0
8	Bypass MLT3 Encoder/ Decoder (100BASE-TX)	R/W	1 = Bypass NRZI/MLT3 encoder and decoder. 0 = Normal operation.	0
7	Bypass Receive Symbol Alignment (100BASE-TX)	R/W	1 = 5B receive symbols not aligned. 0 = Receive symbols aligned to 5B boundaries.	0
6	Reset Scrambler (100BASE-TX)	R/W SC	1 = Reset scrambler to initial state. 0 = Normal scrambler operation.	0
5	Enable LED Traffic Mode	R/W	1 = LED Traffic mode enabled. 0 = LED Traffic mode disabled.	0
4	Force LEDs On	R/W	1 = Force all LEDs into On state. 0 = Normal LED operation.	0
3	Force LEDs Off	R/W	1 = Force all LEDs into Off state. 0 = Normal LED operation.	0
2:1	Reserved	R/W	Use read-modify-write to not change the current value during write. Ignore on read.	Undetermined
0	1000BASE-T Transmit FIFO Elasticity (copper mode) [LSB]	R/W‘	FIFO ELASTICITY [MSB:LSB]: 11 = Supports 18 KB packets. 10 = Supports 13.5 KB packets. 01 = Supports 4.5 to 9 KB packets. 00 = Supports 4.5 KB packets. MSB located at Expansion Register 46, bit 14.	Set by firmware

2.6.12.1 Disable Automatic MDI Crossover

The automatic MDI crossover function can be disabled by setting bit 14 of the 1000BASE-T/100BASE-TX PHY Extended Control register. When the bit is cleared, the BCM84891L performs the automatic MDI crossover function (see Section 1.7.14, Automatic MDI Crossover, for details).

2.6.12.2 Transmit Disable

The transmitter can be disabled by setting bit 13 of the 1000BASE-T/100BASE-TX PHY Extended Control register. The transmitter outputs (TRD± [3:0]) are forced into a high-impedance state.

2.6.12.3 Bypass 4B/5B Encoder/Decoder (100BASE-TX)

The 100BASE-TX4B/5B encoder/decoder can be bypassed by setting bit 10 of the 1000BASE-T/100BASE-TX PHY Extended Control register. The transmitter sends 5B codes from the TX_ER and TXD[3:0] pins directly to the scrambler. TX_EN is ignored and frame encapsulation (insertion of J/K and T/R codes) is not performed. The receiver places descrambled and aligned 5B codes onto the RX_ER and RXD[3:0] pins.

2.6.12.4 Bypass Scrambler/Descrambler (100BASE-TX)

The 100BASE-TX stream cipher function can be disabled by setting bit 9 of the 1000BASE-T/100BASE-TX PHY Extended Control register. The stream cipher function can be reenabled by writing 0 to this bit.

2.6.12.5 Bypass MLT3 Encoder/Decoder (100BASE-TX)

The 100BASE-TX MLT3 encoder and decoder can be bypassed by setting bit 8 of the 1000BASE-T/100BASE-TX PHY Extended Control register. NRZ data is transmitted and received on the cable. The MLT3 encoder can be reenabled by clearing this bit.

2.6.12.6 Bypass Receive Symbol Alignment (100BASE-TX)

The 100BASE-TX receive symbol alignment can be bypassed by setting bit 7 of the 1000BASE-T/100BASE-TX PHY Extended Control register. When used in conjunction with the bypass 4B/5B encoder/decoder bit, unaligned 5B codes are placed directly on the RX_ER and RXD[3:0] pins.

2.6.12.7 Reset Scrambler (100BASE-TX)

When bit 6 of the 1000BASE-T/100BASE-TX PHY Extended Control register is set, the BCM84891L resets the scrambler to an all 1’s. This bit is self-clearing and always returns 0 when read.

2.6.12.8 Enable LED Traffic Mode

When bit 5 of the 1000BASE-T/100BASE-TX PHY Extended Control register is set, the BCM84891L enables the LED traffic mode for activity, $\overline{\text{ACTIVITYLED}}$ and $\overline{\text{XMITLED}}$. When the bit is cleared, the BCM84891L disables the LED traffic mode.

2.6.12.9 Force LEDs On

When bit 4 of the 1000BASE-T/100BASE-TX PHY Extended Control register is set, the BCM84891L forces all LEDs into the on state. When the bit is cleared, the BCM84891L resets all LEDs to normal operation.

2.6.12.10 Force LEDs Off

When bit 3 of the 1000BASE-T/100BASE-TX PHY Extended Control register is set, the BCM84891L forces all LEDs into the off state. When the bit is cleared, the BCM84891L resets all LEDs to normal operation.

2.6.13 1000BASE-T/100BASE-TX PHY Extended Status (DEVAD = 7, Address = 0xFFF1)

Table 140: 1000BASE-T/100BASE-TX PHY Extended Status Register (7.0xFFF1)

Bit	Name	R/W	Description	Default
15	Auto-negotiation BASE Page Selector Field Mismatch	RO LH	1 = Link partner base page selector field mismatched advertised selector field since last read. 0 = No mismatch detected since last read.	0
14	Ethernet@Wirespeed™ Downgrade	RO	1 = Auto-negotiation advertised speed downgraded. 0 = No advertised speed downgrade.	0
13	MDI Crossover State	RO	1 = Crossover MDI mode. 0 = Normal MDI mode.	0
12	Reserved	R/W	Use read-modify-write to not change the current value during write. Ignore on read.	Undetermined
11	Remote Receiver Status	RO LL	1 = Remote receiver OK. 0 = Remote receiver not OK since last read.	0
10	Local Receiver Status	RO LL	1 = Local receiver OK. 0 = Local receiver not OK since last read.	0
9	Locked	RO	1 = Descrambler locked. 0 = Descrambler unlocked.	0
8	Link Status	RO	1 = Link pass. 0 = Link fail.	0
7	CRC Error Detected	RO LL	1 = CRC error detected. 0 = No CRC error since last read.	0
6	Carrier Extension Error Detected	RO LH	1 = Carrier extension error detected since last read. 0 = No carrier extension error since last read.	0
5	Bad SSD Detected (False Carrier)	RO LH	1 = Bad SSD error detected since last read. 0 = No bad SSD error since last read.	0
4	Bad ESD Detected (Premature End)	RO LH	1 = Bad ESD error detected since last read. 0 = No bad ESD error since last read.	0
3	Receive Error Detected	RO LH	1 = Receive error detected since last read. 0 = No receive error since last read.	0
2	Transmit Error Detected	RO LH	1 = Transmit error code received since last read. 0 = No transmit error code received since last read.	0
1	Lock Error Detected	RO LH	1 = Lock error detected since last read. 0 = No lock error since last read.	0
0	MLT3 Code Error Detected	RO LH	1 = MLT3 code error detected since last read. 0 = No MLT3 code error since last read.	0

2.6.13.1 Auto-Negotiation BASE Page Selector Field Mismatch

When this bit is set, the auto-negotiation base page selector does not match the Advertised Selector field since the previous read. When this bit reads back 0, there is no mismatched Page Selector field and Advertised Selector field.

2.6.13.2 Ethernet@Wirespeed Downgrade

The BCM84891L returns 1 in bit 14 when an Ethernet@Wirespeed downgrade has occurred.

2.6.13.3 MDI Crossover State

When the BCM84891L is automatically switching the transmit and receive pairs to communicate with a remote device, the BCM84891L returns 1 in bit 13 of the 1000BASE-T/100BASE-TX PHY Extended Status register. This bit returns 0 when the BCM84891L is in normal MDI mode.

2.6.13.4 Remote Receiver Status

When the remote receiver status is OK, the BCM84891L returns 1 in bit 11 of the 1000BASE-T/100BASE-TX PHY Extended Status register. When the BCM84891L detects that the remote receiver is not OK, this bit is latched at 0 and remains so until the bit is read and the remote receiver status is OK.

2.6.13.5 Local Receiver Status

When the local receiver status is OK, the BCM84891L returns 1 in bit 10 of the 1000BASE-T/100BASE-TX PHY Extended Status register. When the BCM84891L detects that the local receiver is not OK, this bit is latched at 0 and remains so until the bit is read and the remote receiver status is OK.

2.6.13.6 Locked

The BCM84891L returns 1 in bit 9 of the 1000BASE-T/100BASE-TX PHY Extended Status register when the descrambler is locked to the incoming data stream; otherwise, it returns 0.

2.6.13.7 Link Status

The BCM84891L returns 1 in bit 8 of the 1000BASE-T/100BASE-TX PHY Extended Status register when the device has established a link; otherwise, it returns 0.

2.6.13.8 CRC Error Detected

The BCM84891L **retur**ns 1 in bit 7 of the 1000BASE-T/100BASE-TX PHY Extended Status register if a CRC error has been detected since the last time this register was read; otherwise, it returns 0.

2.6.13.9 Carrier Extension Error Detected

The BCM84891L returns 1 in bit 6 of the 1000BASE-T/100BASE-TX PHY Extended Status register if a carrier extension error has been detected since the last time this register was read; otherwise, it returns 0.

2.6.13.10 Bad SSD Detected (False Carrier)

The BCM84891L returns 1 in bit 5 of the 1000BASE-T/100BASE-TX PHY Extended Status register if a bad start-of-stream error has been detected since the last time this register was read; otherwise, it returns 0.

2.6.13.11 Bad ESD Detected (Premature End)

The BCM84891L returns 1 in bit 4 of the 1000BASE-T/100BASE-TX PHY Extended Status register if a bad end-of-stream error has been detected since the last time this register was read; otherwise, it returns 0.

2.6.13.12 Receive Error Detected

The BCM84891L returns 1 in bit 3 of the 1000BASE-T/100BASE-TX PHY Extended Status register if a packet was received with an invalid code since the last time this register was read; otherwise, it returns 0.

2.6.13.13 Transmit Error Detected

The BCM84891L returns 1 in bit 2 of the 1000BASE-T/100BASE-TX PHY Extended Status register if a packet was received with a transmit error code since the last time this register was read; otherwise, it returns 0.

2.6.13.14 Lock Error Detected

The BCM84891L returns 1 in bit 1 of the 1000BASE-T/100BASE-TX PHY Extended Status register if the descrambler has lost lock since the last time this register was read; otherwise, it returns 0.

2.6.13.15 MLT3 Code Error Detected

The BCM84891L returns 1 in bit 0 of the 1000BASE-T/100BASE-TX PHY Extended Status register if an MLT3 coding error has been detected in the receive data stream since the last time this register was read; otherwise, it returns 0.

2.6.14 1000BASE-T/100BASE-TX Receive Error Counter (DEVAD = 7, Address = 0xFFF2)

Table 141: 1000BASE-T/100BASE-TX Receive Error Counter Register (7.0xFFF2)[a]

Bit	Name	R/W	Description	Default
15:0	Receive Error Counter	R/W CR	Number of non-collision packets with receive errors since last read.	0000h

a. Bits 15:0 of this register becomes the SerDes CRC error counter when register 1Ch, shadow 11011, bit 9 is set.

2.6.14.1 Receive Error Counter

This counter increments each time the BCM84891L receives a non collision packet containing at least 1 receive error. This counter freezes at the maximum value of FFFFh. The counter automatically clears when read.

2.6.15 1000BASE-T/100BASE-TX False Carrier Sense Counter (DEVAD = 7, Address = 0xFFF3)

Table 142: 1000BASE-T/100BASE-TX False Carrier Sense Counter (7.0xFFF3)[a]

Bit	Name	R/W	Description	Default
15:8	Reserved	R/W	Use read-modify-write to not change the current value during write. Ignore on read.	Undetermined
7:0	False Carrier Sense Counter	R/W CR	Number of false carrier sense events since last read.	00h

a. Bits 15:0 of this register becomes the SerDes data bit when register 1Ch, shadow 11011, bit 9 is set.

2.6.15.1 False Carrier Sense Counter

The False Carrier Sense Counter increments each time the BCM84891L detects a false carrier sense on the receive input. This counter freezes at the maximum value of FFh. The counter automatically clears when read.

2.6.16 1000BASE-T/100BASE-TX Receiver NOT_OK Counter (DEVAD = 7, Address = FFF4h)

Table 143: 1000BASE-T/100BASE-TX Receiver NOT_OK Counter Register (7.FFF4h)[a]

Bit	Name	R/W	Description	Default
15:8	Local Receiver NOT_OK Counter	R/W CR	Number of times local receiver was NOT_OK since last read.	00h
7:0	Remote Receiver NOT_OK Counter	R/W CR	Number of times BCM84891L detected that the remote receiver was NOT_OK since last read.	00h

a. Bits 15:0 of this register become the CRC error bits when register 1Eh bit 15 is set. Bits 15:0 of this register becomes the SerDes data bit when register 1Ch, shadow 11011, bit 9 is set.

2.6.16.1 Local Receiver NOT_OK Counter

This counter increments each time the local receiver enters the NOT_OK state. This counter freezes at the maximum value of FFh. The counter automatically clears when read.

2.6.16.2 Remote Receiver NOT_OK Counter

This counter increments each time the remote receiver enters the NOT_OK state. This counter freezes at the maximum value of FFh. The counter automatically clears when read.

2.6.17 1000BASE-T/100BASE-TX Expansion Register Access (DEVAD = 7, Address = 0xFFF7)

Table 144: 1000BASE-T/100BASE-TX Expansion and 1000BASE-X Access Register (7.0xFFF7)

Bit	Name	R/W	Description	Default
15:12	Reserved	R/W	Use read-modify-write to not change the current value during write. Ignore on read.	Undetermined
11:8	Expansion and 1000BASE-X Register Select	R/W	Setting these bits to 1111 enable reading from and writing to the Expansion registers through register 15h (FFF5h). These bits should be cleared after the Expansion registers are accessed or when the Expansion registers are not being accessed. 1111 = Expansion register selected. 1110 = 1000BASE-X selected. 0000 = Expansion register not selected. All others = Reserved (do not use).	0h
7:0	Expansion and 1000BASE-X Register Accessed	R/W	Sets the Expansion register number accessed when read/write to register 15h.	00h

2.6.17.1 Expansion Register Accessed

Bits [7:0] of the Expansion Register Access register set the Expansion register number accessed. The Expansion register is read/write through register 15h (FFF5h) when bits [11:8] of this register are set to 1111. The available expansion registers are listed in the table below.

Table 145: Expansion Register Select Values

Expansion Register	Register Name
00h	Expansion Register 00h: Receive/Transmit Packet Counter

2.6.18 1000BASE-T/100BASE-TX Auxiliary Control Shadow Value Access Register (DEVAD = 7, Address = FFF8h)

The table below lists the available 18h registers.

Table 146: 1000BASE-T/100BASE-TX Auxiliary Control Shadow Values Access (7.FFF8h)

Shadow Value	Register Name
000	1000BASE-T/100BASE-TX Auxiliary Control Register (7.0xFFF8)
001	Reserved
010	1000BASE-T/100BASE-TX Power/MII Control Register (7.0xFFF8)
100	1000BASE-T/100BASE-TX Misc. Test Register (7.0xFFF8)
111	1000BASE-T/100BASE-TX Misc. Control Register (7.0xFFF8)

The table below shows the read from register 18h, shadow value zzz.

Table 147: Reading Register 0xFFF8

Register Reads/Writes	Description
Write register 18h (FFF8h), bits [2:0] = 111	This selects the Misc. Control register, shadow value 111. All reads must be done through the Misc. Control register.
Bit [15] = 0	This allows only bits [14:12] and [2:1] to be written.
Bits [14:12] = zzz	This selects shadow value register zzz to be read.
Bits [11:3] = <don't care>	When bit [15] = 0, these bits are ignored.
Bits [2:0] = 111	This sets the Shadow Register Select to 111 (Misc. Control register).
Read register 18h	Data read back is the value from shadow register zzz.

The table below shows the write to register 0xFFF8, shadow value yyy.

Table 148: Writing Register 0xFFF8

Register Writes	Description
Set Bits [15:3] = Preferred write values	Bits [15:3] contain the preferred bits to be written to.
Set Bits [2:0] = yyy	This enables shadow value register yyy to be written. For shadow value 111, bit 15 must also be written.

2.6.19 1000BASE-T/100BASE-TX Auxiliary Control (DEVAD = 7, Address = 0xFFF8, Shadow Value 000b)

Table 149: 1000BASE-T/100BASE-TX Auxiliary Control Register (7.0xFFF8)

Bit	Name	R/W	Description	Default
15	External Loopback	R/W	When set, external loopback operation is enabled. When cleared, normal operation resumes. 1 = External Loopback enabled. 0 = Normal operation.	0
14	Extended Packet Length	R/W	When set, the BCM84891L receives packets up to 18 KB in length. When cleared, the BCM84891L only receives packets up to 4.5 KB in length. 1 = Allow reception of extended length packets. 0 = Allow normal length Ethernet packets only.	1
13:12	Edge Rate Control (1000BASE-T)	R/W	Controls the edge rate of the 1000BASE-T transmit DAC output waveform. 00 = 4.0 ns 01 = 5.0 ns 10 = 3.0 ns 11 = 0.0 ns **NOTE:** The ER pin status is not reflected in the register 0xFFF8 shadow 000.	00
11	Reserved	R/W	Use read-modify-write to not change the current value during write. Ignore on read.	Undetermined
10	Transmit Mode	R/W	This bit must be set for normal PHY operation. 1 = Normal operation. 0 = Test mode.	1
9:8	Reserved	R/W	Use read-modify-write to not change the current value during write. Ignore on read.	Undetermined
7	Disable Partial Response Filter	R/W	When set, the transmitter partial response filter is disabled. When cleared, the transmitter partial response filter is enabled. 1 = Transmitter partial response filter disabled. 0 = Transmitter partial response filter enabled.	0
6	Reserved	R/W	Use read-modify-write to not change the current value during write. Ignore on read.	Undetermined
5:4	Edge-Rate Control (100BASE-TX)	R/W	Controls the edge rate of the 100BASE-TX transmit DAC output waveform. 00 = 4.0 ns 01 = 5.0 ns 10 = 3.0 ns 11 = 0.0 ns **NOTE:** The ER pin status is not reflected in Register 0xFFF8, shadow 000.	00
3	Reserved	R/W	Use read-modify-write to not change the current value during write. Ignore on read.	Undetermined

Table 149: 1000BASE-T/100BASE-TX Auxiliary Control Register (7.0xFFF8) (Continued)

Bit	Name	R/W	Description	Default
2:0	Shadow Register Select	R/W	The Auxiliary Control register provides access to eight registers using a shadow technique. The lower 3 bits written define which set of 13 upper bits are used in accordance with Table 146, defined under bits [2:0]. See the note in Section 2.6.18, 1000BASE-T/100BASE-TX Auxiliary Control Shadow Value Access Register (DEVAD = 7, Address = FFF8h), describing reading/ writing register 0xFFF8. The register set previously shown is for Auxiliary Control operation, obtained when the lower 3 bits are 000. 000 = Auxiliary Control register. 001 = Reserved. 010 = Power/MII Control register. 011 = Reserved. 100 = Misc. Test register. 101 = Reserved. 110 = Reserved. 111 = Misc. Control register.	000

2.6.20 1000BASE-T/100BASE-TX Power/MII Control (DEVAD = 7, Address = 0xFFF8, Shadow Value 010b)

Table 150: 1000BASE-T/100BASE-TX Power/MII Control Register (7.0xFFF8)

Bit	Name	R/W	Description	Default
15:7	Reserved	R/W	Use read-modify-write to not change the current value during write. Ignore on read.	Undetermined
6	Reserved	R/W	Use read-modify-write to not change the current value during write. Ignore on read.	Undetermined
5	Reserved	R/W	Use read-modify-write to not change the current value during write. Ignore on read.	Undetermined
4:3	Reserved	R/W	Use read-modify-write to not change the current value during write. Ignore on read.	Undetermined

Table 150: 1000BASE-T/100BASE-TX Power/MII Control Register (7.0xFFF8) (Continued)

Bit	Name	R/W	Description	Default
2:0	Shadow Register Select	R/W	The 1000BASE-T/100BASE-TX Auxiliary Control register provides access to eight registers using a shadow technique. The lower 3 bits written define the set of 13 upper bits used in accordance with the table defined under bits [2:0]. See the note in 1000BASE-T/100BASE-TX Auxiliary Control Shadow Value Access Register (DEVAD = 7, Address = FFF8h) describing reading from and writing to register 18h. The register set previously shown is for power/MII control, obtained when the lower 3 bits are 010. 000 = Auxiliary Control register. 001 = Reserved. 010 = Power/MII Control register. 011 = Reserved. 100 = Misc. Test register. 101 = Reserved. 110 = Reserved. 111 = Misc. Control register.	010

2.6.21 1000BASE-T/100BASE-TX Misc. Test Register R (DEVAD = 7, Address = 0xFFF8, Shadow Value 100b)

Table 151: 1000BASE-T/100BASE-TX Misc. Test Register (7.0xFFF8)

Bit	Name	R/W	Description	Default
15	Line-side (Remote) Loopback Enable	R/W	Enables line-side (remote) loopback of the copper receive packet back out through the MDI transmit path. 1 = Enable line-side (remote) loopback from MDI (cable end) receive packet, through PCS, and back to the MDI transmit packet. 0 = Disable loopback.	0
14:12	Reserved	R/W	Use read-modify-write to not change the current value during write. Ignore on read.	Undetermined
11	Reserved	R/W	Use read-modify-write to not change the current value during write. Ignore on read.	Undetermined
10:5	Reserved	R/W	Use read-modify-write to not change the current value during write. Ignore on read.	Undetermined
4	Swap RX MDIX	R/W	When set to 1, the transmitter and receiver operate on the same twisted-pair. This function is for use in test modes where the transmitter output is detected by the receiver attached to the same pair. 1 = RX and TX operate on same pair. 0 = Normal operation.	0
3	Reserved	R/W	Use read-modify-write to not change the current value during write. Ignore on read.	Undetermined

Table 151: 1000BASE-T/100BASE-TX Misc. Test Register (7.0xFFF8) (Continued)

Bit	Name	R/W	Description	Default
2:0	Shadow Register Select	R/W	The Misc. Test register provides access to 8 registers using a shadow technique. The lower 3 bits written define the set of 13 upper bits used in accordance with Table 149 under bits [2:0]. See the note on 1000BASE-T/100BASE-TX Auxiliary Control Shadow Value Access Register (DEVAD = 7, Address = FFF8h), describing reading from and writing to register 0xFFF8. The register set previously shown is for miscellaneous testing, obtained when the lower 3 bits are 100. 000 = Auxiliary Control register. 001 = Reserved. 010 = Power/MII Control register. 011 = Reserved. 100 = Misc. Test register. 101 = Reserved. 110 = Reserved. 111 = Misc. Control register.	100

2.6.22 1000BASE-T/100BASE-TX Misc. Control (DEVAD = 7, Address = 0xFFF8, Shadow Value 111b)

Table 152: 1000BASE-T/100BASE-TX Misc. Control Register (7.0xFFF8)

Bit	Name	R/W	Description	Default
15	Write Enable (Bits 11:3)	R/W SC	1 = Write bits [14:0]. 0 = Only write bits [14:12] and [2:0].	0
14:12	Shadow Register Read Selector	R/W	000 = Normal operation. 001 = Reserved. 010 = Power Control register. 011 = Reserved. 100 = Misc. Test register. 101 = Reserved. 110 = Reserved. 111 = Misc. Control register. These bits are written when bit 15 is not set. This sets the shadow value for address 18h register read.	000
11	Packet Counter Mode	R/W	1 = Receive packet counter. 0 = Transmit packet counter.	0
10	Reserved	R/W	Use read-modify-write to not change the current value during write. Ignore on read.	Undetermined
9	Force Auto-MDIX Mode	R/W	1 = Auto-MDIX is enabled when auto-negotiation is disabled. 0 = Auto-MDIX is disabled when auto-negotiation is disabled.	0
8	Reserved	R/W	Use read-modify-write to not change the current value during write. Ignore on read.	Undetermined
7	Reserved	R/W	Use read-modify-write to not change the current value during write. Ignore on read.	Undetermined

Table 152: 1000BASE-T/100BASE-TX Misc. Control Register (7.0xFFF8) (Continued)

Bit	Name	R/W	Description	Default
6	Reserved	R/W	Use read-modify-write to not change the current value during write. Ignore on read.	Undetermined
5	Reserved	R/W	Use read-modify-write to not change the current value during write. Ignore on read.	Undetermined
4	Ethernet@Wirespeed Enable	R/W	1 = Enable Ethernet@Wirespeed. 0 = Disable Ethernet@Wirespeed.	Wirespeed
3	Reserved	R/W	Use read-modify-write to not change the current value during write. Ignore on read.	Undetermined
2:0	Shadow Register Select	R/W	000 = Auxiliary register. 001 = Reserved. 010 = Power Control register. 011 = Reserved. 100 = Misc. Test register. 101 = Reserved. 110 = Reserved. 111 = Misc. Control register.	111

2.6.22.1 Write Enable (Bits 11:3)

If bit 15 of the 1000BASE-T/100BASE-TX Misc. Control register is set when writing to this register, bits [11:3] of this register can be modified. Bits [2:0] and [14:12] can always be written regardless of the state of bit 15. When this bit is set, bits [11:3] are written. When this bit is cleared, only bits [14:12] and [2:0] are written.

2.6.22.2 Shadow Register Read Selector

Bits [14:12] of the 1000BASE-T/100BASE-TX Misc. Control register are written, regardless of the value of bit 15. These bits determine the shadow value for an MII register 18h read operation. See the note in 1000BASE-T/100BASE-TX Auxiliary Control Shadow Value Access Register (DEVAD = 7, Address = FFF8h), describing reading from and writing to register 18h.

2.6.22.3 Packet Counter Mode

Bit 11 of the 1000BASE-T/100BASE-TX Misc. Control register sets the packet counter mode in Expansion register 00h. The counter counts the receive packet when this bit is set; otherwise, it counts the transmit packet.

2.6.22.4 Force Auto-MDIX Mode

Bit 9 of the 1000BASE-T/100BASE-TX Misc. Control register enable the auto-MDIX mode while auto-negotiation is disabled. The default setting disables the auto-MDIX function when auto-negotiation is disabled.

2.6.22.5 Ethernet@Wirespeed Enable

When bit 4 = 1, Ethernet@Wirespeed mode is enabled. If the link cannot be established within two to nine attempts (the number of attempts is set by bits[4:2] in register 1Ch, shadow value 00100), the BCM84891L downgrades its advertised abilities and again tries to establish a link. When bit 4 is cleared, it advertises its abilities according to registers 04h and 09h.

2.6.22.6 Shadow Register Select

Using a shadow technique, the 1000BASE-T/100BASE-TX Misc. Control register provides access to 8 registers. The lower 3 bits written define which set of 13 upper bits are used in accordance with Table 152, defined under bits 2:0.

See the note about the 1000BASE-T/100BASE-TX Auxiliary Control Shadow Value Access Register (DEVAD = 7, Address = FFF8h), describing reading from and writing to register 18h. The register set previously shown is for miscellaneous control, obtained when the lower 3 bits are 111.

2.6.23 1000BASE-T/100BASE-TX Auxiliary Status Summary (DEVAD = 7, Address = 0xFFF9)

Table 153: 1000BASE-T/100BASE-TX Auxiliary Status Summary Register (7.0xFFF9)

Bit	Name	R/W	Description	Default
15	Auto-negotiation Complete	RO	1 = Auto-negotiation complete. 0 = Auto-negotiation in progress.	0
14	Auto-negotiation Complete Acknowledge	RO LH	1 = Entered auto-negotiation link good check state. 0 = State not entered since last read.	0
13	Auto-negotiation Acknowledge Detect	RO LH	1 = Entered auto-negotiation acknowledge detect state. 0 = State not entered since last read.	0
12	Auto-negotiation Ability Detect	RO LH	1 = Entered auto-negotiation ability detect state. 0 = State not entered since last read.	0
11	Auto-negotiation Next Page Wait	RO LH	1 = Entered auto-negotiation Next Page wait state. 0 = State not entered since last read.	0
10:8	Auto-negotiation HCD (Current Operating Speed and Duplex Mode)	RO	111 = 1000BASE-T full-duplex[a]. 110 = 1000BASE-T half-duplex[a]. 101 = 100BASE-TX full-duplex[a]. 100 = 100BASE-T4. 011 = 100BASE-TX half-duplex[a]. 010 = Reserved. 001 = Reserved. 000 = No highest common denominator or auto-negotiation is not complete. When the auto-negotiation function has been disabled, bits[10:8] report the manually selected mode of operation when Register 18h, shadow value 111, bit 9 = 0. If auto-negotiation is disabled and Register 18h, shadow value 111, bit 9 = 1, bits [10:8] = 000.	000
7	Parallel Detection Fault	RO LH	1 = Parallel link fault is detected. 0 = Parallel link fault is not detected.	0
6	Remote Fault	RO	1 = Link partner has detected remote fault. 0 = Link partner has not detected remote fault.	0
5	Auto-negotiation Page Received	RO LH	1 = New page has been received from link partner. 0 = New page has not been received.	0
4	Link Partner Auto-negotiation Ability	RO	1 = Link partner has auto-negotiation capability. 0 = Link partner does not perform auto-negotiation.	0

Table 153: 1000BASE-T/100BASE-TX Auxiliary Status Summary Register (7.0xFFF9) (Continued)

Bit	Name	R/W	Description	Default
3	Link Partner Next Page Ability	RO	1 = Link partner has Next Page capability. 0 = Link partner does not have Next Page capability.	0
2	Link Status	RO	1 = Link is up (link pass state). 0 = Link is down (link fail state).	0
1	Pause Resolution, Receive Direction	RO	1 = Enable pause receive. 0 = Disable pause receive.	0
0	Pause Resolution, Transmit Direction	RO	1 = Enable pause transmit. 0 = Disable pause transmit.	0

a. Indicates the negotiated HCD when auto-negotiation enable = 1, or indicates the manually selected speed and duplex mode when auto-negotiation enable = 0.

2.6.23.1 Auto-Negotiation Complete

When auto-negotiation is complete, the BCM84891L returns 1 in bit 15 of the 1000BASE-T/100BASE-TX Auxiliary Status Summary register. This bit returns 0 while auto-negotiation is in progress.

2.6.23.2 Auto-Negotiation Complete Acknowledge

The BCM84891L returns 1 in bit 14 of the 1000BASE-T/100BASE-TX Auxiliary Status Summary register when the auto-negotiation state machine has entered the link good check state since the last time this register was read; otherwise, it returns 0.

2.6.23.3 Auto-Negotiation Acknowledge Detect

The BCM84891L returns 1 in bit 13 of the 1000BASE-T/100BASE-TX Auxiliary Status Summary register when the auto-negotiation state machine has entered the acknowledge detect state since the last time this register was read; otherwise, it returns 0.

2.6.23.4 Auto-Negotiation Ability Detect

The BCM84891L returns 1 in bit 12 of the 1000BASE-T/100BASE-TX Auxiliary Status Summary register when the auto-negotiation state machine has entered the ability detect state since the last time this register was read; otherwise, it returns 0.

2.6.23.5 Auto-Negotiation Next Page Wait

The BCM84891L returns 1 in bit 11 of the 1000BASE-T/100BASE-TX Auxiliary Status Summary register when the auto-negotiation state machine has entered the Next Page wait state since the last time this register was read; otherwise, it returns 0.

2.6.23.6 Auto-Negotiation HCD (Current Operating Speed and Duplex Mode)

Bits [10:8] of the 1000BASE-T/100BASE-TX Auxiliary Status Summary register report the mode of operation negotiated between the BCM84891L and its link partner. As reported by bit 15 of the Auxiliary Status Summary register, the bits return 000 until auto-negotiation has completed. When the auto-negotiation function has been disabled, bits [10:8] report the manually selected mode of operation.

2.6.23.7 Parallel Detection Fault

When a parallel detection fault has occurred in the auto-negotiation state machine, bit 7 of the 1000BASE-T/100BASE-TX Auxiliary Status Summary register returns 1. When a parallel detection fault occurs, this bit is latched to 1 and remains so until the next register read. This bit returns 0 when a parallel detection fault has not occurred since the last time it was read.

2.6.23.8 Remote Fault

The BCM84891L returns 1 in bit 6 of the 1000BASE-T/100BASE-TX Auxiliary Status Summary register when the link partner has detected a remote fault; otherwise, it returns 0.

2.6.23.9 Auto-Negotiation Page Received

The BCM84891L returns 1 in bit 5 of the 1000BASE-T/100BASE-TX Auxiliary Status Summary register when a new link code word has been received from the link partner since the last time this register was read; otherwise, it returns 0.

2.6.23.10 Link Partner Auto-negotiation Ability

The BCM84891L returns 1 in bit 4 of the 1000BASE-T/100BASE-TX Auxiliary Status Summary register when the link partner is known to have auto-negotiation capability. Before any auto-negotiation information is exchanged or if the link partner does not comply with IEEE auto-negotiation, the bit returns 0.

2.6.23.11 Link Partner Next Page Ability

The BCM84891L returns 1 in bit 3 of the 1000BASE-T/100BASE-TX Auxiliary Status Summary register when the link partner must transmit Next Page information; otherwise, it returns 0.

2.6.23.12 Link Status

The BCM84891L returns 1 in bit 2 of the 1000BASE-T/100BASE-TX Auxiliary Status Summary register when the link status is good; otherwise, it returns 0.

2.6.23.13 Pause Resolution in the Receive Direction and Transmit Direction

When auto-negotiation has completed, the BCM84891L returns the result of the pause resolution function for full-duplex flow control on bits [1:0] of the 1000BASE-T/100BASE-TX Auxiliary Status Summary register. When bit 1 returns 1, the link partner can send pause frames toward the local device. When bit 0 returns 1, pause frames can be transmitted by the local device to the link partner. These bits are only guaranteed to be valid when bit 15 of the Auxiliary Status Summary register is 1.

2.6.24 1000BASE-T/100BASE-TX Register 1Ch Access (DEVAD = 7, Address = 0xFFFC)

Reading and writing to the 1000BASE-T/100BASE-TX register 1Ch (0xFFFC) is through register 1Ch (0xFFFC) bits [15:10]. Bits [14:10] set the shadow value of register 1Ch (0xFFFC), and bit 15 enables the writing of the bits [9:0]. Setting bit 15 allows writing to bits [9:0] of register 1Ch (0xFFFC). To read register 1C (0xFFFC) shadow zzzzz, set writes to register 1Ch with bit 15 = 0, and bits 14:10 to zzzzz first. The subsequent register read from register 1Ch (0xFFFC) contains the shadow zzzzz register value. The register 1Ch (0xFFFC) shadow values are listed in the table below.

Table 154: 1000BASE-T/100BASE-TX Register 1Ch Shadow Values (7.0xFFFC)

Shadow Value	Register Name
00100	1000BASE-T/100BASE-TX Spare Control 2 Register (7.0xFFFC)
01010	Auto Power-Down Register (7.0xFFFC)

2.6.25 1000BASE-T/100BASE-TX Spare Control 2 (DEVAD = 7, Address = 0xFFFC, Shadow Value 00100b)

1000BASE-T/100BASE-TX Spare Control 2 is enabled by register 1Ch with shadow value in bits [14:10] = 00100.

Table 155: 1000BASE-T/100BASE-TX Spare Control 2 Register (7.0xFFFC)

Bit	Name	R/W	Description	Default
15	Write Enable	R/W	1 = Write bits [9:0]. 0 = Read bits [9:0].	0
14:10	Shadow Register Selector	R/W	00100 = Spare Control 2 register.	00100
9:6	Reserved	R/W	Use read-modify-write to not change the current value during write. Ignore on read.	Undetermined
5	Reserved	R/W	Use read-modify-write to not change the current value during write. Ignore on read.	Undetermined
4:2	Ethernet@Wirespeed Retry Limit	RO	000 = Downgrade after two failed auto-negotiation attempts. 001 = Downgrade after three failed auto-negotiation attempts. 010 = Downgrade after four failed auto-negotiation attempts. 011 = Downgrade after five failed auto-negotiation attempts. 100 = Downgrade after six failed auto-negotiation attempts. 101 = Downgrade after seven failed auto-negotiation attempts. 110 = Downgrade after eight failed auto-negotiation attempts. 111 = Downgrade after nine failed auto-negotiation attempts.	0 1 1
1	Energy Detect on INTR Pin	R/W	1 = Routes Energy Detect to interrupt signal. Use LED selectors (register 1Ch shadow 01101 and 01110) and program to INTR mode. 0 = INTR pin is Interrupt function.	0
0	Reserved	R/W	Use read-modify-write to not change the current value during write. Ignore on read.	Undetermined

2.6.25.1 Write Enable

During a write to this register, setting bit 15 of the 1000BASE-T/100BASE-TX Spare Control 2 register allows writing to bits [9:0] of this register. To read the values of bits [9:0], perform an MDIO write with bit 15 cleared and preferred shadow values in bits [14:10]. The next MDIO read of register address 1Ch contains the preferred shadow register values in bits [9:0].

2.6.25.2 Shadow Register Selector

Bits [14:10] must be set to 00100 to enable a read/write to the 1000BASE-T/100BASE-TX Spare Control 2 register.

2.6.25.3 Ethernet@Wirespeed Retry Limit

Bits [4:2] set the number of auto-negotiation attempts to link up prior to speed downgrade. The Ethernet@Wirespeed mode must be enabled for these bits to work.

2.6.25.4 Energy Detect on INTR Pin

Bit 1 enables the signal detect or energy detect input on the INTR pin. Set the LED selector register to enable INTR LED mode (1Ch shadow 01101 or 01110 set bit [7:4]/[3:0] to 0110 depending on the LED).

2.6.26 1000BASE-T/100BASE-TX Auto Power-Down (DEVAD = 7, Address = 0xFFFC, Shadow Value 01010b)

Auto Power-Down is enabled by 1000BASE-T/100BASE-TX Auto Power-Down register 1Ch with shadow value in bits [14:10] = 01010.

Table 156: Auto Power-Down Register (7.0xFFFC)

Bit	Name	R/W	Description	Default
15	Write Enable	R/W	During a write to this register, setting this bit allows writing to bits [9:0] of this register. To read the values of bits [9:0], perform an MDIO write with this bit cleared and preferred shadow values in bits [14:10]. The next MDIO read of register address 1Ch contains the preferred shadow register values in bits [9:0]. 1 = Write bits [9:0]. 0 = Read bits [9:0].	0
14:10	Shadow Register Selector	R/W	These bits must be set to 01010 to enable a read/write to the 1000BASE-T/100BASE-TX Auto Power-Down register address 1Ch. 01010 = Auto Power-Down register.	01010
9:6	Reserved	R/W	Use read-modify-write to not change the current value during write. Ignore on read.	Undetermined
5	Auto Power-Down Mode	R/W	Setting this bit enables the auto power-down mode. 1 = Auto power-down mode enabled. 0 = Auto power-down mode disabled.	0
4	Sleep Timer Select	R/W	Setting this bit changes the wake-up time leaving auto power-down mode. 1 = Sleep timer is 5.4s. 0 = Sleep timer is 2.7s.	0

Table 156: Auto Power-Down Register (7.0xFFFC) (Continued)

Bit	Name	R/W	Description	Default
3:0	Wake-up Timer Select	R/W	The port continues wake-up mode for a time based on the count stored in this register. The minimum value is 84 ms and the maximum value is 1.26s. This only applies when the part is in auto power-down mode. Counter for wake-up timer in units of 84 ms. 0001 = 84 ms 0010 = 168 ms ... 1111 = 1.26s	0001

2.6.27 1000BASE-T/100BASE-TX Master/Slave Seed (DEVAD = 7, Address = FFFDh)

Table 157: 1000BASE-T/100BASE-TX Master/Slave Seed (7.FFFDh)

Bit	Name	R/W	Description	Default
15	Enable Shadow Register	R/W	1 = Select shadow register. 0 = Normal operation. Writes to the selected register are done on a single cycle.	0
14	Master/Slave Seed Match	RO LH	1 = Seeds match. 0 = Seeds do not match.	0
13	Link Partner Repeater/DTE Bit	RO	1 = Link partner is a repeater/switch device port. 0 = Link partner is a DTE device port.	0
12	Link Partner Manual Master/Slave Configuration Value	RO	1 = Link partner is configured as master. 0 = Link partner is configured as slave.	0
11	Link Partner Manual Master/Slave Configuration Enable	RO	1 = Link partner manual master/slave configuration enabled. 0 = Link partner manual master/slave configuration disabled.	0
10:0	Local Master/Slave Seed Value	R/W	Returns the automatically generated M/S random seed.	000h

2.6.27.1 Enable Shadow Register

When bit 15 of the 1000BASE-T/100BASE-TX Master/Slave Seed register is cleared, the Master/Slave Seed register is selected. If bit 15 is set, the shadow register HCD Status register is selected for read/write.

2.6.27.2 Master/Slave Seed Match

When bit 14 of the 1000BASE-T/100BASE-TX Master/Slave Seed register returns 1 when the master/slave seed matches; otherwise, it returns 0.

2.6.27.3 Link Partner Repeater/DTE Bit

When read-only bit 13 of the 1000BASE-T/100BASE-TX Master/Slave Seed register returns 1, the link partner is configured as a repeater or a switch. If this bit returns 0, the link partner is configured as a DTE port.

2.6.27.4 Link Partner Manual Master/Slave Configuration Value

When read-only bit 12 of the 1000BASE-T/100BASE-TX Master/Slave Seed register returns 1, the link partner is configured as a master. If this bit returns 0, the link partner is configured as a slave.

2.6.27.5 Link Partner Manual Master/Slave Configuration Enable

When read-only bit 11 of the 1000BASE-T/100BASE-TX Master/Slave Seed register returns 1, the link partner manual master/slave configuration is enabled. If this bit returns 0, the link partner manual master/slave configuration is disabled.

2.6.27.6 Local Master/Slave Seed Value

Bits [10:0] of the 1000BASE-T/100BASE-TX Master/Slave Seed register return the automatically generated local master/slave seed value.

2.6.28 1000BASE-T/100BASE-TX HCD Status (DEVAD = 7, Address = FFFDh)

Table 158: 1000BASE-T/100BASE-TX HCD Status (7.FFFDh)

Bit	Name	R/W	Description	Default
15	Enable Shadow Register	R/W	1 = Select Shadow register. 0 = Normal operation.	0
14	Ethernet@Wirespeed Disable Gigabit Advertising	RO	1 = Disable advertising Gigabit. 0 = Advertise Gigabit based on register 09h.	0
13	Ethernet@Wirespeed Disable 100TX Advertising	RO	1 = Disable advertising 100TX. 0 = Advertise 100TX based on register 04h.	0
12	Ethernet@Wirespeed Downgrade	RO LH	1 = Ethernet@Wirespeed downgrade occurred since last read. 0 = Ethernet@Wirespeed downgrade cleared.	0
11	HCD 1000BASE-T FDX	RO LH	1 = Gigabit full-duplex occurred since last read. 0 = HCD cleared.	0
10	HCD 1000BASE-T	RO LH	1 = Gigabit half-duplex occurred since last read. 0 = HCD cleared.	0
9	HCD 100BASE-TXFDX	RO LH	1 = 100BASE-TX full-duplex occurred since last read. 0 = HCD cleared.	0
8	HCD 100BASE-T	RO LH	1 = 100BASE-TX half-duplex occurred since last read. 0 = HCD cleared.	0
7:6	Reserved	R/W	Use read-modify-write to not change the current value during write. Ignore on read.	Undetermined
5	HCD 1000BASE-T FDX (Link Never Came Up)	RO LH	1 = Gigabit full-duplex HCD and the *link never came up* occurred since the last read. 0 = HCD cleared.	0
4	HCD 1000BASE-T (Link Never Came Up)	RO LH	1 = Gigabit half-duplex HCD and the *link never came up* occurred since the last read. 0 = HCD cleared.	0
3	HCD 100BASE-TX FDX (Link Never Came Up)	RO LH	1 = 100BASE-TX full-duplex HCD and the *link never came up* occurred since the last read. 0 = HCD cleared.	0

Table 158: 1000BASE-T/100BASE-TX HCD Status (7.FFFDh) (Continued)

Bit	Name	R/W	Description	Default
2	HCD 100BASE-T (Link Never Came Up)	RO LH	1 = 100BASE-TX half-duplex HCD and the *link never came up* occurred since the last read. 0 = HCD cleared.	0
1:0	Reserved	R/W	Use read-modify-write to not change the current value during write. Ignore on read.	Undetermined

NOTE: Bits 12:0 are cleared when auto-negotiation is disabled through MII register 0 bit 12 or restarted through MII register 0 bit 9.

2.6.28.1 Enable Shadow Register

When bit 15 of 1000BASE-T/100BASE-TX HCD Status register is cleared, the 1000BASE-T/100BASE-TX Master/Slave Seed register is selected. If bit 15 is set, the shadow register HCD Status register (auto-negotiation highest common denominator resolution), is selected for read/write. This bit must be set to be able to read/write to the HCD Status register.

2.6.28.2 Ethernet@Wirespeed Disable Gigabit Advertising

When bit 14 = 1, 1000BASE-T half-duplex and 1000BASE-T full-duplex are not advertised.

2.6.28.3 Ethernet@Wirespeed Disable 100BASE-TX Advertising

When bit 13 = 1, 100BASE-TX half-duplex and 100BASE-TX full-duplex are not advertised.

2.6.28.4 Ethernet@Wirespeed Downgrade

When bit 12 = 1, an Ethernet@Wirespeed downgrade has occurred since the last read.

2.6.28.5 HCD 1000BASE-T FDX

When bit 11 of the 1000BASE-T/100BASE-TX HCD Status register returns 1, a Gigabit full-duplex HCD has occurred since the last read.

2.6.28.6 HCD 1000BASE-T

When bit 10 of the 1000BASE-T/100BASE-TX HCD Status register returns 1, a Gigabit half-duplex HCD has occurred since the last read.

2.6.28.7 HCD 100BASE-TX FDX

When bit 9 of the 1000BASE-T/100BASE-TX HCD Status register returns 1, a 100BASE-TX full-duplex HCD has occurred since the last read.

2.6.28.8 HCD 100BASE-T

When bit 8 of the 1000BASE-T/100BASE-TX HCD Status register returns 1, a 100BASE-TX half-duplex HCD has occurred since the last read.

2.6.28.9 HCD 1000BASE-T FDX (Link Never Came Up)

When bit 5 of the 1000BASE-T/100BASE-TX HCD Status register returns 1, a Gigabit full-duplex HCD has occurred, but the link was not established since the last read.

2.6.28.10 HCD 1000BASE-T (Link Never Came Up)

When bit 4 of the 1000BASE-T/100BASE-TX HCD Status register returns 1, a Gigabit half-duplex HCD has occurred, but the link was not established since the last read.

2.6.28.11 HCD 100BASE-TX FDX (Link Never Came Up)

When bit 3 of the 1000BASE-T/100BASE-TX HCD Status register returns 1, a 100BASE-TX full-duplex HCD has occurred, but the link was not established since the last read.

2.6.28.12 HCD 100BASE-TX (Link Never Came Up)

When bit 2 of the 1000BASE-T/100BASE-TX HCD Status register returns 1, a 100BASE-TX half-duplex HCD has occurred, but the link was not established since the last read.

2.6.29 1000BASE-T/100BASE-TX Test Register 1 (DEVAD = 7, Address = FFFEh)

Table 159: 1000BASE-T/100BASE-TX Test Register 1 (7.FFFEh)

Bit	Name	R/W	Description	Default
15	CRC Error Counter Selector	R/W	Setting this bit enables the 1000BASE-T/100BASE-TX Receiver NOT_OK Counter (DEVAD = 7, Address = FFF4h) to start counting CRC errors and store the counts in register 14h. 1 = Receiver NOT_OK Counters (register 14h) becomes 16-bit CRC error counter (CRC errors are counted only after this bit is set). 0 = Normal operation.	0
14:8	Reserved	R/W	Use read-modify-write to not change the current value during write. Ignore on read.	Undetermined
7	Manual Swap MDI State	R/W	Setting this bit manually swaps the MDI transmit and receive pairs during forced 100BASE-TX operation. When set, the BCM84891L transceiver transmits on pairs TRD± {1} and receives on TRD± {0} when operating in 100BASE-TX mode. If cleared, the BCM84891L transmits on pairs TRD± {0} and receives on TRD± {1} when operating in 100BASE-TX mode. This bit is ignored when auto-negotiation is enabled. **NOTE:** To change the MDI state in forced 100BASE-TX mode, the PHY must first be put into a non-link condition, set bit 7 = 1, and finally set the PHY into force 100BASE-TX mode. 1 = Manually swap MDI state. 0 = Normal operation.	0
6:0	Reserved	R/W	Use read-modify-write to not change the current value during write. Ignore on read.	Undetermined

2.6.30 Expansion Register 00h: Receive/Transmit Packet Counter

Expansion register 00h is enabled by writing to 1000BASE-T/100BASE-TX Expansion (FFF7h) bits 11:0 = 'F00'h, and read/write access is through register FFF5h.

Table 160: Expansion Register 00h: Receive/Transmit Packet Counter

Bit	Name	R/W	Description	Default
15:0	Packet Counter (copper only)	R/W CR	Returns the transmitted and received packet count. The counter mode is set by bit 11 of 1000BASE-T/100BASE-TX Misc. Control Register (7.0xFFF8). Either receive or transmit packets are counted. This counter is cleared on read and freezes at FFF8h.	0000h

2.6.31 Expansion Register 42h: Operating Mode Status

Expansion register 42h is enabled by writing to 1000BASE-T/100BASE-TX Expansion Register Access Register (DEVAD = 7, Address = FFF7h) bits 11:0 = F42h, and read/write access is through register (DEVAD = 7, Address = FFF5h).

Table 161: Expansion Register 42h: Operating Mode Status Register

Bit	Name	R/W	Description	Default
15	SerDes Link	RO	1 = Link up in fiber, SGMII, or media converter modes (when set in SGMII or media converter mode, both copper and SerDes link must be valid). 0 = Link down.	0
14:13	SerDes Speed	RO	10 = SerDes speed 1000 (SGMII 1000BASE or 1000BASE-X). 01 = SerDes speed 100. 00 = Reserved.	10
12	SerDes Duplex	RO	1 = SerDes full-duplex. 0 = SerDes half-duplex or auto-negotiation in progress.	0
11	Copper Link	RO	1 = Link up on copper side (copper, SGMII, or GBIC mode). 0 = Link down.	0
10:9	Copper Speed	RO	10 = 1000BASE-T. 01 = 100BASE-T. 00 = Auto-negotiation in progress.	00
8	Copper Duplex	RO	1 = Full-duplex. 0 = Half-duplex or auto-negotiation in progress.	0
7	Copper Energy Detect	RO	1 = Copper energy detected. 0 = No copper energy detected.	0
6	Fiber Signal Detect	RO	1 = Fiber signal detect from pin (filtered) (same as register 1ch shadow 11111 [4]). 0 = No fiber signal detect from pin.	0
5	Sync Status	RO	1 = Valid SerDes PCS receive synchronization. 0 = Invalid SerDes PCS receive synchronization.	0

Table 161: Expansion Register 42h: Operating Mode Status Register (Continued)

Bit	Name	R/W	Description	Default
4:0	Operating Mode Status	RO	00000 = Reserved. 00001 = Reserved. 00010 = Reserved. 00011 = Reserved. 00100 = Reserved. 00101 = Reserved. 00110 = Reserved. 00111 = Reserved. 01000 = Reserved. 01001 = Reserved. 01010 = Reserved. 01011 = Reserved. 01100 = Reserved. 01101 = Reserved. 01110 = Reserved. 01111 = Reserved. 10000 = Reserved. 10001 = Reserved. 10010 = Reserved. 10011 = Reserved. 10100 = Reserved. 10101 = Reserved. 10110 = Reserved. 10111 = Reserved.	00000

2.6.32 Expansion Register 46h: Pattern Generator Status

Expansion register 46h is enabled by writing to 1000BASE-T/100BASE-TX Expansion Register Access Register (DEVAD = 7, Address = FFF7h) bits 11:0 = F46h, and read/write access is through register (DEVAD = 7, Address = FFF5h).

Table 162: Expansion Register 46h: Operating Mode Status Register

Bit	Name	R/W	Description	Default
15	Reserved	R/W	Use read-modify-write to not change the current value during write. Ignore on read.	Undetermined
14	1000BASE-T Transmit FIFO Elasticity (copper mode) (MSB)	R/W	FIFO Elasticity [MSB:LSB] 11 = Supports 18 KB packets. 10 = Supports 13.5 KB packets. 01 = Supports 9 KB packets. LSB located at Register FFF0, bit 0.	Set by firmware
12:0	Reserved	RO	Ignore on read.	Undetermined

2.7 XFI Registers

2.7.1 XFI PMD_PMA Register Description (DEVAD = 1 PMA/PMD)

2.7.1.1 XFI 10GBASE-R PMD Control Register (DEVAD = 1, Address = 0x0000)

Table 163: XFI 10GBASE-R PMD Control Register (1.0x0000)

Bit(s)	Name	R/W	Description	Default
15	Reset	R/W	1 = Active-high. Reset digital core section. It is a self-clearing bit.	0
14	Reserved	RO	Ignore on read.	Undetermined
13	Speed Selection	R/W	1.0.6 1.0.13 1 1 = Bit 5:2 select speed 1 0 = 1000 Mb/s 0 1 = 100 Mb/s 0 0 = Reserved	1
12	Reserved	RO	Ignore on read.	Undetermined
11	Low Power	R/W	1 = Low power. 0 = Normal operation. Disables the sublayer clocks for low power.	0
10:7	Reserved	RO	Ignore on read.	Undetermined
6	Speed Selection	R/W	1.0.6 1.0.13 1 1 = Bit 5:2 select speed 1 0 = 1000 Mb/s 0 1 = 100 Mb/s 0 0 = Reserved	1
5:2	Speed Selection	R/W	0000 = 10 Gb/s All other codes are reserved.	0000
1	Reserved	RO	Ignore on read.	Undetermined
0	PMA Loopback	RO	1 = Enables PMA loopback.	0

2.7.1.2 XFI 10GBASE-R Status Register (DEVAD = 1, Address = 0x0001)

Table 164: XFI 10GBASE-R Status Register (1.0x0001)

Bit(s)	Name	R/W	Description	Default
15:8	Reserved	RO	Ignore on read.	Undetermined
7	Local Fault	RO	1 = Local fault condition detected. 0 = Local fault condition not detected.	1
6:3	Reserved	RO	Ignore on read	Undetermined
2	Receive Link Status	RS/LL	1 = PMD Link is good. 0 = PMD Link is down.	0
1	Low Power ability	RO	1 = PMD supports low power.	0
0	Reserved	RO	Ignore on read.	Undetermined

2.7.1.3 XFI 10GBASE-R PMD Speed Ability Register (DEVAD = 1, Address = 0x0004)

Table 165: XFI 10GBASE-R PMD Speed Ability (1.0x0004)

Bit(s)	Name	R/W	Description	Default
15:6	Reserved	RO	Ignore on read.	Undetermined
5	speed100M	RO	1 = PMA/PMD is capable of operating at 100 Mb/s. 0 = PMA/PMD is not capable of operating at 100 Mb/s.	0x1
4	speed1000M	RO	1 = PMA/PMD is capable of operating at 1000 Mb/s. 0 = PMA/PMD is not capable of operating at 1000 Mb/s.	0x1
3:1	Reserved	RO	Ignore on read.	Undetermined
0	10G-capable	RO	1 = PMD capable of operating at 10G.	1

2.7.1.4 XFI 10GBASE-R Device in Package 1 Register (DEVAD = 1, Address = 0x0005)

Table 166: XFI 10GBASE-R Devices in Package 1 (1.0x0005)

Bit(s)	Name	R/W	Description	Default
15:8	Reserved	RO	Ignore on read.	Undetermined
7	Auto Neg Present	RO	1 = Auto-negotiation present in the package.	1
6	TC Present	RO	1 = TC present in the package.	0
5	DTE XS present	RO	1 = DTE XS present in the package.	0
4	PHY XS present	RO	1 = PHY XS present in the package.	0
3	PCS present	RO	1 = PCS present in the package.	1
2	WIS present	RO	1 = WIS present in the package.	0
1	PMD/PMA present	RO	1 = PMD/PMA present in the package.	1
0	Clause 22 registers present	RO	1 = Clause 22 registers present.	1

NOTE: All registers, including Clause 22 registers, are accessible through Clause 45 in this device.

2.7.1.5 XFI 10GBASE-R Device in Package 2 Register (DEVAD = 1, Address = 0x0006)

Table 167: XFI 10GBASE-R Devices in Package 2 (1.0x0006)

Bit(s)	Name	R/W	Description	Default
15	Vendor-specific device present	RO	1 = Vendor-specific device present.	0
14	Vendor-specific device 1 present	RO	1 = Vendor-specific device present.	0
13	CL22 Extension Present	RO	1 = Clause 22 extension present in the package.	1
12:0	Reserved	RO	Ignore on read.	Undetermined

2.7.1.6 XFI 10GBASE-R PMD Control 2 Register (DEVAD = 1, Address = 0x0007)

Table 168: XFI 10GBASE-R PMD Control 2 Register (1.0x0007)

Bit(s)	Name	R/W	Description	Default
15:4	Reserved	RO	Ignore on read.	Undetermined
3:0	PMA Type Selection	R/W	1 1 1 1 = Reserved 1 1 1 0 = 100BASE-TX PMA/PMD type 1 1 0 1 = 1000BASE-KX PMA/PMD type 1 1 0 0 = 1000BASE-T PMA/PMD type 1 0 1 1 = 10GBASE-KR PMA/PMD type 1 0 1 0 = 10GBASE-KX4 PMA/PMD type 1 0 0 1 = 10GBASE-T PMA type 1 0 0 0 = 10GBASE-LRM PMA/PMD type 0 1 1 1 = 10GBASE-SR PMA/PMD type 0 1 1 0 = 10GBASE-LR PMA/PMD type 0 1 0 1 = 10GBASE-ER PMA/PMD type 0 1 0 0 = 10GBASE-LX4 PMA/PMD type 0 0 1 1 = 10GBASE-SW PMA/PMD type 0 0 1 0 = 10GBASE-LW PMA/PMD type 0 0 0 1 = 10GBASE-EW PMA/PMD type 0 0 0 0 = 10GBASE-CX4 PMA/PMD type	0110
NOTE: This register can be loaded from the nonvolatile memory.				

2.7.1.7 XFI 10GBASE-R Status 2 Register (DEVAD = 1, Address = 0x0008)

Table 169: XFI 10GBASE-R Status 2 Register (1.0x0008)

Bit(s)	Name	R/W	Description	Default
15:14	Device present	RO	10 = Device responding at this address.	10
13	Transmit local fault ability	RO	1 = Detects local fault condition on the transmit path.	1
12	Receive local fault ability	RO	1 = Detects local fault condition on the receive path.	1
11	Transmit local fault	R/LH	1 = Local fault condition detected on transmit path.	1
10	Receive local fault	R/LH	1 = Local fault condition detected on receive path.	1
9	Extended abilities	RO	1 = PMD has extended abilities listed in register 1.11 (address 0x000B).	1
8	PMD transmit disable ability	RO	1 = PMD can disable the transmit path.	1
7	10GBASE-SR ability	RO	1 = Able to perform 10GBASE-SR.	0
6	10GBASE-LR ability	RO	1 = Able to perform 10GBASE-LR.	0
5	10GBASE-ER ability	RO	1 = Able to perform 10GBASE-ER.	0
4	10GBASE-LX4 ability	RO	1 = Able to perform 10GBASE-LX4.	0
3	10GBASE-SW ability	RO	1 = Able to perform 10GBASE-SW.	0
2	10GBASE-LW ability	RO	1 = Able to perform 10GBASE-LW.	0
1	10GBASE-EW ability	RO	1 = Able to perform 10GBASE-EW.	0
0	PMA Loopback ability	RO	1 = Able to perform PMA loopback.	1

2.7.1.8 XFI 10GBASE-R PMD Transmit Disable Register (DEVAD = 1, Address = 0x0009)

Table 170: XFI 10GBASE-R Transmit Disable Register (1.0x0009)

Bit(s)	Name	R/W	Description	Default
15:5	Reserved	RO	Ignore on read.	Undetermined
4	PMD transmit disable 3	RO[a]	1 = Disable output on transmit lane 3. Not used. Bits 3, 2, and 1 are the same, but for lanes 2, 1, and 0.	0
3	PMD transmit disable 2	RO[a]	1 = Not used.	0
2	PMD transmit disable 1	RO[a]	1 = Not used.	0
1	PMD transmit disable 0	RO[a]	1 = Not used.	0
0	Global PMD transmit disable	R/W	1 = Disable transmitter output.	0

a. Cannot program bits 4:1.

2.7.1.9 XFI 10GBASE-R PMD Receive Signal Detect Register (DEVAD = 1, Address = 0x000A)

Table 171: XFI 10GBASE-R PMD Receive Signal Detect Register (1.0x000A)

Bit(s)	Name	R/W	Description	Default
15:5	Reserved	RO	Ignore on read.	Undetermined
4	PMD receive signal detect 3	RO	1 = Signal detected on receive lane 3.	0
3	PMD receive signal detect 2	RO	1 = Signal detected on receive lane 2.	0
2	PMD receive signal detect 1	RO	1 = Signal detected on receive lane 1.	0
1	PMD receive signal detect 0	RO	1 = Signal detected on receive lane 0.	0
0	Global PMD receive signal OK	RO	1 = Signal OK on receive.	0

2.7.1.10 XFI 10GBASE-R PMD Extended Ability Register (DEVAD = 1, Address = 0x0000B)

Table 172: XFI 10GBASE-R PMD Extended Ability Register (1.0x000B)

Bit(s)	Name	R/W	Description	Default
15:8	Reserved	RO	Ignore on read.	Undetermined
7	100BASE-TX ability	RO	1 = Able to perform 100BASE-TX.	0
6	1000BASE-KX ability	RO	1 = Able to perform 1000BASE-KX.	1
5	1000BASE-T ability	RO	1 = Able to perform 1000BASE-T.	0
4	10GBASE-KR ability	RO	1 = Able to perform 10GBASE-KR.	1
3	10GBASE-KX4 ability	RO	1 = Able to perform 10GBASE-KX4.	0
2	10GBASE-T ability	RO	1 = Able to perform 10GBASE-T.	0
1	10GBASE-LRM ability	RO	1 = Able to perform 10GBASE-LRM.	0
0	10GBASE-CX4 ability	RO	1 = Able to perform 10GBASE-CX4.	0

2.7.1.11 XFI_TX_prbs_gen_config: PRBS Generator Control (DEVAD = 1, Address = 0xD0E1)

Table 173: XFI_TX_prbs_gen_config: PRBS Generator Control (1.0xD0E1)

Bit(s)	Name	R/W	Description	Default
15:6	Reserved	RSVD	Reserved bits write has no effect, and read always returns 0.	Undetermined
5	prbs_gen_err_ins	R/W	PRBS error insert. 0-to-1 transition on this signal inserts single bit error in the MSB bit of the data bus. Reset value is 0x0.	0
4	prbs_gen_inv	R/W	PRBS invert enable. 1 = Inverts all the data bits from the PRBS generator. 0 = Sends normal data from the PRBS generator. Reset value is 0x0.	0
3:1	prbs_gen_mode_sel	R/W	PRBS generator mode select. Selects the PRBS polynomial as shown below: 3'd0: PRBS 7 3'd1: PRBS 9 3'd2: PRBS 11 3'd3: PRBS 15 3'd4: PRBS 23 3'd5: PRBS 31 3'd6: PRBS 58 (1 + x^39 + x^58) 3'd7: Reserved for future use. Reset value is 0x5.	0
0	prbs_gen_en	R/W	PRBS generator enable. 1 = Enables the PRBS generator. 0 = Disables the PRBS generator. Reset value is 0x0.	0

2.7.1.12 XFI_RX_prbs_chk_config: PRBS Checker Control (DEVAD = 1, Address = 0xD0D1)

Table 174: XFI_RX_prbs_chk_config: PRBS Checker Control (1.0xD0D1)

Bit(s)	Name	R/W	Description	Default
15:12	Reserved	RSVD	Reserved bits write has no effect, and read always returns 0.	Undetermined
11	prbs_chk_clk_en_frc_on	R/W	PRBS checker clock enable. 1'b1 enables PRBS checker clock. Should be enabled before enabling prbs_chk_en. Reset value is 0x0.	0
10	trnsum_error_count_en	R/W	Training sum error counter mode enable. 1 = Makes the PRBS error counter to be used as trnsum_error counter. PRBS checker cannot be used during this mode. 0 = PRBS checker mode. Reset value is 0x0.	0

Table 174: XFI_RX_prbs_chk_config: PRBS Checker Control (1.0xD0D1) (Continued)

Bit(s)	Name	R/W	Description	Default
9	prbs_chk_err_cnt_burst_ mode	R/W	PRBS error counter mode. 1 = Each error burst is counted as 1 error in the error counter. Each error burst must be separated by 1 error-free cycle of data, which in worst case should be 39 bits. 0 = Each bit error is counted. Reset value is 0x0.	0
8	Reserved	RSVD	Reserved bits write has no effect, and read always returns 0.	Undetermined
7	prbs_chk_en_auto_mode	R/W	PRBS checker enable mode control. 1 = Selects (rx_dsc_lock and prbs_chk_en) as PRBS checker enable control. 0 = Selects prbs_chk_en as PRBS checker enable control. Reset value is 0x0.	0
6:5	prbs_chk_mode	RSVD	PRBS lock state machine select. 2'd0: Self-sync mode with hysteresis. PRBS seed register is continuously seeded with previous received bits. 2'd1: Initial seed mode with hysteresis. PRBS seed register is seeded with previous received bits only till PRBS lock is acquired and then runs locally and independently from the received data until the checker goes out of PRBS lock. 2'd2: Initial seed mode without hysteresis. Similar to mode 1, except once locked it stays locked until PRBS is disabled. 2'd3: Reserved for future use. Reset value is 0x1.	Undetermined
4	prbs_chk_inv	R/W	PRBS invert enable. 1 = Inverts all the data bits to the PRBS checker. 0 = Sends normal data to the PRBS checker. Reset value is 0x0.	0
3:1	prbs_chk_mode_sel	R/W	PRBS checker mode select. Selects the PRBS polynomial as shown below: 3'd0: PRBS 7 3'd1: PRBS 9 3'd2: PRBS 11 3'd3: PRBS 15 3'd4: PRBS 23 3'd5: PRBS 31 3'd6: PRBS 58 (1 + x^39 + x^58) 3'd7: Reserved for future use. Reset value is 0x5.	0
0	prbs_chk_en	R/W	PRBS checker enable. 1 = Enables the PRBS checker. 0 = Disables the PRBS checker. Reset value is 0x0.	0

2.7.1.13 XFI_RX_prbs_chk_lock_status: PRBS Checker LOCK Status (DEVAD = 1, Address = 0xD0D9)

Table 175: XFI_RX_prbs_chk_lock_status: PRBS Checker LOCK Status (1.0xD0D9)

Bit(s)	Name	R/W	Description	Default
15:1	Reserved	RSVD	Reserved bits write has no effect, and read always returns 0.	Undetermined
0	prbs_chk_lock	RO	PRBS checker lock indication. This is a live indication of the status of the PRBS checker state machine. 1 = PRBS checker is in locked state. 0 = PRBS checker is out of lock state and state machine is searching for a lock. Reset value is 0x0.	0

2.7.1.14 XFI_RX_prbs_chk_err_cnt_msb_status: PRBS Checker Error Counter MSB Status (DEVAD = 1, Address = 0xD0DA)

Table 176: XFI_RX_prbs_chk_err_cnt_msb_status: PRBS Checker Error Counter MSB Status (1.0xD0DA)

Bit(s)	Name	R/W	Description	Default
15	prbs_chk_lock_lost_lh	RO	PRBS checker LOCK_LOST latch high indication. This register captures the 1 to 0 transition on the prbs_chk_lock live status register and keeps it latched until read. This is a clear-on-read status register. Reset value is 0x1.	0
14:0	prbs_chk_err_cnt_msb	RO	15 bits MSB portion of PRBS Checker Error Counter Status register. It is a clear-on-read register. Once the MSB bits [30:16] of the counter are read, LSB bits [15:0] of the error counter are loaded into a holding register, and all internal PRBS error counter's bits are cleared to 0s (or if there are any errors in that particular clock cycle, they are loaded). MSB portion must be read first before reading the LSB portion of the error counter. Reset value is 0x0.	0

2.7.1.15 XFI_RX_prbs_chk_err_cnt_lsb_status: PRBS Checker Error Counter LSB Status (DEVAD = 1, Address = 0xD0DB)

Table 177: XFI_RX_prbs_chk_err_cnt_lsb_status: PRBS Checker Error Counter LSB Status (1.0xD0DB)

Bit(s)	Name	R/W	Description	Default
15:0	prbs_chk_err_cnt_lsb	RO	16 bits LSB portion of PRBS Checker Error Counter Status register. This register indicates the value in the holding register when MSB portion [30:16] of the error counter are read. MSB portion must be read first before reading the LSB portion of the error counter. Reset value is 0x0.	0

2.7.2 XFI PCS Register Description (DEVAD = 3 PHY XS) 15867339858

2.7.2.1 XFI 10GBASE-R PCS Control 1 Register (DEVAD = 3, Address = 0x0000)

Table 178: XFI 10GBASE-R PCS Control 1 Register (3.0x0000)

Bit(s)	Name	R/W	Description	Default
15	Reset	R/W	1 = Active-high. Reset digital core section. Self-clearing after completion.	0
14	Loopback	R/W	1 = Active-high. Enables PCS system loopback.	0
13	Speed Selection LSB	R/W	Only 1 can be written. 0 is not allowed.	1
12	Reserved	RO	Ignore on read.	Undetermined
11	Power Down	R/W	1 = Low power. 0 = Normal operation. Disables sublayer clocks for low power.	0
10:7	Reserved	RO	Ignore on read.	Undetermined
6	Speed Selection MSB	R/W	Only 1 can be written. 0 is not allowed.	1
5:2	Speed Selection	R/W	0000 = 10 Gb/s. No others are valid.	0000
1:0	Reserved	RO	Ignore on read.	Undetermined

2.7.2.2 XFI 10GBASE-R Status 1 Register (DEVAD = 3, Address = 0x0001)

Table 179: XFI 10GBASE-R Status 1 Register (3.0x0001)

Bit(s)	Name	R/W	Description	Default
15:12	Reserved	RO	Ignore on read.	Undetermined
11	TX_LPI_RECEIVED	RO	1 = TX PCS has received LP idle. 0 = LP Idle not received LH.	Undetermined
10	RX_LPI_RECEIVED	RO	1 = RX PCS has received LP idle. 0 = LP Idle not received LH.	Undetermined
9	TX_LPI_INDICATION	RO	1 = TX PCS is currently receiving LP idle. 0 = PCS is not currently receiving LP idle.	Undetermined
8	RX_LPI_INDICATION	RO	1 = RX PCS is currently receiving LP idle. 0 = PCS is not currently receiving LP idle.	Undetermined
7	Local fault	RO	1 = Local fault detected.	1
6:3	Reserved	RO	Ignore on read.	Undetermined
2	PCS receive link status	R/LL	1 = PCS Receive link-up. Latching low version of 0x0020.12.	0
1	Low power ability	RO	Supports low power.	0
0	Reserved	RO	Ignore on read.	Undetermined

2.7.2.3 XFI 10GBASE-R Speed Ability Register (DEVAD = 3, Address = 0x0004)

Table 180: XFI 10GBASE-R Speed Ability (3.0x0004)

Bit(s)	Name	R/W	Description	Default
15:1	Reserved	RO	Ignore on read.	Undetermined
0	10G-capable	RO	1 = PMD can operate at 10G.	1

2.7.2.4 XFI 10GBASE-R Devices in Package 1 Register (DEVAD = 3, Address = 0x0005)

Table 181: XFI 10GBASE-R Devices in Package 1 (3.0x0005)

Bit(s)	Name	R/W	Description	Default
15:8	Reserved	RO	Ignore on read.	Undetermined
7	AN	RO	1 = Auto-negotiation present in package. 0 = Auto-negotiation not present in package.	0x1
6	Reserved	RO	Ignore on read.	Undetermined
5	DTE XS present	RO	1 = DTE XS present in package.	0
4	PHY XS present	RO	1 = PHY XS present in package.	0
3	PCS present	RO	1 = PCS present in package.	1
2	WIS present	RO	1 = WIS present in package.	0
1	PMD/PMA present	RO	1 = PMD/PMA present in package.	1
0	Clause 22 registers present	RO	1 = Clause 22 registers present.	1

2.7.2.5 XFI 10GBASE-R Device in Package 2 Register (DEVAD = 3, Address = 0x0006)

Table 182: XFI 10GBASE-R Devices in Package 2 (3.0x0006)

Bit(s)	Name	R/W	Description	Default
15	Vendor-specific device present	RO	1 = Vendor-specific device present.	0
14	Vendor-specific device 1 present	RO	1 = Vendor-specific device present.	0
13:0	Reserved	RO	Ignore on read.	Undetermined

2.7.2.6 XFI 10GBASE-R PCS Control 2 Register (DEVAD = 3, Address = 0x0007)

Table 183: XFI 10GBASE-R PCS Control 2 Register (3.0x0007)

Bit(s)	Name	R/W	Description	Default
15:2	Reserved	RO	Ignore on read.	Undetermined
1:0	PCS type selection	R/W	11 = Reserved. 10 = 10GBASE-W PCS Type (Not available). 01 = 10GBASE-X PCS Type (Not available). 00 = 10GBASE-R PCS Type.	00

2.7.2.7 XFI 10GBASE-R PCS Status 2 Register (DEVAD = 3, Address = 0x0008)

Table 184: XFI 10GBASE-R PCS Status 2 Register (3.0x0008)

Bit(s)	Name	R/W	Description	Default
15:14	Device present	RO	A 10 indicates device responds at this address: for any other value, it does not.	10
13:12	Reserved	RO	Ignore on read.	Undetermined
11	Transmit local fault	R/LH	1 = Local fault condition on transmit path.	0
10	Receive local fault	R/LH	1 = Local fault condition on receive path. Latching high version of the inverse of 10R_status (12) bit.	1
9:3	Reserved	RO	Ignore on read.	Undetermined
NOTE: 1: Transmit local fault. TX FIFO collision. 2: Receive local fault. R64 loss of block lock.				

Table 184: XFI 10GBASE-R PCS Status 2 Register (3.0x0008) (Continued)

Bit(s)	Name	R/W	Description	Default
2	10GBASE-W capable	RO	1 = PCS able to support 10GBASE-W PCS type.	0
1	10GBASE-X capable	RO	1 = PCS able to support 10GBASE-X.	0
0	10GBASE-R	RO	1 = PCS able to support 10GBASE-R.	1
NOTE: 1: Transmit local fault. TX FIFO collision. 2: Receive local fault. R64 loss of block lock.				

2.7.2.8 XFI 10GBASE-R PCS Status 1 (DEVAD = 3, Address = 0x0020)

Table 185: XFI 10GBASE-R PCS Status 1 (DEVAD = 3, Address = 0x0020)

Bit(s)	Name	R/W	Description	Default
15:13	RESERVED	RO	Reserved bits write has no effect and read always returns 0.	0
12	RCV_LINK_STS	RO	10GBASE-T receive link status. 1 = 10GBASE-R or 10GBASE-T PCS receive link up. 0 = 10GBASE-R or 10GBASE-T PCS receive link down.	0
11:4	RESERVED	RO	Reserved bits write has no effect and read always returns 0.	0
3	PRBS9_ABILITY	RO	PRBS9 Pattern testing ability. 0= PCS cannot support PRBS9 pattern testing. 1 = PCS can support PRBS9 pattern testing.	0
2	PRBS31_CAP	RO	PRBS31 pattern testing ability. 1 = PCS can support PRBS31 pattern testing. 0 = PCS cannot support PRBS31 pattern testing.	0
1	HBER	RO	PCS high BER. 1 = PCS reporting a high BER. 0 = PCS not reporting a high BER.	0
0	BLK_LOCK	RO	PCS block lock. 1 = PCS locked to received blocks. 0 = PCS not locked to received blocks.	0

2.7.2.9 XFI 10GBASE-R Status 2 (DEVAD = 3, Address = 0x0021)

Table 186: XFI 10GBASE-R Status 2 (DEVAD = 3, Address = 0x0021)

Bit(s)	Name	R/W	Description	Default
15	BLK_LOCK_L	RO	Latched low block lock. 1 = PCS locked to received blocks. 0 = PCS not locked to received blocks.	0
14	HBER_L	RO	Latched high BER. 1 = PCS reporting a high BER. 0 = PCS not reporting a high BER.	Undetermined
13:8	BER	RO	BER counter, same as LFER_COUNT. Saturates at 0x3F. Clear by read of this register or every 125 µs.	0x0
7:0	ERR_BLK_CNT	RO	Errored blocks counter. Saturates at 0xFF. Clear by read of this register.	0x0

2.8 User-Defined Registers (Device = 30)

2.8.1 AutogrEEEn Control 1 Register (DEVAD = 30, Address = 0x400A)

Table 187: AutogrEEEn Threshold High Register (DEVAD = 30, Address = 0X400B)

Bit(s)	Name	R/W	Description	Default
15:2	Reserved	RO	Write as 00h, ignore on read.	00h
1	TXAI_TX_AI_LPI_MODE	R/W	1 = Variable latency. 0 = Constant latency.	0
0	AILPIEN	R/W	1 = AILPI is enabled on both TX and RX path. 0 = AILPI is disabled on both TX and RX path.	0

2.8.2 AutogrEEEn Threshold High Register (DEVAD = 30, Address = 0X400B)

Table 188: AutogrEEEn Threshold High Register (DEVAD = 30, Address = 0X400B)

Bit(s)	Name	R/W	Description	Default
15:0	AutogrEEEn Threshold High	R/W	AutogrEEEn threshold high.	0

2.8.3 AutogrEEEn Threshold Low Register (DEVAD = 30, Address = 0X400C)

Table 189: AutogrEEEn Threshold Low Register (DEVAD = 30, Address = 0X400C)

Bit(s)	Name	R/W	Description	Default
15:0	AutogrEEEn Threshold Low	R/W	AutogrEEEn threshold low.	0

2.8.4 Status Register (DEVAD = 30, Address = 0x400D)

Table 190: Status Register (30.0x400D)

Bit	Name	R/W	Description	Default
15:14	SPIROM CRC check status	RO	Device initialized CRC check status: 00 = SPIROM CRC check is ongoing. 01 = SPIROM good CRC. 10 = SPIROM bad CRC. 11 = Reserved.	0
13	MAC side link status	RO	1 = Link is up. 0 = Link is down.	—
12	Fiber status	–	1 = Line-side XFI (fiber) is up. 0 = Line-side XFI (fiber) is down.	0
11	Lineside_Media	–	0 = Copper PHY. 1 = XFI PHY.	0
10:9	Frame type	–	0 = Reserved 1 = IEEE802p3BZ 2 = NBASET 3 = Reserved	00
7:8	Reserved	–	–	0

Table 190: Status Register (30.0x400D) (Continued)

Bit	Name	R/W	Description	Default
6	Media priority	–	0 = Copper priority 1 = Fiber priority	0
5	Copper link status	RO	Copper link status: 0 = Copper link is not up. 1 = Copper link is up.	0
4:2	Copper speed	RO	Copper speed: 000 = Reserved 010 = 100M 100 = 1G 110 = 10G 001 = 2.5G 011 = 5G	0
1	Copper detected	RO	Copper detected. 0 = Copper is not active. 1 = Copper is active.	0
0	Reserved	RO	Ignore on read.	—

2.8.5 User Request 1 Status Register (DEVAD = 30, Address = 0x400E)

Table 191: User Request 1 Status Register (30.0x400E)

Bit	Name	R/W	Description	Default
15:2	Reserved	RO	Reserved	0
1	DON'T_CHANGE_STRAP	RO	0 = Can change strap register 1E.0x401A. 1 = Do not change strap register 1.e.0x401A. **NOTE:** After changing XGPHY disabled bit (1E.0x401A.7)/ SUPER_I (1E.0x401A.15) bit, check register 1E.0x400E bit 1 to be clear before issuing any further MDIO write operation or for any other status bit to be valid.	0
0	Reserved	RO	Reserved	0

2.8.6 Firmware Rev Register (DEVAD = 30, Address = 0x400F)

Table 192: TOP_CONFIG_FW_REV_REG Register (30.0x400F)

Bit	Name	R/W	Description	Default
15:12	FW_VER_BUILD	RO	Firmware version: Build	Set by firmware
11:7	FW_VER_MAIN	RO	Firmware version: Main	Set by firmware
6:0	FW_VER_BRANCH	RO	Firmware Version: Branch	Set by firmware

2.8.7 Firmware Date Register (DEVAD = 30, Address = 0x4010)

Table 193: TOP_CONFIG_FW_DATE_REG Register (30.0x4010)

Bit	Name	R/W	Description	Default
15:14	Reserved	RO	Ignore on read.	Undetermined

Table 193: TOP_CONFIG_FW_DATE_REG Register (30.0x4010) (Continued)

Bit	Name	R/W	Description	Default
13	FW_DATE_YEAR[4]	RO	Year bit4	Set by firmware
12:9	FW_DATE_MONTH	RO	Firmware date: Month	Set by firmware
8:4	FW_DATE_DAY	RO	Firmware date: Day	Set by firmware
3:0	FW_DATE_YEAR[3:0]	RO	Firmware date: Year	Set by firmware

2.8.8 Config Strap Pins Registers (DEVAD = 30, Address = 0x401A)

Table 194: Config Strap Pins Registers (30.0x401A)

Bit(s)	Name	R/W	Description	Default
15:8	Reserved	RO	Reserved.	—
7	Copper disabled	R/W	0: Use the copper device. 1: Do not use the copper device.	FW_Strap[7]
6	Low-power (short reach) mode	RO	0: Disable low TX power short reach mode. 1: Enable low TX power short reach mode.	FW_Strap[6]
5	Pair swap type	RO	0: No cross on even ports. 1: abcd to dcba cross on even ports.	FW_Strap[5]
4	LED control	RO	0: Firmware controls all LEDs except LED4. 1: User controls the LEDs.	FW_Strap[4]
3:0	Reserved	R/W	Reserved.	FW_Strap[3:0]

2.8.9 Strap Pins Registers (DEVAD = 30, Address = 0x401C)

Table 195: Strap Pins Register (30.0x401C)

Bits	Name	R/W	Description	Default
15:9	Reserved	RO	Reserved	—
8	SUPER_I	R/W,	If the SUPER_I strap is high when reset is transitioning from low-to-high, the PHY is placed into super isolate mode and the SUPER_I bit must be cleared. 0: SUPER_I is disabled. 1: SUPER_I is enabled.	Default: SUPER_I STRAP
7:0	Reserved	RO	Reserved	—

2.8.10 SYNC_E Configuration 1 (DEVAD=30, Address = 0x404F)

Table 196: SYNC_E Configuration 1 (30.0x404F)

Bit	Name	R/W	Description	Default
15:5	Reserved	RO	Reserved.	0
4	Enable SYNC_E	R/W	Enables Synchronous Ethernet Clocks onto output pad.	0
3:0	Reserved	RO	Reserved.	0

2.8.11 User Control Register (DEVAD = 30 Address 0x4191)

Table 197: User Control Register (DEVAD = 30 Address 0x4191)

Bit	Name	R/W	Description	Default
15:1	Reserved	RO	Write as 00h, ignore on read.	00h
0	Soft Reset Notify	R/W	Notifies soft reset.	0

2.8.12 SYNC Common CFG Register (DEVAD = 30, Address = 0xA04C)

Table 198: SYNC Common CFG Register (0xA04C)

Bit	Name	R/W	Description	Default
15:10	Reserved	RSVD	Reserved bits write has no effect and read always returns 0.	0
9:4	Reserved	RO	Reserved	0
3	P3_LOCK_STATUS	RO	Lock status bit from Port 3.	0x0
2	P2_LOCK_STATUS	RO	Lock status bit from Port 2.	0x0
1	P1_LOCK_STATUS	RO	Lock status bit from Port 1.	0x0
0	P0_LOCK_STATUS	RO	Lock status bit from Port 0.	0x0

2.8.13 MDIO Control 0 Register (DEVAD = 30, Address = 0x4110)

Table 199: MDIO Control 0 Register (30.0x4110)

Bit	Name	R/W	Description	Default
15:0	MDIO_CONTROL_0	R/W	See Section 2.2, Register Maps, for details.	0

2.8.14 MDIO Control 1 Register (DEVAD = 30, Address = 0x4111)

Table 200: MDIO Control 1 Register (30.0x4111)

Bit	Name	R/W	Description	Default
15:0	MDIO_CONTROL_1	R/W	See Section 2.2, Register Maps, for details.	0

2.8.15 MDIO Control 2 Register (DEVAD = 30, Address = 0x4112)

Table 201: MDIO Control 2 Register (30.0x4112)

Bit	Name	R/W	Description	Default
15:0	MDIO_CONTROL_2	R/W	See Section 2.2, Register Maps, for details.	0

2.8.16 MDIO Control 3 Register (DEVAD = 30, Address = 0x4113)

Table 202: MDIO Control 3 Register (30.0x4113)

Bit	Name	R/W	Description	Default
15:0	MDIO_CONTROL_3	R/W	See Section 2.2, Register Maps, for details.	0

2.8.17 MDIO Control 4 Register (DEVAD = 30, Address = 0x4114)

Table 203: MDIO Control 4 Register (30.0x4114)

Bit	Name	R/W	Description	Default
15:0	MDIO_CONTROL_4	R/W	See Section 2.2, Register Maps, for details.	0

2.8.18 MDIO Control 5 Register (DEVAD = 30, Address = 0x4115)

Table 204: MDIO Control 5 Register (30.0x4115)

Bit	Name	R/W	Description	Default
15:0	MDIO_CONTROL_5	R/W	See Section 2.2, Register Maps, for details.	0

Chapter 3: Pin Descriptions

3.1 I/O Pin Assignments and Descriptions

The table below shows the conventions used to identify the I/O types. The I/O pin type is useful in referencing DC pin characteristics.

Table 205: I/O Signal Type Definitions

Abbreviation	Description
A	Analog pin type
B	Bias pin type
DNC	Do not connect
GND	Ground pin
I	Input
I_{CS}	Input, continuously sampled
I_{PD}	Input with internal pull-down resistor
I_{PU}	Input with internal pull-up resistor
I_{SOR}	Input sampled on reset
I_{ST}	Schmitt trigger input
I_{XT}	Input crystal pin type
I/O	Bidirectional
NC	No connect
O	Output
O_D	LVCMOS output
O_{OC}	Open-collector output
O_{OT}	Output tristate signal
O_{PU}	Pull-up output
PWR	Power pin
S	SGMII/SerDes pin type
All I/O pins have 1.8V as reference voltage unless otherwise specified.	

Table 206: Ball Descriptions

Label	Type	Description
Media Connections		
TRD[0]+	A	**Transmit/Receive Pairs**. In 10GBASE-T, 5GBASE-T, 2.5GBASE-T, and 1000BASE-T mode, differential data from copper media is transmitted and received on all four signal pairs. In auto-negotiation and 100BASE-TX modes, the PHY normally transmits on TRD[0]± and receives on TRD[1]±.
TRD[0]–	A	
TRD[1]+	A	
TRD[1]–	A	
TRD[2]+	A	
TRD[2]–	A	
TRD[3]+	A	
TRD[3]–	A	
Clock		
XTAL_N	I_{XT}	Reference Clock Inputs. These pins accept the clock base on the configuration settings of XTAL_Bypass pins. A continuous 50 MHz (or 156.25 MHz) reference clock must be supplied to the PHY. When XTAL_BP pin is low, apply a 50 MHz crystal oscillator only.
XTAL_P	I_{XT}	
Sync Ethernet		
SYNCECLK/ PRTAD[3]	O	Synchronous Ethernet Recovered Clock0. This pin provides a 25 MHz recovered clock signal that is synchronous to the incoming Ethernet signal on the device. PRTAD[3] is sampled when reset is transitioning from low-to-high. PRTAD provides the MDIO PHY address the device accesses on the first port.
SYNCELOCK/ PRTAD[2]	O	Synchronous Ethernet Lock0. PRTAD[2] is sampled when reset is transitioning from low-to-high. PRTAD provides the MDIO PHY address the device accesses on the first port.
IEEE 1588		
SYNC_IN0	I_{PD}	Sync Input 0. This is the SyncIn0 input signal used in IEEE 1588.
SYNC_IN1_OUT	I_{PD}, O	Bidirectional I/O signal: {Sync Input 1 or Sync Output} This port can be provisioned (through register writes) as the SyncIn1 input signal, or as the SyncOut output signal used in IEEE 1588. After reset, this pin is set as input (SyncIn1).
PTP_XTALN	I_{PD}	PTP Clock Input.
PTP_XTALP	I_{PD}	
XFI		
RDN	I, Internally biased differential CMOS, AC-coupled internally	XFI/10GBASE-KR, USXGMII, 5000BASE-R, 2500BASE-R, 5000BASE-X, 2500BASE-X, and 1000BASE-X (SGMII) Receive Serial Data. Differential input data.
RDP		
TDN	O, differential CMOS, AC-coupled externally	XFI/10GBASE-KR, USXGMII, 5000BASE-R, 2500BASE-R, 5000BASE-X, 2500BASE-X, and 1000BASE-X (SGMII) Transmit Serial Data. Differential output data.
TDP		
SPI Interface		
SPI_MISO	I_{PD}	The PHY latches in data from the SPIROM on the rising edge.

Table 206: Ball Descriptions (Continued)

Label	Type	Description
SPI_MOSI	O_{OT}	Serial Data Input. The PHY latches in data from the ROM on the rising edge.
SPI_SCK	O_{OT}	Serial Clock. Output pin. Clock signal that synchronizes communication between the PHY and a memory device.
SPI_CSB/ XTALBP	$O_{OT, PU}$	ROM Chip Select. A low level on this pin selects the memory device, while a high level deselects the device. XTALBP is a shared signal with SPI_CSB. If XTALBP is high while reset is transitioning from low-to-high, the reference clock is configured for the oscillator/system clock. If low, the reference clock is configured for crystal mode.
MDIO Interface		
MDC	I_{PD}	Management Data Clock for Port. The MDC clock input must be provided to allow MII management functions.
MDIO	$I/O_{PU, D}$	Management Data I/O for Port. This serial input/output bit reads from and write to the MII registers. The data value on the MDIO pin is valid and latched on the rising edge of MDC.
PRTAD[0]	I/O_{PU}	Port Address or PHY Address. Using these pins sets the Port Address values for all single ports. PRTAD[4:0] is sampled when reset is transitioning from low-to-high. PRTAD provides the MDIO PHY address the device accesses on the first port. **NOTE:** Only add an external pull-up or pull-down on the PRTAD[0] signal. This signal is an output after reset.
RESET		
RESETn	$I_{PU, CS, ST}$	Reset. Active-low, RESET is Schmitt Trigger Input. The RESET signal resets the BCM84891L. The BCM84891L requires a hardware reset prior to normal operation. Configuration settings obtained through Hardware Strap Option pins are latched on the rising edge of RESET. Latched on the rising edge of RESET.
LED		
LED1/PRTAD[1]	O_{OT}	Status LED1. Active-Low. Port Address or PHY Address. Using these pins sets the Port Address values for all single ports. PRTAD[1] is sampled when reset is transitioning from low-to-high. PRTAD provides the MDIO PHY address the device accesses on the first port. **NOTE:** PRTAD[1] is a shared signal. Only add an external pull-up or pull-down on the PRTAD[1] signal. This signal is an output after reset.
LED2/ REFCLK_SEL	O_{OT}	Status LED2. Active-Low. Select Reference Clock. Active-high. Pulling this pin high enables the XTAL_N/P inputs to select a 156.25 MHz reference input source. Pulling this pin low enables a 50 MHz reference clock input source. **NOTE:** REFCLK_SEL is a shared signal. Only add an external pull-up or pull-down on the REFCLK_SEL signal. This signal is an output after reset.
LED3/PRTAD[4]	O_{OT}	Status LED3. Active-Low. Port Address or PHY Address. Using these pins sets the Port Address values for all single ports. PRTAD[4] is sampled when reset is transitioning from low-to-high. PRTAD provides the MDIO PHY address the device accesses on the first port. **NOTE:** PRTAD[4] is a shared signal. Only add an external pull-up or pull-down on the PRTAD[4] signal. This signal is an output after reset.
LED4	O_{OT}	Status LED4. Active-Low.
LED5/SUPER_I	O_{OT}	Status LED5. Active-Low. When this signal is active, the device is placed into super isolation. **NOTE:** Super Isolate is a shared signal. Only add an external pull-up or pull-down on the SUPER_I signal. This signal is an output after reset.

Table 206: Ball Descriptions (Continued)

Label	Type	Description
Interrupts		
INTERR_MLC/ CONFIG13	O_D	Dual-function signal. INTERR_MLC. Dedicated Interrupt Pin. Indicates an interrupt on port 0. This signal is active-low. CONFIG13. When this bit is high, the PHY firmware is loaded from SPIROM. When this pin is low, PHY firmware is loaded from the MDIO interface and no external SPIROM is used. Use this register for monitoring purposes only. Use read-modify-write to not change the current value of this register bit during write. **NOTE:** CONFIG13 is a shared signal. Only add an external pull-up or pull-down on the CONFIG13 signal. This signal is an output after reset.
JTAG		
TCK	I	Test Clock. JTAG serial clock.
TDI	$I_{PU, CS}$	Test Data Input. JTAG serial data input.
TDO	O_{OT}	Test Data Output. JTAG serial data output.
TMS	I_{PU}	Test Mode Select. JTAG mode select input.
TRST	$I_{PU, CS}$	JTAG Reset. Active-low. Resets the JTAG controller. This signal must be pulled low during normal operation.
Power Regulation		
DVDD	PWR	Digital Core Voltage. 0.8V ±5%
Analog		
RDAC	B	RDAC Bias Resistors. Adjusts the reference current of the transmitter DAC. A 6.04k ±1% resistor is connected between RDAC and GND.
RCALP	A	Resistor CAL. Place a 4.53k ±1% between RCALP and GND (for RDN/P and TDN/P).
Power and Ground		
VDDIO2	PWR	PWR VDD for MDIO and MDC digital Interface. 1.2V or 2.5V ±5%
VDDIO1	PWR	VDD Supply. The VDD supply for all digital I/O interfaces, except the MDIO/MDC. Connect this supply pins to a 1.88V ±3% source.
VDDIOL	PWR	VDD Supply. VDDIOL supply for the LED pin. 3.3V or 2.5V **NOTE:** When the LED output is not used, VDDIOL can be 1.88V.
PVDDL	PWR	PLL VDD. Connect to +0.8V
AVDDH	PWR	AVDD High. 1.88V ±3%
AVDDL	PWR	AVDD Low. 0.8V ±5%
XFIVDD	PWR	XFI VDD. 0.8V ±5%
XFI_PVDD	PWR	XFI PVDD. 0.8V ±5%
GND	GND	Analog/digital ground

NOTE: All digital I/O pins, except MDIO/MDC, support 1.8V signaling (powered by VDDIO1 = 1.88V).

- MDIO/MDC pins support 3.3V, 2.5V, 1.8V, or 1.2V signaling, based on VDDIO2 power rail voltage level. MDIO/MDC pins are 3.3V tolerant when VDDIO2=2.5V.
- All other digital I/O signals are 1.8V signaling and do not tolerate 2.5V except for specific instances indicated in the pin description.

3.2 Pin List

3.2.1 Pin List by Ball Number

Ball	Signal
A1	GND
A2	MDC
A3	GND
A4	RDN
A5	RDP
A6	GND
A7	TDN
A8	TDP
A9	GND
B1	VDDIO2
B2	MDIO
B3	GND
B4	GND
B5	XFI_PVDD
B6	RCALP
B7	XFIVDD
B8	XFIVDD
B9	GND
C1	TCK
C2	SYNCELOCK/ PRTAD[2]
C3	TDI
C4	GND
C5	GND
C6	RESETn
C7	TRST
C8	TMS
C9	PTP0_XTALN
D1	LED1/PRTAD[1]
D2	SYNC_IN0
D3	VDDIO1
D4	DVDD
D5	GND
D6	DVDD
D7	GND
D8	SYNCECLK/ PRTAD[3]
D9	PTP0_XTALP

Ball	Signal
E1	LED2/ REFCLK_SEL
E2	PRTAD[0]
E3	SPI_SCK
E4	GND
E5	DVDD
E6	GND
E7	SPI_CSB/ XTALBP
E8	INTERR_MLC/ CONFIG13
E9	SYNC_IN1_OUT
F1	LED5/SUPER_I
F2	LED4
F3	LED3/PRTAD[4]
F4	DVDD
F5	GND
F6	GND
F7	SPI_MISO
F8	SPI_MOSI
F9	TDO
G1	VDDIOL
G2	AVDDH
G3	AVDDH
G4	AVDDL
G5	GND
G6	DNC
G7	RDAC
G8	DNC
G9	DNC
H1	GND
H2	TRD[0]–
H3	TRD[1]–
H4	TRD[2]+
H5	TRD[3]–
H6	GND
H7	XTAL_P
H8	DNC

Ball	Signal
H9	PVDDL
J1	GND
J2	TRD[0]+
J3	TRD[1]+
J4	TRD[2]–
J5	TRD[3]+
J6	GND
J7	XTAL_N
J8	DNC
J9	GND

3.2.2 Pin List by Signal Name

Signal	Ball
AVDDH	G2
AVDDH	G3
AVDDL	G4
DNC	G6
DNC	G8
DNC	G9
DNC	H8
DNC	J8
DVDD	D4
DVDD	D6
DVDD	E5
DVDD	F4
GND	A1
GND	A3
GND	A6
GND	A9
GND	B3
GND	B4
GND	B9
GND	C4
GND	C5
GND	D5
GND	D7
GND	E4
GND	E6
GND	F5
GND	F6
GND	G5
GND	H1
GND	H6
GND	J1
GND	J6
GND	J9
INTERR_MLC/ CONFIG13	E8
LED1/PRTAD[1]	D1
LED2/ REFCLK_SEL	E1
LED3/PRTAD[4]	F3
LED4	F2

Signal	Ball
LED5/SUPER_I	F1
MDC	A2
MDIO	B2
PRTAD[0]	E2
PTP0_XTALN	C9
PTP0_XTALP	D9
PVDDL	H9
RDAC	G7
RDN	A4
RDP	A5
RCALP	B6
RESETn	C6
SPI_CSB/ XTALBP	E7
SPI_MISO	F7
SPI_MOSI	F8
SPI_SCK	E3
SYNC_IN0	D2
SYNC_IN1_OUT	E9
SYNCECLK/ PRTAD[3]	D8
SYNCELOCK/ PRTAD[2]	C2
TCK	C1
TDI	C3
TDN	A7
TDO	F9
TDP	A8
TMS	C8
TRD[0]–	H2
TRD[0]+	J2
TRD[1]–	H3
TRD[1]+	J3
TRD[2]–	J4
TRD[2]+	H4
TRD[3]–	H5
TRD[3]+	J5
TRST	C7
VDDIO1	D3
VDDIO2	B1
VDDIOL	G1

Signal	Ball
XFI_PVDD	B5
XFIVDD	B7
XFIVDD	B8
XTAL_N	J7
XTAL_P	H7

3.3 Pinout Diagram

Figure 18: Pinout Diagram

	1	2	3	4	5	6	7	8	9	
A	GND	MDC	GND	RDN	RDP	GND	TDN	TDP	GND	A
B	VDDIO2	MDIO	GND	GND	XFI_PVDD	RCALP	XFIVDD	XFIVDD	GND	B
C	TCK	SYNCELOCK	TDI	GND	GND	RESETn	TRST	TMS	PTP0_XTALN	C
D	LED1/PRTAD[1]	SYNC_IN0	VDDIO1	DVDD	GND	DVDD	GND	SYNCECLK	PTP0_XTALP	D
E	LED2/ REFCLK_SEL	PRTAD[0]	SPI_SCK	GND	DVDD	GND	SPI_CSB/ XTALBP	INTERR_MLC/ CONFIG13	SYNC_IN1_OUT	E
F	LED5/SUPER_I	LED4	LED3/PRTAD[4]	DVDD	GND	GND	SPI_MISO	SPI_MOSI	TDO	F
G	VDDIOL	AVVDH	AVDDH	AVDDL	GND	DNC	RDAC	DNC	DNC	G
H	GND	TRD[0]–	TRD[1]–	TRD[2]+	TRD[3]–	GND	XTAL_P	DNC	PVDDL	H
J	GND	TRD[0]+	TRD[1]+	TRD[2]–	TRD[3]+	GND	XTAL_N	DNC	GND	J
	1	2	3	4	5	6	7	8	9	

Chapter 4: Electrical Characteristics

4.1 Parameters and Timing

CAUTION! These specifications indicate levels where permanent damage to the device can occur. Functional operation is not guaranteed under these conditions. Operation at absolute maximum conditions for extended periods can adversely affect long-term reliability of the device.

Table 207: Absolute Maximum Ratings

Parameter	Min.	Typ.	Max.	Units
Storage temperature	–45	—	125	°C
Voltage on DVDD with respect to GND	–0.3	—	TBD	V
Voltage on AVDDL, XFIPVDD0 to XFIPVDD7, XFIVDD, and XFIVDDP with respect to GND.	–0.5	—	TBD	V
Voltage on AVDDH, XFIVDDH0 to XFIVDDH4 with respect to GND	–0.5	—	TBD	V
VDDIO	–0.5	—	TBD	V
VDDIOM	–0.5	—	TBD	V
VDDIOL	–0.5	—	TBD	V
CMOS sink current	—	—	20	mA

Table 208: Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Ambient temperature under bias	—	—	0	25	70	°C
Ambient temperature ramp rate	—	—	—	—	2	°C/min
Supply voltages on DVDD (XFI-to-copper)	—	—	0.76	0.8	0.84	V
Supply voltages on XFIVDD, XFIPLLVDD, and APLLVDD	—	—	0.76	0.8	0.84	V
Supply voltage on AVDDL	—	—	0.76	0.8	0.84	V
Supply Voltage on AVDDH	—	—	1.8236	1.88	1.9364	V
Supply Voltage on PVDDL	—	—	0.76	0.8V	0.84	V
Supply Voltage on VDDIO1	—	—	1.8236	1.88	1.9364	V
Supply voltage on VDDIO2	—	2.5	2.375	2.5	2.625	V
	—	1.2	1.14	1.2	1.26	V
	—	1.88	1.8236	1.88	1.9364	V
Ground voltage (GND)	—	—	—	0	—	V
Reference clock frequency	—	—	—	50	—	MHz
	—	—	—	156.25	—	MHz
Reference clock frequency tolerance asynchronous	—	—	–50	—	50	ppm
Reference clock input voltage swing differential pk-pk	—	—	500	—	2000	mVppd
Reference clock duty cycle	—	—	40	—	60	%
NOTE: Device specifications, unless otherwise noted, are guaranteed under the recommended operating conditions of Table 208. **NOTE:** Customer can select (through REFCLK_SEL pin) between two reference clock frequencies 50 MHz and 156.25 MHz. The crystal oscillator option only supports 50 MHz (XTAL_BP is set to low).						

Table 208: Recommended Operating Conditions (Continued)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Reference clock rise and fall times	—	20% to 80% of amplitude	—	—	0.5	ns for every 500 mV ppd
Reference clock jitter (from 80 Hz to 20 MHz)	—	—	—	—	See Jitter Mask (Figure 19 and Figure 20).	
Differential input termination resistance (external)	R_{DIFF}	—	—	—	Hi-Z	Ω
PTP clock frequency	—	—	—	125	—	MHz
PTP clock frequency tolerance	—	—	–100	—	+100	ppm
PTP clock duty cycle	—	—	40	—	60	%
PTP clock rise and fall times	—	20% to 80% of amplitude	—	—	0.5	ns for every 500 mV ppd

NOTE: Device specifications, unless otherwise noted, are guaranteed under the recommended operating conditions of Table 208.

NOTE: Customer can select (through REFCLK_SEL pin) between two reference clock frequencies 50 MHz and 156.25 MHz. The crystal oscillator option only supports 50 MHz (XTAL_BP is set to low).

Figure 19: 156.25 MHz Reference Clock Jitter Mask

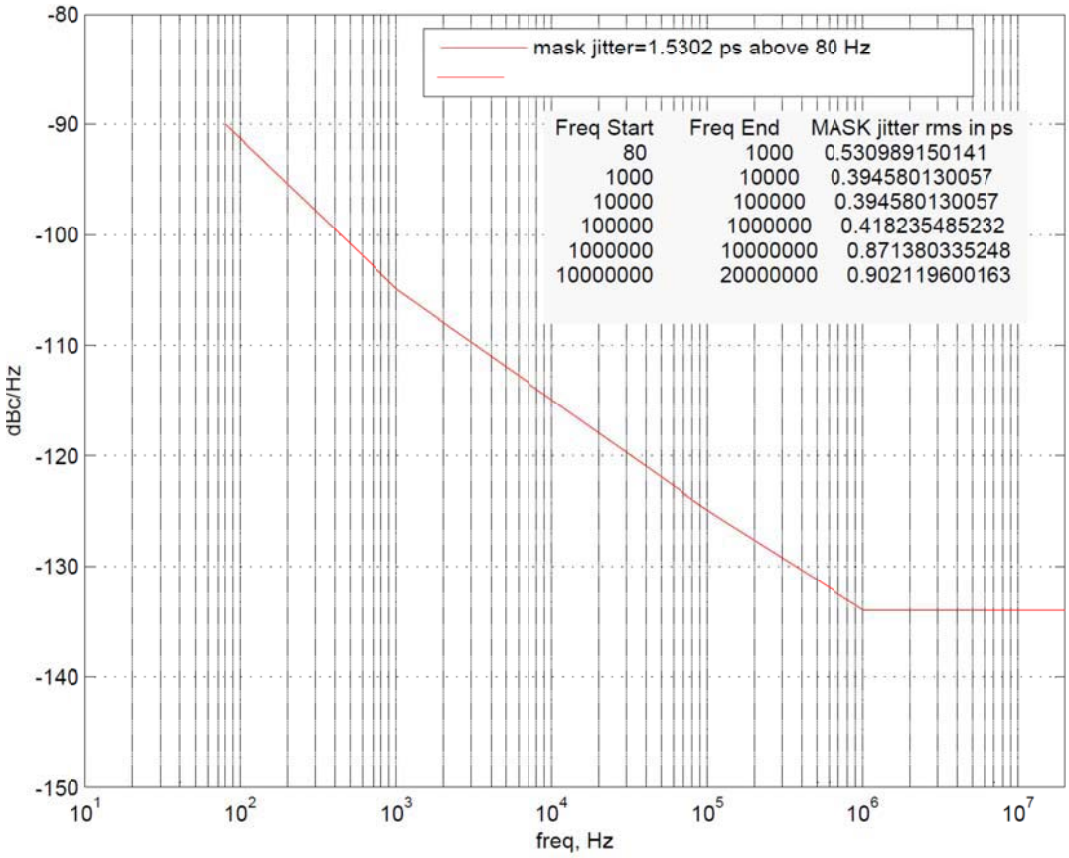


Figure 20: 50 MHz Reference Clock Jitter Mask

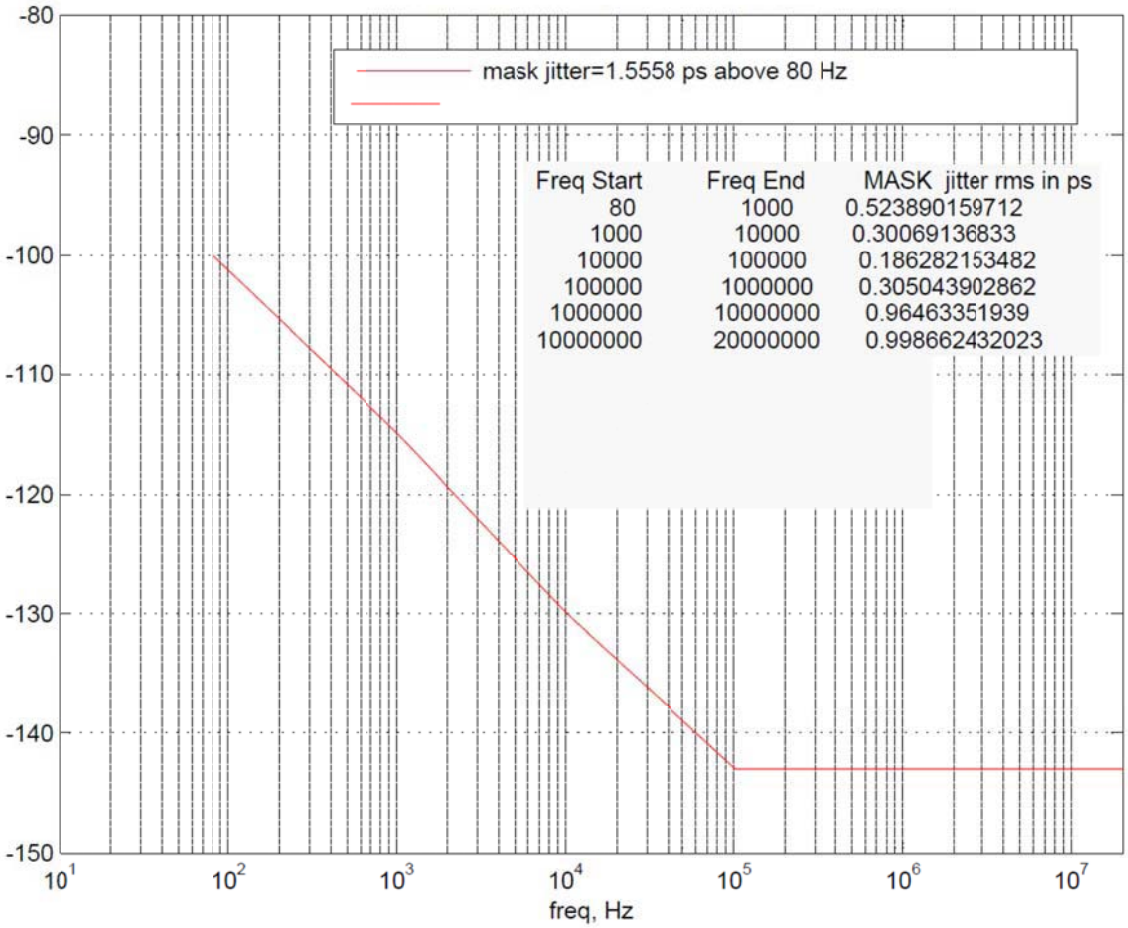
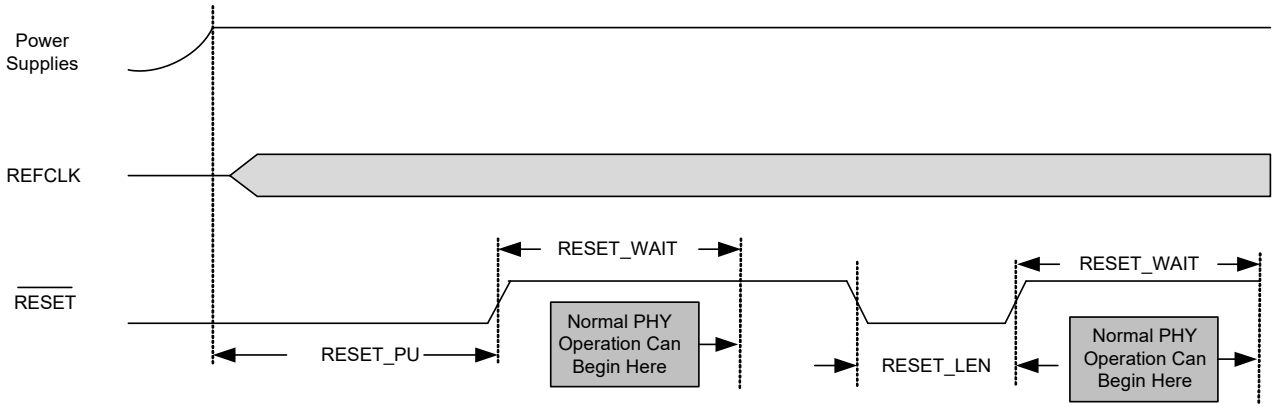


Figure 21: Recommended Operating Conditions



4.2 Reset Timing

Table 209: Reset Timing

Parameter	Symbol	Min.	Typ.	Max.	Units
Power-up to RESET deassertion	RESET_PU	4	—	—	ms
RESET deassertion to normal PHY operation	RESET_WAIT	—	—	—	ms
RESET pulse length	RESET_LEN	2	—	—	µs

NOTE:

- RESET_WAIT timing is based on 4 Mb of code loading from SPIROM into the BCM84891L, plus the internal initialization time (SPRIOM speed should be 31.25 MHz or faster). Timing is based on one SPIROM per two ports.
- When RESET is low, there must be a valid clock signal at the XTALI input and all external power supplies must be stable.
- MDIO register read/write access and normal PHY operation can start at the end of RESET_WAIT time.
- RESET_PU must be performed when the device is first powered up. Software reset or RESET_LEN does not need to be performed after RESET_PU.
- Software reset or RESET_LEN should not be performed until after RESET_PU and RESET_WAIT have been completed. After issuing a RESET_LEN, normal PHY operation can commence after completion of RESET_WAIT time.
- For Reset timing of SHARED_SPIROM mode details, refer to the *Design Guidelines for SerDes Transceivers* application note (document number: SerDes-AN1xx-R).

Figure 22: Clock Input Receiver

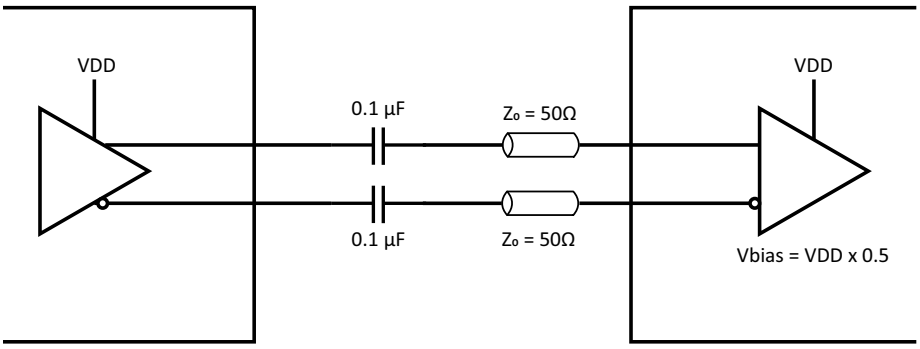


Table 210: MDC and MDIO AC Characteristics

Parameters	Symbol	Conditions	Min.	Typ.	Max.	Units
MDIO output propagation delay after rising edge of MDC	t_{C2D}	Pull-up voltage = 1.2V R = 500Ω, C = 50 pF	—	—	25	ns
		Pull-up voltage = 1.2V R = 10 kΩ, C = 50 pF	—	—	25	ns
MDIO output from driven to high-impedance after rising edge of MDC	t_{D2Z}	Pull-up voltage = 1.2V R = 500Ω, C = 50 pF	—	—	20	ns
		Pull-up voltage = 1.2V R = 10 kΩ, C = 50 pF	—	—	100	ns
MDC frequency	$MDC_{Frequency}$	Pull-up voltage = 1.2V R = 500Ω, C = 50 pF	—	—	25	MHz
		Pull-up voltage = 1.2V R = 10 kΩ, C = 50 pF	—	—	0.4	MHz
MDC duty cycle	t_{CKH}/t_{CK}	—	30	—	70	%
MDIO input setup time to the rising edge of MDC	t_{DIS}	—	10	—	—	ns

Table 210: MDC and MDIO AC Characteristics (Continued)

Parameters	Symbol	Conditions	Min.	Typ.	Max.	Units
MDIO input hold time after the rising edge of MDC	t_{DIH}	—	5	—	—	ns

Figure 23: MDC and MDIO Timing Waveforms

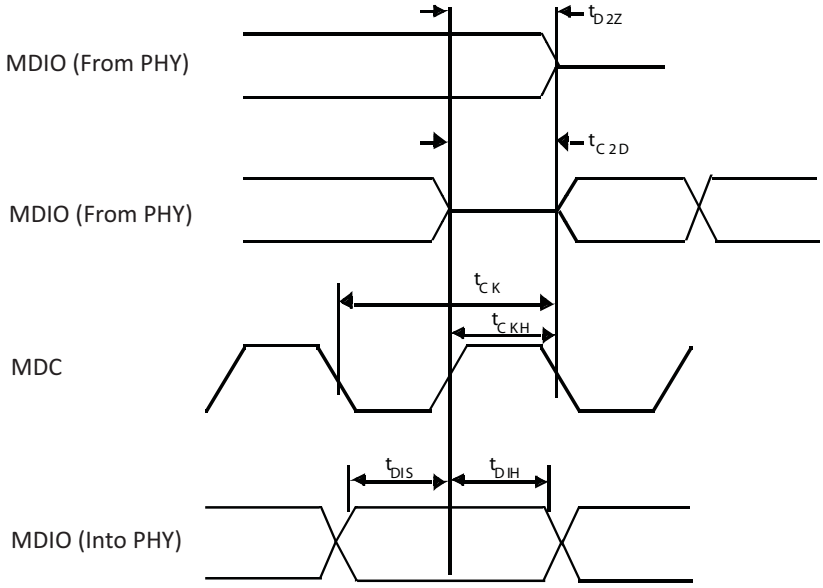


Table 211: 1.2V CMOS Output DC Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
CMOS output low voltage	V_{OL}	VDDIO2 = 1.2V, IOL = 2 mA	–0.3	—	0.2	V
CMOS output high voltage	V_{OH}	VDDIO2 = 1.2V, IOH = –2 mA	VDDIO2 – 0.2V	—	1.5	V

Table 212: 1.2V CMOS Input DC Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
CMOS input low voltage	V_{IL}	VDDIO2 = 1.2V	–0.3	—	0.35 VDDIO2	V
CMOS input high voltage	V_{IH}	VDDIO2 = 1.2V	0.65 VDDIO2	—	1.5	V
Input low current	I_{IL}	—	—	—	–5	µA
Input high current	I_{IH}	—	—	—	5	µA
NOTE: T_A = 0°C to +70°C, unless otherwise noted.						

Table 213: 1.8V CMOS Output DC Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
CMOS output low voltage	V_{OL}	VDDIO1 = 1.8V VDDIO1 = 1.8V IOL = 6 mA	0.00	—	0.45	V
CMOS output high voltage	V_{OH}	VDDIO1 = 1.8V VDDIO1 = 1.8V IOH = –6 mA	VDDIO1 – 0.45V	—	1.8	V
NOTE: T_A = 0°C to +70°C, unless otherwise noted.						

Table 214: 1.8V CMOS Input DC Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
CMOS input low voltage	V_{IL}	VDDIO1 = 1.8V	–0.3	—	0.35 VDDIO1	V
CMOS input high voltage	V_{IH}	VDDIO1 = 1.8V	0.65 VDDIO1	—	VDDIO1 + 0.3V	V
Input low current	I_{IL}	—	—	—	–80	µA
Input high current	I_{IH}	—	—	—	5	µA
NOTE: T_A = 0°C to +70°C, unless otherwise noted.						

Table 215: 2.5V CMOS Output DC Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
CMOS output low voltage	V_{OL}	VDDIO2 = 2.5V VDDIO2 = 2.5V IOL = 6 mA	0.00	—	0.4	V
CMOS output high voltage	V_{OH}	VDDIO2 = 2.5V VDDIO2 = 2.5V IOH = –6 mA	VDDIO2 – 0.4V	—	2.5	V
NOTE: T_A = 0°C to +70°C, unless otherwise noted.						

Table 216: 2.5V CMOS Input DC Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
CMOS input low voltage	V_{IL}	VDDIO2 = 2.5V	0.00	—	0.70	V
CMOS input high voltage	V_{IH}	VDDIO2 = 2.5V	1.7	—	2.5	V
Input low current	I_{IL}	—	—	—	–80	µA
Input high current	I_{IH}	—	—	—	5	µA
NOTE: T_A = 0°C to +70°C, unless otherwise noted.						

Table 217: XFI Transmitter Performance Specifications

Parameter	Conditions	Min.	Typ.	Max.	Units
Nominal VCO center frequency	—	—	10.3125	—	GHz
Total jitter	Refer to *XFI INF-8077i*.	—	—	0.61	UI
Total non-EQJ Jitter	Refer to *XFI INF-8077i*.	—	—	0.41	UI
Eye mask	X1	—	—	0.305	UI
Eye mask	Y1	60	—	—	mV
Eye mask	Y2	—	—	410	mV

Figure 24: XFI Far-End Eye Mask

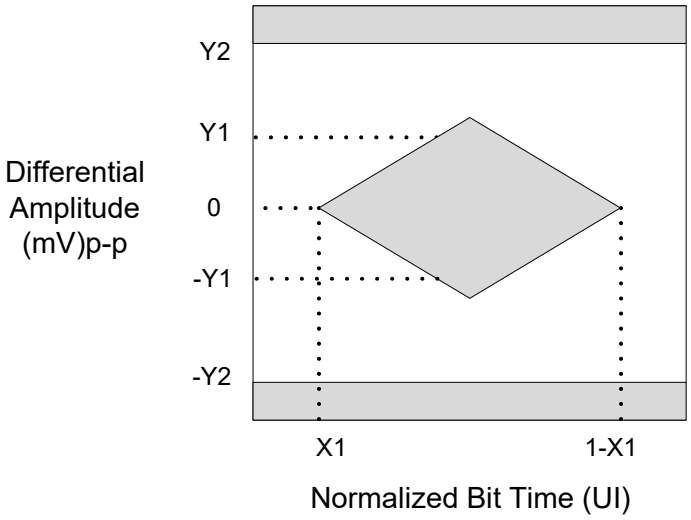


Table 218: XFI Differential CMOS Data Output

Parameter	Conditions	Min.	Typ.	Max.	Units
Reference differential impedance	—	—	100	—	Ω
Termination mismatch	—	—	—	5	%
Output rise and fall time (20% to 80%)	Refer to the XFI specification.	20	—	—	ps
Output AC common mode voltage	—	—	—	15	mV (RMS)
Output rise and fall time (20% to 80%)	Refer to the XFI specification.	20	—	—	ps

Table 219: XFI Receiver Input Performance Specifications

Parameter	Conditions	Min.	Typ.	Max.	Units
Total jitter	Refer to the XFI specification.	—	—	0.65	UI (p-p)
Total non-EQJ jitter	Refer to the XFI specification.	—	—	0.45	UI (p-p)
Sinusoidal jitter tolerance	Sinusoidal jitter tolerance for datacom. See Figure 25.	—	—	—	—
Eye mask X1	Mask coordinate X1 = 0.225 if total non-EQJ jitter is measured.	—	—	0.325	UI
Eye mask Y1	—	55	—	—	mV

Table 219: XFI Receiver Input Performance Specifications (Continued)

Parameter	Conditions	Min.	Typ.	Max.	Units
Eye mask Y2	Out of 525 mV, 100 mV is allocated for multiple reflection.	—	—	525	mV

Figure 25: Receiver Input Sinusoidal Jitter Tolerance

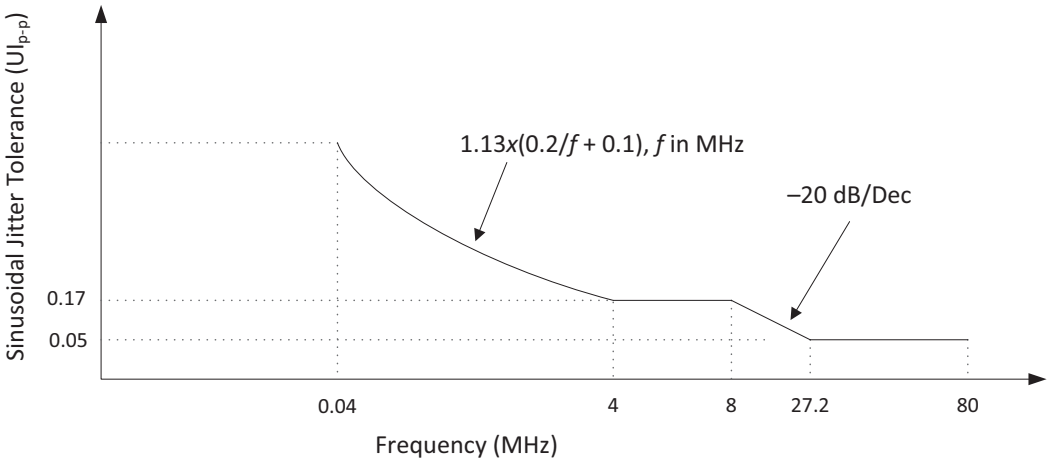


Table 220: XFI Differential CMOS Data Input

Parameter	Conditions	Min.	Typ.	Max.	Units
Reference differential impedance	—	80	100	120	Ω
Termination mismatch	—	—	—	5	%

Chapter 5: Thermal Characteristics

5.1 Package

This section includes thermal information for the BCM84891L (81-pin package). Table 221 and Table 222 provide a comparison of ThetaJA versus airflow, along with ThetaJB and ThetaJC. The BCM84891L is designed and rated for a maximum junction temperature of 110°C.

Table 221: $Theta_{JA}$ Versus Airflow for T_A = 70°C

Package	Airflow (Feet Per Minute)				
	0	100	200	400	600
$Theta_{JA}$ (°C/W) with external heat sink (with heat spreader)[a]	23.44	17.45	15.23	13.42	12.43

a. Heat sink size: 19 mm × 19 mm × 10 mm with airflow of 100 LFPM.

Table 222: $Theta_{JB}$ and $Theta_{JC}$ Values for T_A = 70°C

Package	°C/W
$Theta_{JB}$ (°C/W) with heat spreader	14.90
$Theta_{JC}$ (°C/W) with heat spreader	1.44

5.2 External Heat Sink and Thermal Interface

Table 223: External Heat Sink and Thermal Interface

Package	Description
Heat sink and dimension	19 mm × 19 mm × 10 mm fin type heat sink aluminum, k = 205 (W/m × K), epsilon = 0.8
Thermal interface	SE4450, 0.1 mm thick, k = 1.97 (W/m × K)

NOTE: Refer to the *Heat Sink Attachment and Rework Guidelines Using Thermal Epoxy* application note (PACKAGING-AN7xx-R) for information on heat sink attachment and rework guidelines using thermal epoxy.

5.3 Junction Temperature Estimation and Psi_{JT} Versus $Theta_{JC}$ Overview

Package thermal characterization parameter Psi_{JT} (Ψ_{JT}) yields a better estimation of actual device junction temperature (T_J) versus using the junction-to-case thermal resistance parameter $Theta_{JC}$ (θ_{JC}). The reason for this is that θ_{JC} assumes that all the power is dissipated through the top surface of the package case. In actual applications, some of the power is dissipated through the bottom and sides of the package. Ψ_{JT} takes into account power dissipated through the top, bottom, and sides of the package. The equation for calculating the device junction temperature is as follows:

$$T_J = T_T + P \cdot \Psi_{JT}$$

Where:

- T_J = Junction temperature at steady-state condition, °C.
- T_T = Package case top center temperature at steady-state condition, °C.
- P = Device power dissipation, Watts.
- Ψ_{JT} = Package thermal characteristics (no airflow), °C/W.

Table 224: Psi_{JT} Values T_A = 70°C

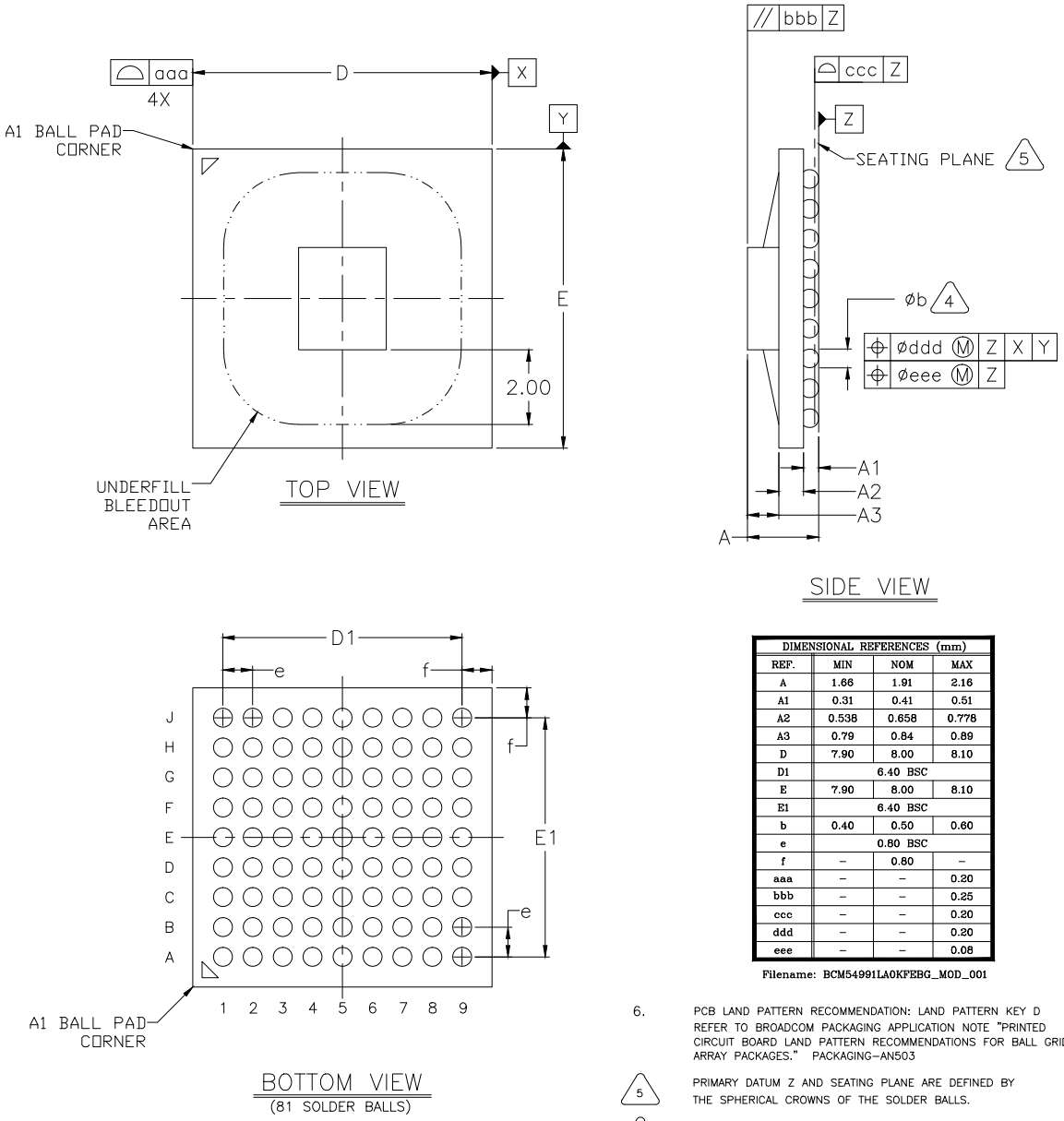
	Airflow (Feet Per Minute)				
Package	**0**	**100**	**200**	**400**	**600**
Psi_{JT} (°C/W) with external heat sink (with head spreader)[a]	0.89	1.01	1.06	1.09	1.10

a. Heat sink size: 19 mm × 19 mm × 10 mm.

Chapter 6: Mechanical Information

6.1 Package Outline

Figure 26: BCM84891LA0KFSBG/BCM84891LA0IFSBGOutline Drawing (8 mm × 8 mm Package)



DIMENSIONAL REFERENCES (mm)			
REF.	MIN	NOM	MAX
A	1.66	1.91	2.16
A1	0.31	0.41	0.51
A2	0.538	0.658	0.778
A3	0.79	0.84	0.89
D	7.90	8.00	8.10
D1		6.40 BSC	
E	7.90	8.00	8.10
E1		6.40 BSC	
b	0.40	0.50	0.60
e		0.80 BSC	
f	–	0.80	–
aaa	–	–	0.20
bbb	–	–	0.25
ccc	–	–	0.20
ddd	–	–	0.20
eee	–	–	0.08

Filename: BCM54991LA0KFEBG_MOD_001

6. PCB LAND PATTERN RECOMMENDATION: LAND PATTERN KEY D REFER TO BROADCOM PACKAGING APPLICATION NOTE "PRINTED CIRCUIT BOARD LAND PATTERN RECOMMENDATIONS FOR BALL GRID ARRAY PACKAGES." PACKAGING–AN503

5 PRIMARY DATUM Z AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

4 DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM Z.

3. THE BASIC SOLDER BALL GRID PITCH IS 0.80mm

2. THIS PACKAGE CONFORMS TO THE JEDEC REGISTERED OUTLINE MO–205F.

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994.

NOTES: UNLESS OTHERWISE SPECIFIED

6.2 RoHS-Compliant Packaging

Broadcom offers a RoHS6 package (Pb-free) that is compliant with RoHS6 and WEEE directives. The RoHS6-compliant parts have the letter G added to the top line of the part marking. For the surface-mount process of the Pb-free parts, refer to the *Heat Sink Attachment and Rework Guidelines Using Thermal Epoxy* application note (PACKAGING-AN7xx-R).

Table 225 shows the solder ball composition of the RoHS6-compliant package and the recommended maximum reflow temperature.

Table 225: RoHS6-Compliant Package

Part Number	Solder Ball Composition	Maximum Reflow Temperature (°C)
BCM84891LA0KFEBG	96.5%Sn/3%Ag/0.5%Cu	245°C
BCM84891LA0IFEBG		
BCM84891LB0KFEBG		
BCM84891LB0IFEBG		

Chapter 7: Ordering Information

Table 226: Ordering Information

Part Number	Package	Ambient Temperature
BCM84891LA0KFEBG	81-ball BGA (RoHS-compliant)	0°C to 70°C
BCM84891LA0IFEBG	81-ball BGA (RoHS-compliant)	–40°C to 85°C
BCM84891LB0KFEBG	81-ball BGA (RoHS-compliant)	0°C to 70°C
BCM84891LB0IFEBG	81-ball BGA (RoHS-compliant)	–40°C to 85°C

Glossary

The table below lists the acronyms and abbreviations used in this document.

Table 227: Acronyms and Abbreviations

Term	Description
ADC	Analog-to-digital converter
CRC	Cyclic redundancy check
DAC	Digital-to-analog converter
DFE	Decision-feedback equalization
EEE	Energy Efficient Ethernet
EMI	Electromagnetic Interference
FFE	Feed-forward equalization
GbE	Gigabit Ethernet
ISI	Intersymbol interference
MAC	Media access control
MDI	Medium-dependent interface
PCB	Printed circuit board
PHY	Physical layer
THP	Tomlinson-Harashima Precoder
100BASE-TX	Fast Ethernet at 100 Mb/s (12.5 MB/s) with auto-negotiation using two pairs of Category 5 twisted-pair cable for a distance of up to 100 meters (IEEE 802.3u)
1000BASE-T	Fast Ethernet at 1 Gb/s (125 MB/s) using four pairs of Category 5 twisted-pair cable for a distance of up to 100 meters (IEEE 802.3ab)