ACM8625P 2×33W Stereo | 1×51W Mono, Digital Input Class-D Audio Amplifier with Rich Audio Effect Tuning

1. Features

- Flexible Power Supply Configurations
  - PVDD: 4.5V to 21V
  - DVDD and I/O: 3.3V
- Various output configurations
  - 2×33W, Stereo mode (6Ω, 21V, THD+N = 1%)
  - 1×51W, Mono mode (4Ω, 21V, THD+N = 1%)
- Excellent Audio Performance
  - THD+N ≤ 0.04% at 1W, 1kHz, PVDD = 12V
  - 112 dB A-weighted signal-to-noise ratio (SNR)
  - Idle switching A-weighted noise ≤ $35\ uV_{RMS}$
  - 18 mA low quiescent current
  - 90% efficiency into 6Ω load at 12V
- Configurable digital audio interface
  - I^2C control with up to 4 selectable addresses
  - I^2S, Left-justified, Right-justified, TDM audio format
  - 3-Wire digital audio interface without MCLK required
  - 32kHz, 44.1kHz/48kHz, 88.2kHz/96kHz, 176.4kHz/192kHz input sample rate
  - SDOUT for Acoustic Echo Cancellation – AEC or 1.1 / 2.1 system sub-channel signal routing
- Advanced audio effect tuning
  - Flexible digital and analog gain adjustment
  - High pass filter for DC blocking
  - Input signal router for left and right channel
  - 2×15 pre BQs & 2×5 post BQs to support enhanced audio frequency tuning
  - Pre volume & post volume for dynamic headroom and loudness control
  - 3 band dynamic range control (DRC) with time delay buffer & post compensation BQs for flexible and flat multiple band control
- Analog protections
  - FAULT status report through GPIO and I^2C registers
  - Over current and Direct current protection
  - Over temperature protection
  - Under-voltage and Over-voltage protection
  - Clock error protection

2. Applications

- Portable Speakers: Bluetooth, Smart Speakers with Voice Assistant
- Home Audio: TV, Soundbar, STB (set top box), HTiB (Home Theatre in a Box)
- Smart Appliances
- PCs and Laptops

3. General Description

ACM8625P is a fully integrated, high efficiency, stereo Class-D audio amplifier with digital inputs. The application circuit requires few passives components to operate with 4.5V to 21V PVDD supply, 3.3V DVDD supply. It can drive 2×33W output power into BTL 6Ω and 1×51W into PBTL 4Ω@1% THD+N.

ACM8625P features one novel PWM modulation architecture, which adjusts PWM common duty cycle during start-up phase to avoid startup pop click.

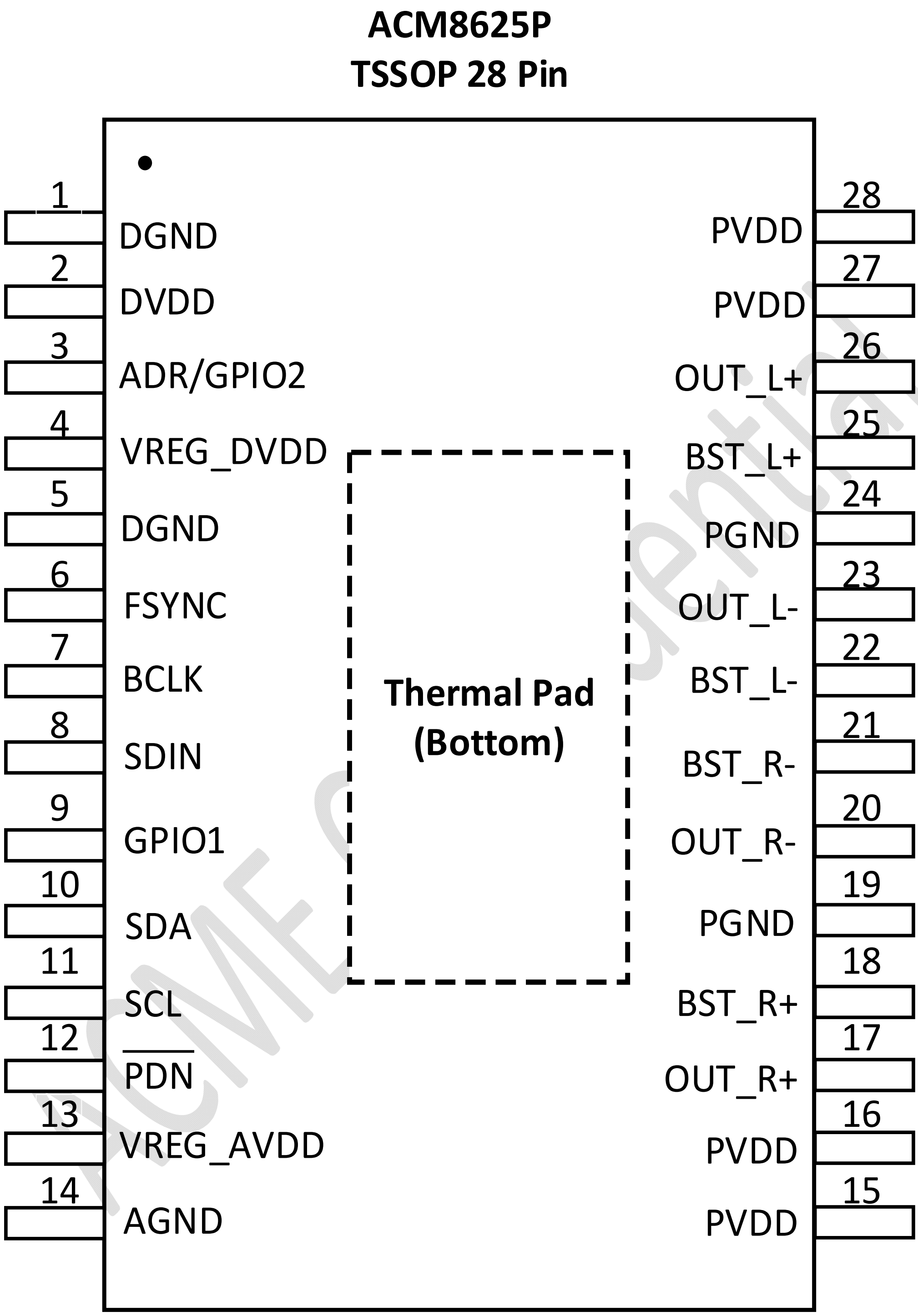
Spread spectrum technology provides lower EMI radiated emissions. It allows inductor free application with specified output power situation with ACM8625P.

The advanced audio effect tuning capability inside ACM8625P provides one highly integrated solution. It allows turning on / off each block with highly free operations. Both pre and pose BQs / volume helps a lot to maintain audio headroom. Furthermore, 3 band DRC with time delay buffer and post compensation BQs is available to implement flexible and flat multiple band control.

4. Device Information

Part number	Package	Body size
ACM8625P	TSSOP 28	9.7 mm × 4.4 mm

5. Pin Configuration and Function Descriptions



Pin No.	Name	Type	Description
1	DGND	PWR	Digital Ground.
2	DVDD	PWR	Digital power supply input: 3.3V.
3	ADR/GPIO2	DIO	I^2C address selection / GPIO2: FAULT / WARNING / SDOUT…

4	VREG_DVDD	AOUT	Digital regulator output.
5	DGND	PWR	Digital Ground
6	FSYNC	DIN	Word select clock for the digital signal.
7	BLCK	DIN	Bit clock for the digital signal.
8	SDIN	DIN	Serial data input.
9	GPIO1	DIO	GPIO1: FAULT / WARNING / SDOUT…
10	SDA	DIO	I^2C serial data.
11	SCL	DIN	I^2C clock.
12	$\overline{PDN}$	DIN	Shut down, low active.
13	VREG_AVDD	AOUT	Analog regulator output.
14	AGND	PWR	Analog ground.
15	PVDD	PWR	Power stage supply input.
16	PVDD	PWR	Power stage supply input.
17	OUT_R+	AOUT	Right channel positive output of H-bridge.
18	BST_R+	AIN	Bootstrap capacitor for OUT_R+.
19	PGND	PWR	Power stage ground.
20	OUT_R-	AOUT	Right channel negative output of H-bridge.
21	BST_R-	AIN	Bootstrap capacitor for OUT_R-.
22	BST_L-	AIN	Bootstrap capacitor for OUT_L-.
23	OUT_L-	AOUT	Left channel negative output of H-bridge.
24	PGND	PWR	Power stage ground.
25	BST_L+	AIN	Bootstrap capacitor for OUT_L+.
26	OUT_L+	AOUT	Left channel positive output of H-bridge.
27	PVDD	PWR	Power stage supply input.
28	PVDD	PWR	Power stage supply input.

6. Device Family Comparison

Device Name	R_{dson}	**PVDD**	**Output Power**
ACM8615M	135 mΩ	4.5V ~ 21V	Mono 1×21W (8Ω, 20V, THD+N = 1%)
ACM8625M	135 mΩ	4.5V ~ 26.4V	Stereo 2×26W (8Ω, 22V, THD+N = 1%)
ACM8625P	75 mΩ	4.5V ~ 21V	Stereo 2×45W (4Ω, 21V, THD+N = 1%)

7. Specifications

7.1 Absolute Maximum Ratings (1)

		MIN	MAX	UNIT
DVDD	Low-voltage digital supply	-0.3	3.9	V
PVDD	PVDD supply	-0.3	28	V
$V_{I(Digin)}$	DVDD referenced digital inputs (2)	-0.5	V_{DVDD}+0.5	V
$V_{I(OUTxx)}$	Voltage at speaker output pins	-0.3	28	V
T_A	Ambient operating temperature	-25	85	℃
T_{stg}	Storage temperature	-40	125	℃

(1) Stressed beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicted under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) DVDD referenced digital pins include: ADR/GPIO2, GPIO3, FSYNC, BCLK, SDIN, GPIO1, SDA, SCL, $\overline{PDN}$.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
$V_{(SUPLLY)}$	Power supply inputs	DVDD	2.8		3.63	V
		PVDD	4.5		21	
	Recommended PVDD Range	BTL Mode, Speaker Load=4Ω (+/-20% Variation)	4.5		21	V
		BTL Mode, Speaker Load=6Ω (+/-20% Variation)	4.5		21	
		BTL Mode, Speaker Load=8Ω (+/-20% Variation)	4.5		21	
		PBTL Mode, Speaker Load=2Ω (+/-20% Variation)	4.5		21	
		PBTL Mode, Speaker Load=3Ω (+/-20% Variation)	4.5		21	
		PBTL Mode, Speaker Load=4Ω (+/-20% Variation)	4.5		21	
$V_{IH(DIGIN)}$	Input logic high for DVDD reference digital inputs		0.9×DVDD		DVDD	V
$V_{IL(DIGIN)}$	Input logic low for DVDD reference digital inputs				0.1×DVDD	
L_{OUT}	Minimal inductor value in LC filter under short-circuit condition		1			μH

7.4 Thermal Information

		ACM8625P TSSOP 28 PINS	UNIT
		JEDEC STANDARD 4-LAYER PCB	
θ_{JA}	Junction-to-ambient thermal resistance	28	℃/W
θ_{JT}	Junction-to-case (top) thermal resistance	22	℃/W
ψ_{JT}	Junction-to-top characterization parameter	1.2	℃/W

7.5 Electrical Characteristics

Free-are room temperature 25° C, High Performance mode, LC filter=10uH+0.68uF, Fsw=480kHz, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL I/O						
|IIH|	Input logic high current level for DVDD referenced digital input pins	$V_{IN(Digin)}=V_{DVDD}$			10	μA
|IIL|	Input logic low current level for DVDD referenced digital input pins	$V_{IN(Digin)}$=0 V			-10	μA
$V_{IH(Digin)}$	Input logic high threshold for DVDD referenced digital inputs		70%			V_{DVDD}
$V_{IL(Digin)}$	Input logic low threshold for DVDD referenced digital inputs				30%	V_{DVDD}
$V_{OH(Digin)}$	Output logic high threshold for DVDD referenced digital inputs	I_{OH} = 2mA	80%			V_{DVDD}
$V_{OL(Digin)}$	Output logic low threshold for DVDD referenced digital inputs	I_{OH} = -2mA			20%	V_{DVDD}
I²C CONTROL PORT						
$C_{L(I2C)}$	Allowable load capacitance for each I²C line				400	pF
$F_{SCL(fast)}$	Support SCL frequency	No wait states, fast mode			400	kHz
$F_{SCL(slow)}$	Support SCL frequency	No wait states, fast mode			100	kHz
SERIAL AUDIO PORT						
t_{DLY}	Required FSYNC to BCLK rising edge delay		5			ns
D_{SCLK}	Allowable SCLK duty cycle		40%		60%	
f_S	Supported input sample rates		32		192	kHz
F_{BCLK}	Supported BCLK frequencies		32		64	f_S
AMPLIFIER OPERATING MODE AND DC PARAMETERS						
t_{OFF}	Turn-off Time	Excluding volume ramp			10	ms
$A_{V(SPK\_AMP)}$	Programmable Gain	Value represents the 'peak voltage' disregarding clipping due to lower PVDD Measured at 0dB input (1FS)	4.95		29.5	V_{peak}/FS
$\Delta A_{V(SPK\_AMP)}$	Amplifier gain error	Gain=29.5V_P/FS		0.5		dB
F_{SW}	Switching frequency of the speaker amplifier			384		kHz
				260		kHz
				480		kHz
				576		kHz
				768		kHz

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{DS(ON)}$	Drain-to-source on resistance of the individual output MOSFETs	FET + Metallization. V_{PVDD}=21V, $I_{(OUT)}$=500mA, T_J=25℃		75		mΩ
PROTECTION						
OCE_{THRES}	Over-Current Error Threshold	Speaker Output Current (Post LC filter), Speaker current, PVDD=21V (100Hz Burst on, 500 cycles interval), LC filter=10uF+0.68uF, Fsw=480kHz	7	7.5		A
$UVE_{THRES(PVDD)}$	PVDD under voltage error threshold			4.2		V
$OVE_{THRES(PVDD)}$	PVDD over voltage error threshold			23		V
DCE_{THRES}	Output DC Error protection threshold	Class D Amplifier's output DC voltage cross speaker load to trigger Output DC Fault protection		1.9		V
T_{DCDET}	Output DC Detect time	Class D Amplifier's output remain at or above DCE_{THRES}		620		ms
OTE_{THRES}	Over temperature error threshold			160		℃
$OTE_{Hysteresis}$	Over temperature error hysteresis			10		℃
OTW_{THRES}	Over temperature warning level			135		℃
AUDIO PERFORMANCE (STEREO BTL)						
$\vert V_{OS}\vert$	Amplifier offset voltage	Measure differentially with zero input data, programmable gain configured with 29.5Vp/FS, V_{PVDD}=12V	-10		10	mV
$P_{O(SPK)}$	Output Power (Per Channel) (High Performance Mode, Fsw=480kHz)	V_{PVDD}=12V,R_{SPK}=6Ω,f=1kHz,THD+N=10%		13.5		W
		V_{PVDD}=12V,R_{SPK}=6Ω,f=1kHz,THD+N=1%		11		W
		V_{PVDD}=18V,R_{SPK}=6Ω,f=1kHz,THD+N=10%		30		W
		V_{PVDD}=18V,R_{SPK}=6Ω,f=1kHz,THD+N=1%		24		W
		V_{PVDD}=21V,R_{SPK}=6Ω,f=1kHz,THD+N=10%		41		W
		V_{PVDD}=21V,R_{SPK}=6Ω,f=1kHz,THD+N=1%		33		W
$THD+N_{SPK}$	Total harmonic distortion and noise (P_O=1W,f=1kHz,R_{SPK}=6Ω, High Performance Mode, Fsw=480kHz)	V_{PVDD}=12V		0.024		%
		V_{PVDD}=18V		0.021		%
		V_{PVDD}=21V		0.012		%
$ICN_{(SPK)}$	Idle channel noise (A-Weighted, AES17)	VPVDD=12V, LC filter=10uH+0.47uF, Load=6Ω, LPD Mode		32.24		µVrms
		V_{PVDD}=12V, LC filter=10uH+0.47uF, Load=6Ω, High Performance Mode		35.58		µVrms
DR	Dynamic range	A-Weighted, -60dBFS method. V_{PVDD}=21V， Analog Gain=29.5Vp/FS		111		dB
SNR	Signal-to-noise ratio	A-Weighted, reference to 1% THD+N Output Level, V_{PVDD}=21V		114		dB
PSRR	Power supply rejection ratio	Injected Noise=1kHz, 1Vrms, V_{PVDD}=12V, input audio signal=digital zero		72		dB
$X\text{-}talk_{SPK}$	Cross-talk (worst case between left-to-right and right-to-left channel)	f=1kHz, V_{PVDD}=21V, Load=6Ω		90		dB
AUDIO PERFORMANCE (MONO PBTL)						
$\vert V_{OS}\vert$	Amplifier offset voltage	Measure differentially with zero input data, programmable gain configured with 29.5Vp/FS, V_{PVDD}=12V	-10		10	mV

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$P_{O(SPK)}$	Output Power	V_{PVDD}=21V,R_{SPK}=4Ω,f=1kHz,THD+N=1%		51		W
		V_{PVDD}=21V,R_{SPK}=4Ω,f=1kHz,THD+N=10%		63		W
		V_{PVDD}=18V,R_{SPK}=4Ω,f=1kHz,THD+N=1%		37		W
		V_{PVDD}=18V,R_{SPK}=4Ω,f=1kHz,THD+N=10%		46		W
$THD+N_{SPK}$	Total harmonic distortion and noise (P_O=1W, f=1kHz)	V_{PVDD}=21V, LC filter, R_{SPK}=4 Ω , High Performance Mode		0.04		%
DR	Dynamic range	A-Weighted, -60dBFS method, V_{PVDD}=21V, R_{SPK}=4Ω		115		dB
SNR	Signal-to-noise ratio	A-Weighted, reference to 1% THD+N Output Level, V_{PVDD}=21V, R_{SPK}=4Ω		117		dB
$ICN_{(SPK)}$	Idle channel noise (A-Weighted, AES17)	VPVDD=21V, LC filter=10uH+0.47uF, Load=4Ω, High Performance Mode		33		µVrms
PSRR	Power supply rejection ratio	V_{PVDD}=12V, LC filter=10uH+0.47uF, Load=4Ω, High Performance Mode		72		dB

7.6 Timing Requirements

		MIN	NOM	MAX	UNIT
Serial Audio Port Timing-Slave Mode					
f_{BCLK}	BCLK frequency	1.024			MHz
t_{BCLK}	BCLK period	40			ns
t_{BCLKL}	BCLK pulse width, low	16			ns
t_{BCLKH}	BCLK pulse width, high	16			ns
t_{BF}	BCLK rising to FSYNC edge	8			ns
t_{FB}	FSYNC Edge to BCLK rising edt	8			ns
t_{SU}	Data setup time, before BCLK rising edge	8			ns
t_{DH}	Data hold time, after BCLK rising edge	8			ns
t_{DFB}	Data delay time from BCLK failing edge		30		ns
I²C Bus Timing-Standard					
f_{SCL}	SCL clock frequency			100	kHz
t_{BUF}	Bus free time between a STOP and START condition	4.7			µs
t_{LOW}	Low period of the SCL clock	4.7			µs
t_{HI}	High period of the SCL clock	4			µs
t_{RS-SU}	Setup time for (repeated) START condition	4.7			µs
t_{S-HD}	Hold time for (repeated) START condition	4			µs
t_{D-SU}	Data setup time	250			ns
t_{D-HD}	Data hold time	0		3450	ns
t_{SCL-R}	Rise time of SCL signal			1000	ns
t_{SCL-R1}	Rise time of SCL signal after a repeated START condition and after an acknowledge bit			1000	ns
t_{SCL-F}	Fall time of SCL signal			1000	ns
t_{SDA-R}	Rise time of SDA signal			1000	ns
t_{SDA-F}	Fall time of SDA signal			1000	ns
t_{P-SU}	Setup time for STOP condition	4			µs
C_B	Capacitive load for each bus line			400	pf
I²C Bus Timing-Fast					
f_{SCL}	SCL clock frequency			400	kHz

		MIN	NOM	MAX	UNIT
t_{BUF}	Bus free time between a STOP and START condition	1.3			µs
t_{LOW}	Low period of the SCL clock	1.3			µs
t_{HI}	High period of the SCL clock	600			ns
$t_{RS\text{-}SU}$	Setup time for (repeated) START condition	600			ns
$t_{RS\text{-}HD}$	Hold time for (repeated) START condition	600			ns
$t_{D\text{-}SU}$	Data setup time	100			ns
$t_{D\text{-}HD}$	Data hold time	0		900	ns
$t_{SCL\text{-}R}$	Rise time of SCL signal	$20+0.1C_B$		300	ns
$t_{SCL\text{-}R1}$	Rise time of SCL signal after a repeated START condition and after an acknowledge bit	$20+0.1C_B$		300	ns
$t_{SCL\text{-}F}$	Fall time of SCL signal	$20+0.1C_B$		300	ns
$t_{SDA\text{-}R}$	Rise time of SDA signal	$20+0.1C_B$		300	ns
$t_{SDA\text{-}F}$	Fall time of SDA signal	$20+0.1C_B$		300	ns
$t_{P\text{-}SU}$	Setup time for STOP condition	600			ns
t_{SP}	Pulse width of spike suppressed			50	ns
C_B	Capacitive load for each bus line			400	pf

7.7 Timing Parametric Requirements Information

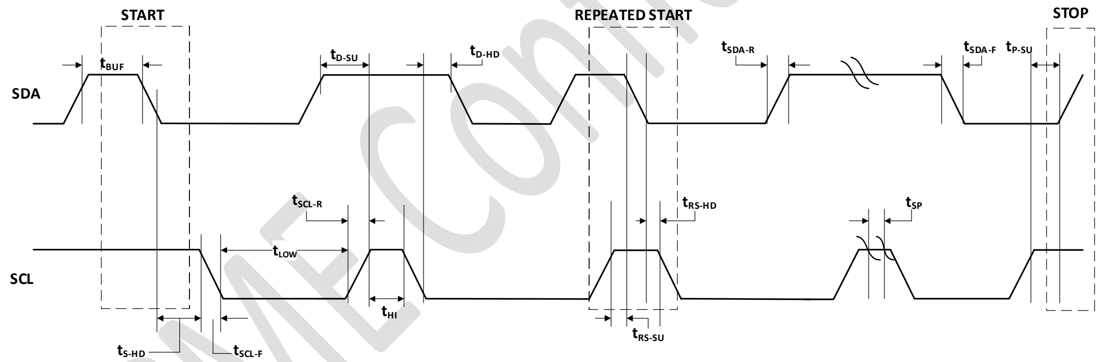


Figure 1 I²C Communication Port Timing Diagram

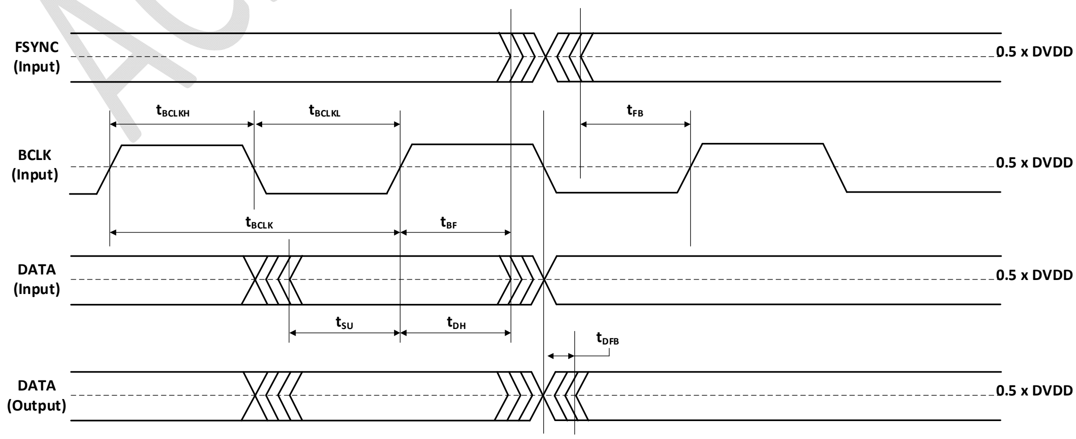


Figure 2 Serial Audio Port Timing in Slave Mode

8. *Idle Power Dissipation*

8.1 DVDD Current

Fs=480kHz, Free-are room temperature 25°C.

Table 1 DVDD Current

DVDD (V)	Device Mode	Current Consumption (mA)	Setting Register Location
3.3	Play Mode (DSP Enable)	23.79	Register 0x04
	Play Mode (DSP Bypass)	9.37	Register 0x04 and Register 0x05
	Driver-off (DSP Enable)	23.79	Register 0x04
	Driver-off (DSP Bypass)	9.09	Register 0x04
	Analog-off	1.89	Register 0x04
	Digital-off	1.89	Register 0x04
	$\overline{PDN}$=0	0.01	Pin 12 pulled to low

8.2 PVDD Current

Fs=480kHz, Free-are room temperature 25°C. LC Filter=10uH+0.68uF. LPD Mode.

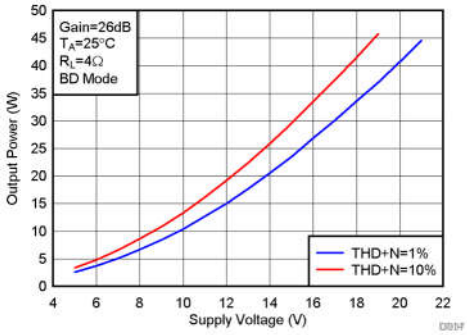
Table 2 PVDD Current

PVDD (V)	Device Mode	Current Consumption (mA)	Setting Register Location
7.4	Play	20.11	Register 0x04
	Driver-off	9.44	
	Analog-off	5.91	
	Digital-off	0.093	
	$\overline{PDN}$=0	0.0018	Pin 12 pulled to low
12	Play	23.57	Register 0x04
	Driver-off	9.505	
	Analog-off	5.981	
	Digital-off	0.101	
	$\overline{PDN}$=0	0.0018	Pin 12 pulled to low
18	Play	26.69	Register 0x04
	Driver-off	9.56	
	Analog-off	6.04	
	Digital-off	0.104	
	$\overline{PDN}$=0	0.0018	Pin 12 pulled to low
21	Play	30.94	Register 0x04
	Driver-off	9.67	
	Analog-off	6.12	
	Digital-off	0.107	
	$\overline{PDN}$=0	0.018	Pin 12 pulled to low

9. Typical Characteristics

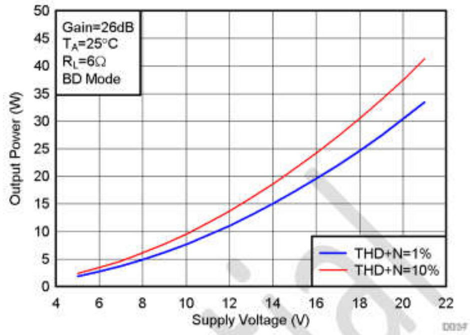
9.1 Bridge Tied Load (BTL) Configuration Curves with High Performance Mode

Free-air room temperature 25℃ (unless otherwise noted). ACM8625PEVM board, device PWM Modulation mode set to High Performance mode with 480kHz Fsw.



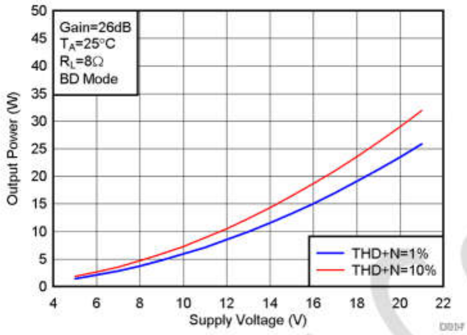
(Load=4Ω, Fsw=480kHz, High Performance Mode)

Figure 3 Output Power vs PVDD



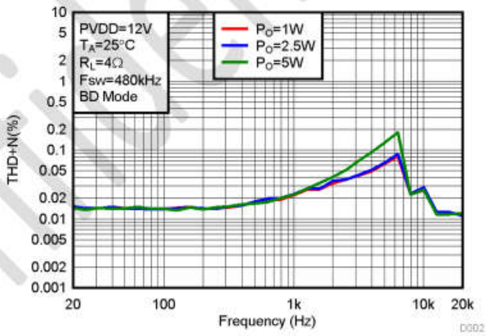
(Load=6Ω, Fsw=480kHz, High Performance Mode)

Figure 4 Output Power vs PVDD



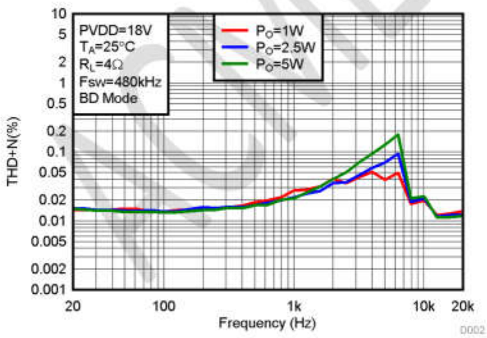
(Load=8Ω, Fsw=480kHz, High Performance Mode)

Figure 5 Output Power vs PVDD



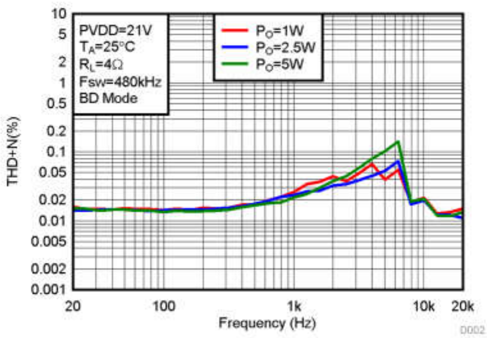
(PVDD=12V, Load=4Ω, Fsw=480kHz)

Figure 6 THD+N vs Frequency



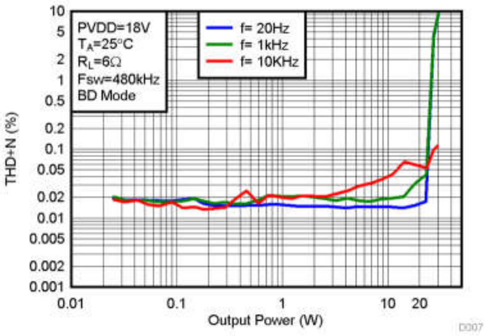
(PVDD=18V, Load=4Ω, Fsw=480kHz)

Figure 7 THD+N vs Frequency



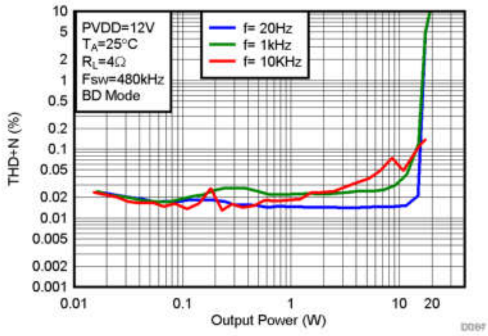
(PVDD=21V, Load=4Ω, Fsw=480kHz)

Figure 8 THD+N vs Frequency



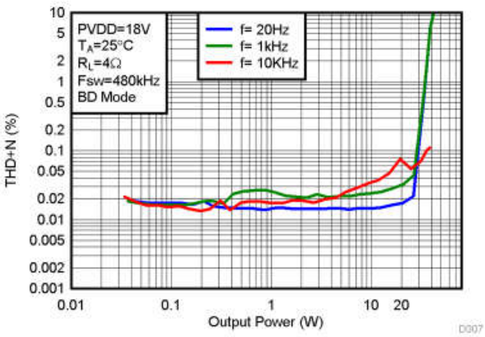
(PVDD=18V, Load=6Ω, Fsw=480kHz)

Figure 9 THD+N vs Output Power



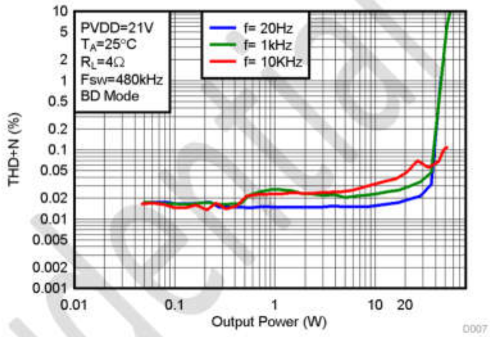
(PVDD=12V, Load=4Ω, Fsw=480kHz)

Figure 10 THD+N vs Output Power



(PVDD=18V, Load=4Ω, Fsw=480kHz)

Figure 11 THD+N vs Output Power

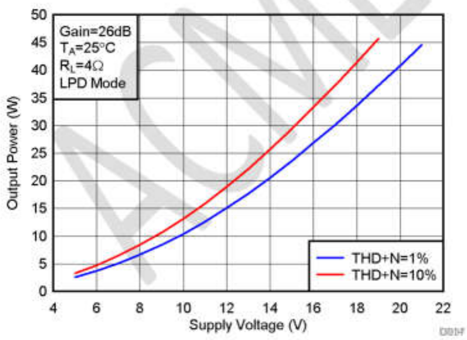


(PVDD=21V, Load=4Ω, Fsw=480kHz)

Figure 12 THD+N vs Output Power

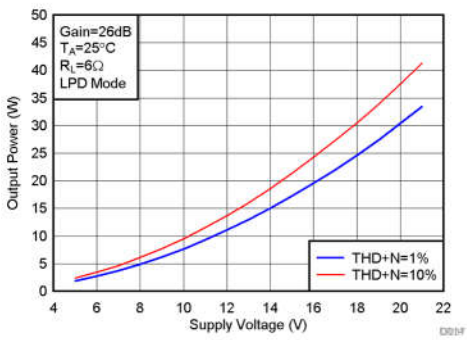
9.2 Bridge Tied Load (BTL) Configuration Curves with LPD Mode

Free-air room temperature 25℃ (unless otherwise noted). ACM8625PEVM board, device PWM Modulation mode set to Low Power Dissipation mode with 480kHz Fsw.



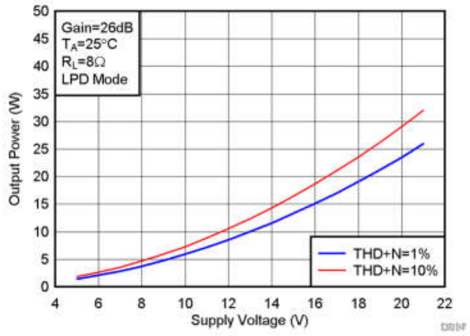
(Load=4Ω, Fsw=480kHz, LPD Mode)

Figure 13 Output Power vs PVDD



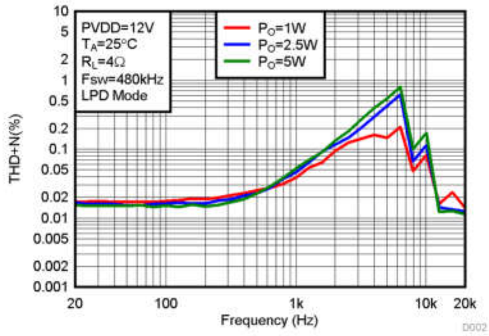
(Load=6Ω, Fsw=480kHz, LPD Mode)

Figure 14 Output Power vs PVDD



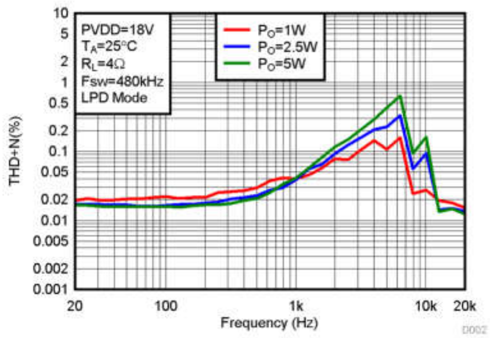
(Load=8Ω, Fsw=480kHz, LPD Mode)

Figure 15 Output Power vs PVDD



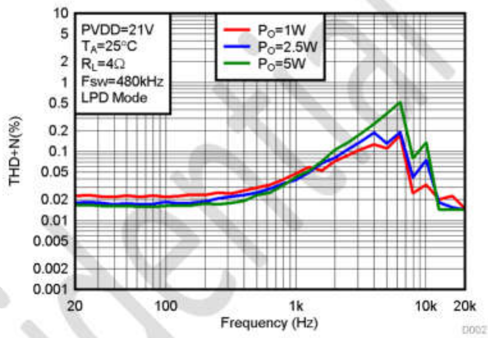
(PVDD=12V, Load=4Ω, Fsw=480kHz)

Figure 16 THD+N vs Frequency



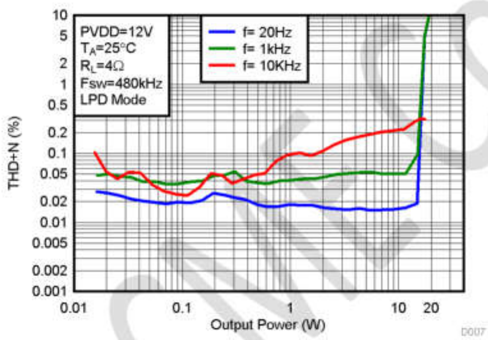
(PVDD=18V, Load=4Ω, Fsw=480kHz)

Figure 17 THD+N vs Frequency



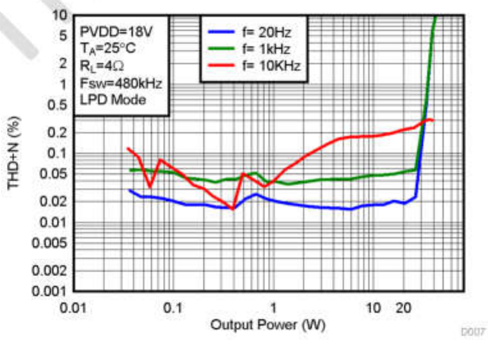
(PVDD=21V, Load=4Ω, Fsw=480kHz)

Figure 18 THD+N vs Frequency



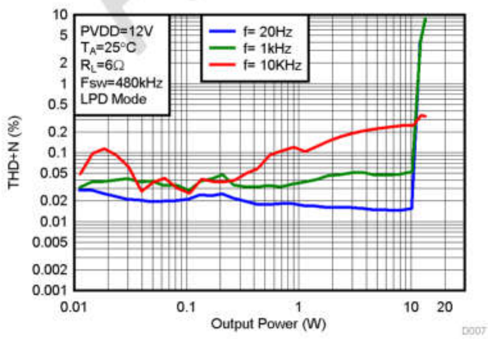
(PVDD=12V, Load=4Ω, Fsw=480kHz)

Figure 19 THD+N vs Output Power



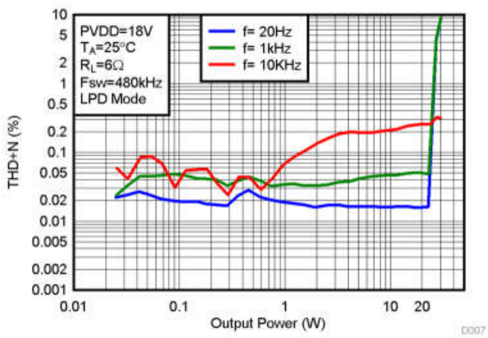
(PVDD=18V, Load=4Ω, Fsw=480kHz)

Figure 20 THD+N vs Output Power



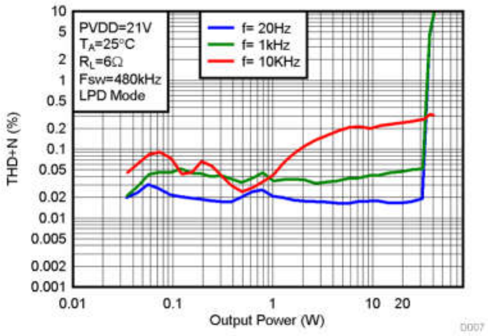
(PVDD=12V, Load=6Ω, Fsw=480kHz)

Figure 21 THD+N vs Output Power



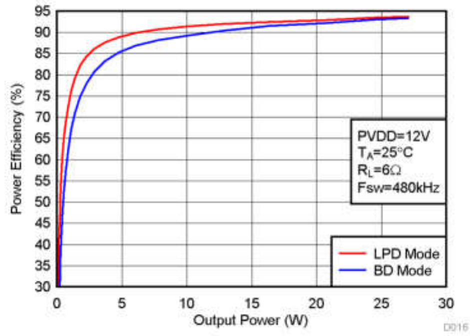
(PVDD=18V, Load=6Ω, Fsw=480kHz)

Figure 22 THD+N vs Output Power



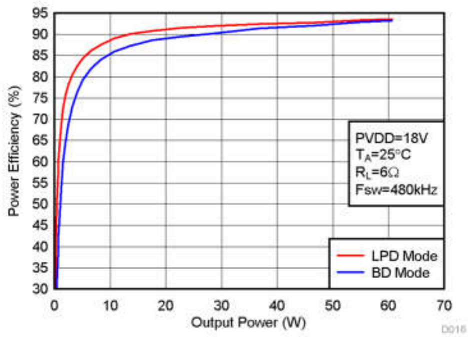
(PVDD=21V, Load=6Ω, Fsw=480kHz)

Figure 23 THD+N vs Output Power



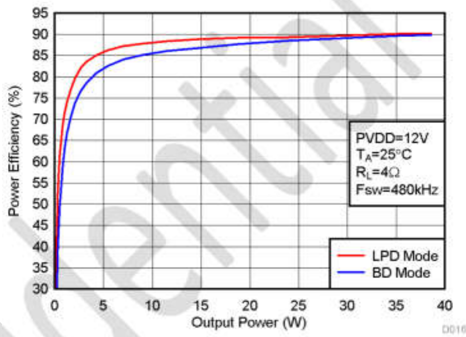
(PVDD=12V, Load=6Ω, Fsw=480kHz)

Figure 24 Efficiency vs Output Power



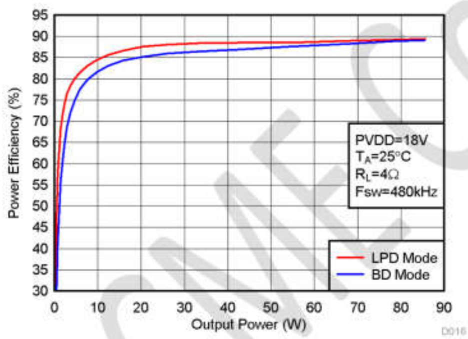
(PVDD=18V, Load=6Ω, Fsw=480kHz)

Figure 25 Efficiency vs Output Power



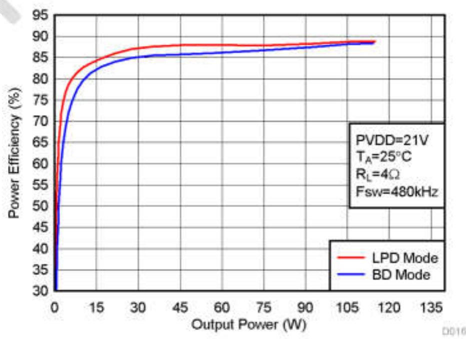
(PVDD=12V, Load=4Ω, Fsw=480kHz)

Figure 26 Efficiency vs Output Power



(PVDD=18V, Load=4Ω, Fsw=480kHz)

Figure 27 Efficiency vs Output Power

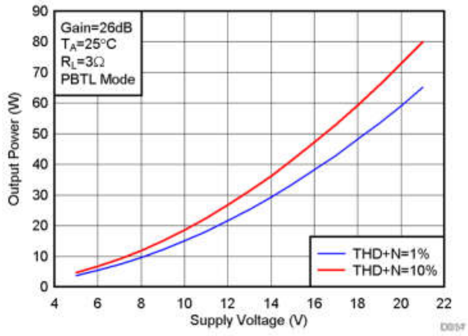


(PVDD=21V, Load=4Ω, Fsw=480kHz)

Figure 28 Efficiency vs Output Power

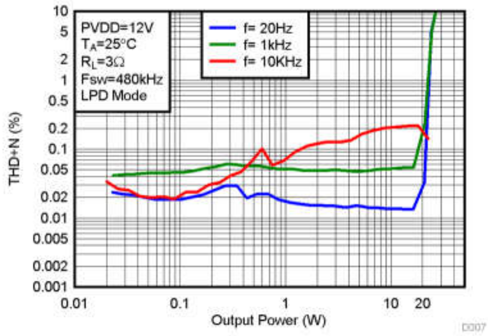
9.3 Parallel Bridge Tied Load (PBTL) Configuration Curves with LPD Mode

Free-air room temperature 25℃ (unless otherwise noted). ACM8625PEVM board, device PWM Modulation mode set to Low Power Dissipation mode with 480kHz Fsw.



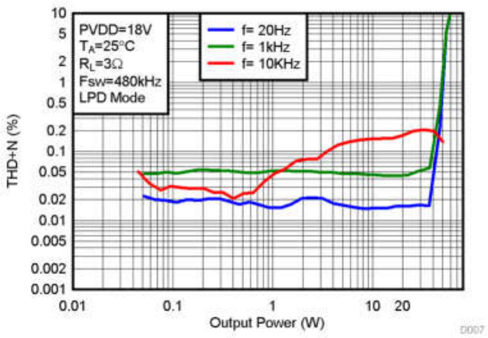
(Load=3Ω, Fsw=480kHz, LPD Mode)

Figure 29 Output Power vs PVDD



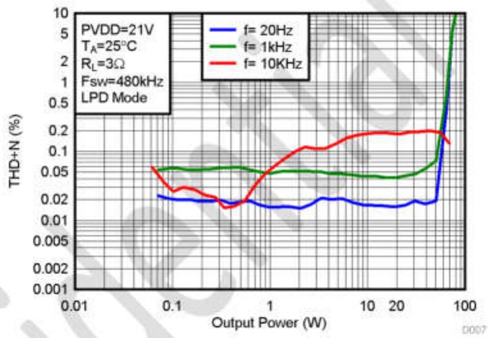
(Load=3Ω, Fsw=480kHz, LPD Mode)

Figure 30 THD+N vs Output Power



(Load=3Ω, Fsw=480kHz, LPD Mode)

Figure 31 THD+N vs Output Power



(Load=3Ω, Fsw=480kHz, LPD Mode)

Figure 32 THD+N vs Output Power

10. Detailed Description

10.1 Overview

The ACM8625P device integrates 4 main building blocks together into a single cohesive device that maximizes sound quality, flexibility, and ease of use. The 4 main building blocks are listed as follows:

- A stereo audio DAC
- An Audio Effect Tuning engine
- A flexible closed-loop amplifier capable of operating in stereo or mono, at different switching frequencies, and supporting a variety of output voltages and loads
- An I²C control port for communication with the device

The device requires only two power supplies for proper operation. A DVDD supply is required to power the low voltage digital circuitry. Another supply, called PVDD, is required to provide power to the output stage of the audio amplifier. Two internal LDOs convert PVDD to 5V for VREG_AVDD and 3.3V for VREG_DVDD respectively.

10.2 Functional Block Diagram

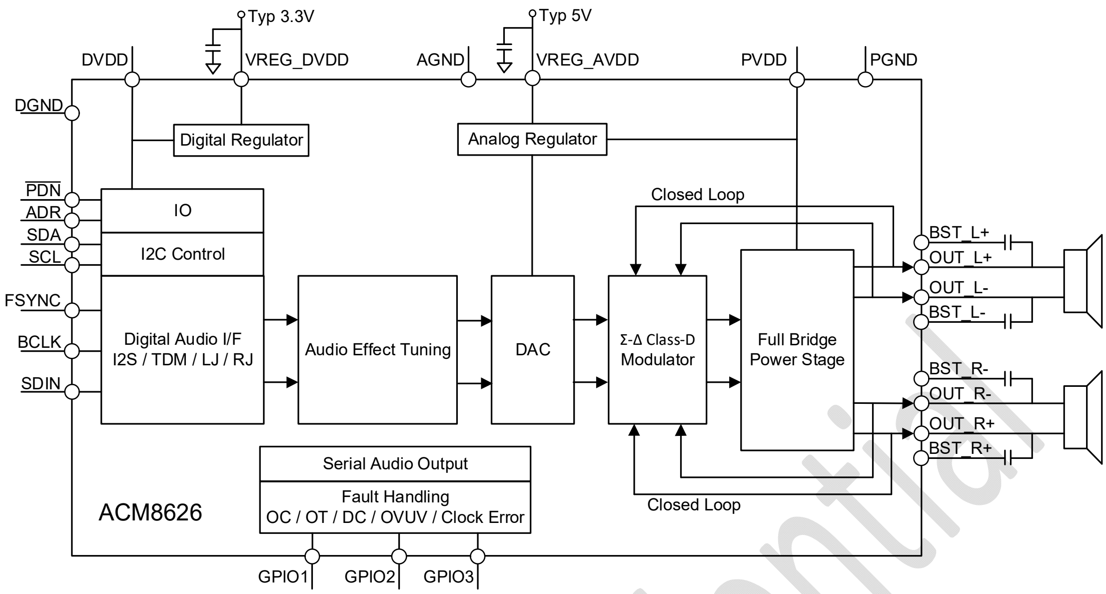


Figure 33 Function Block Diagram

10.3 Device Clocking

9.3.1 Main Clocks

The ACM8625P device has flexible systems for clocking. Internally, the device requires a number of clocks, mostly at related clock rates to function correctly. All of these clocks can be derived from the Serial Audio Interface.
The serial audio interface typically has 3 connection pins which are listed as follows:

- BCLK
- FSYNC/LRCLK (Left/Right Word Clock and Frame Sync)
- SDIN (Input Data)

The device has an internal PLL that is used to take BCLK as reference clock and create the higher rate clocks required by the Audio Effect Tuning and the DAC clock.
The ACM8625P device has an audio sampling rate detection circuit that automatically senses the sampling frequency. Common audio sampling frequencies of 32kHz, 44.1kHz-48kHz, 88.2kHz-96kHz, 176.4kHz-192kHz are supported. The sampling frequency detector sets the clock for DAC and Audio Effect Tuning automatically.
The ACM8625P device has an audio sampling rate detection circuit that automatically senses the sampling frequency. Common audio sampling frequencies of 32kHz, 44.1kHz-48kHz, 88.2kHz-96kHz, 176.4kHz-192kHz are supported. The sampling frequency detector sets the clock for DAC and Audio Effect Tuning automatically.

9.3.2 Serial Audio Port – Clock Rates

The serial audio interface port is a 3-wire serial port with the signals FSYNC/LRCLK, BCLK, and SDIN. BCLK is the serial audio bit clock, used to clock the serial data present on SDIN into the serial shift register of the audio interface. Serial data is clocked into the ACM8625P device on the rising edge of BCLK. The FSYNC/LRCLK pin is the serial audio left/right word clock or frame sync when the device is operated in TDM mode.

Table 3. Audio Data Formats, Bit Depths and Clock Rates

FORMAT	DATA BITS	MAXIMUM LRCLK/FS FREQUENCY (kHz)	BCLK RATE (Fs)
I²S/LJ/RJ	32,24,20,16	32 to 96	64,32
TDM	32,24,20,16	32	128
		44.1/48	128,256,512
		96	128,256

When clock halt, non-supported BCLK to FSYNC/LRCLK ratio is detected, the device reports clock error in Register 0x18 in Page0.

9.3.3 Clock Halt Auto-recovery

As some of host processor halts I²S clock when there is no audio playing. After clock halt, the device puts all channels into Hi-Z state and reports clock error in register 0x18 in Page0. After audio clock recovery, the device automatically returns to the previous state.

9.3.4 Sample Rate on The Fly Change

ACM8625P supports FSYNC/LRCLK rate on the fly change. For example, change FSYNC/LRCLK from 32kHz to 48kHz or 96kHz, Host processor needs to put LRCLK (FSYNC) to Halt state at least 10ms before changing to new sample rate.

9.3.5 Serial Audio Port – Data Formats and Bit Depths

The device supports industry-standard audio data formats, including standard I²S, left-justified, right-justified and TDM/DSP data. Data formats are selected via Register 0x07 in Page0. If the high width of FSYNC/LRCLK in TDM/DSP mode is less than 8 cycles of BCLK, the register Page0/0x07 D[5:4] should be set to 01. All formats require binary two's complement, MSB-first audio data, up to 32-bit audio data is accepted. All the data formats, word length and clock rate supported by this device are shown in Table 1. The data formats are detailed in Figure 14 to Figure 18. The word length are selected via Register Page0/0x07 D[1:0]. The offset of data is selected via Register Page0/0x08.

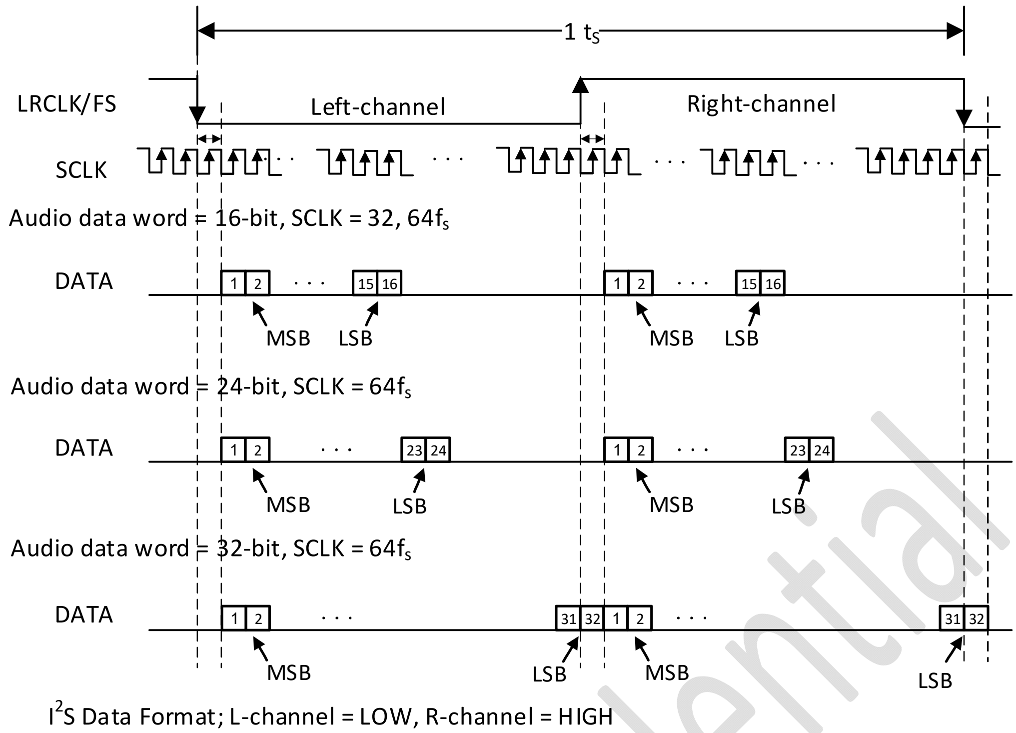


Figure 34 I²S Audio Data Format

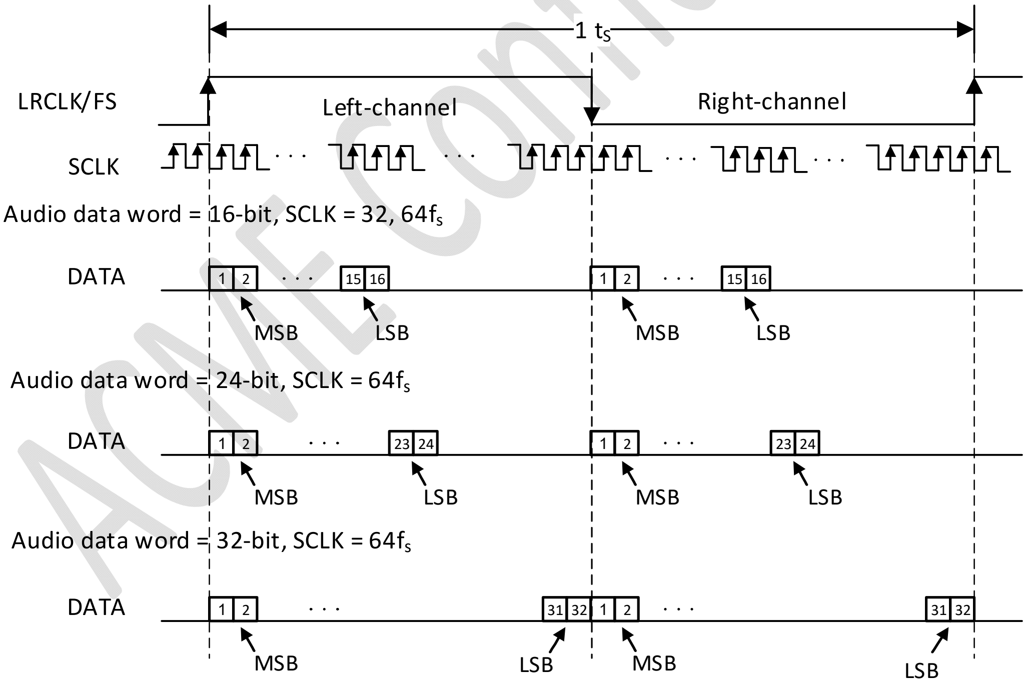


Figure 35 Left-Justified Audio Data Format

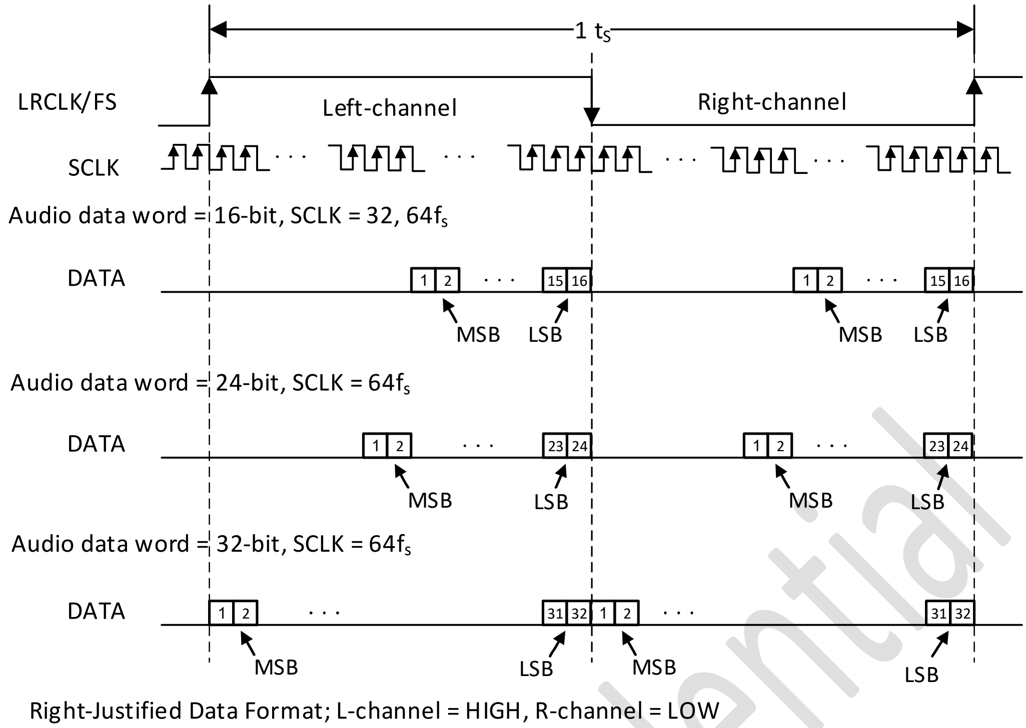


Figure 36 Right-Justified Audio Data Format

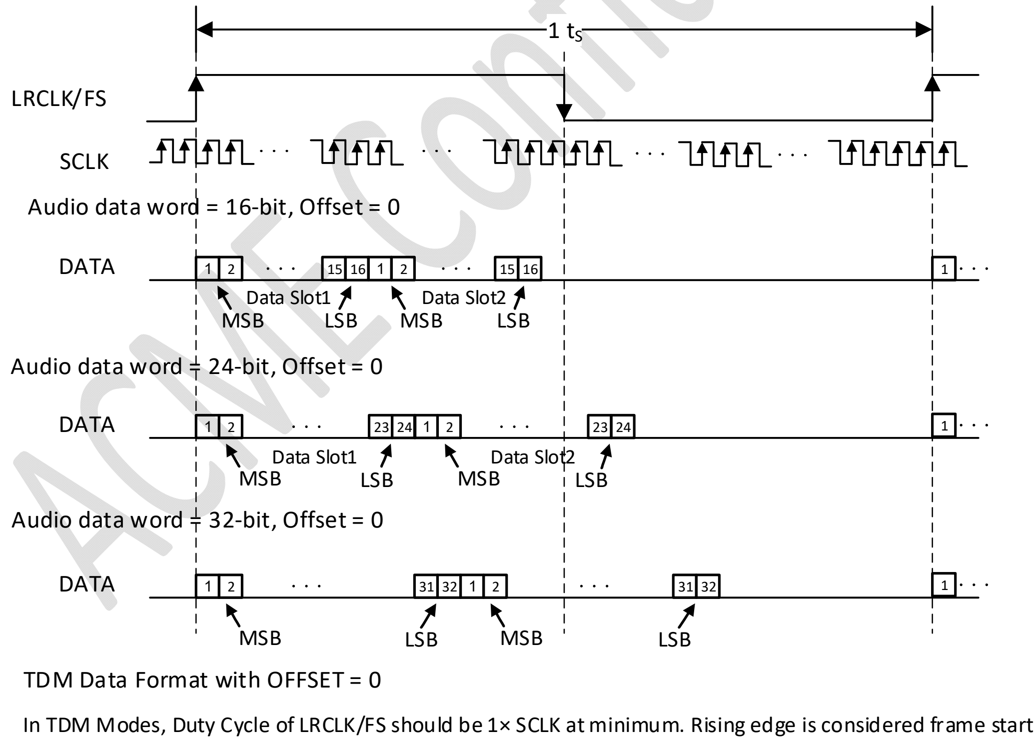
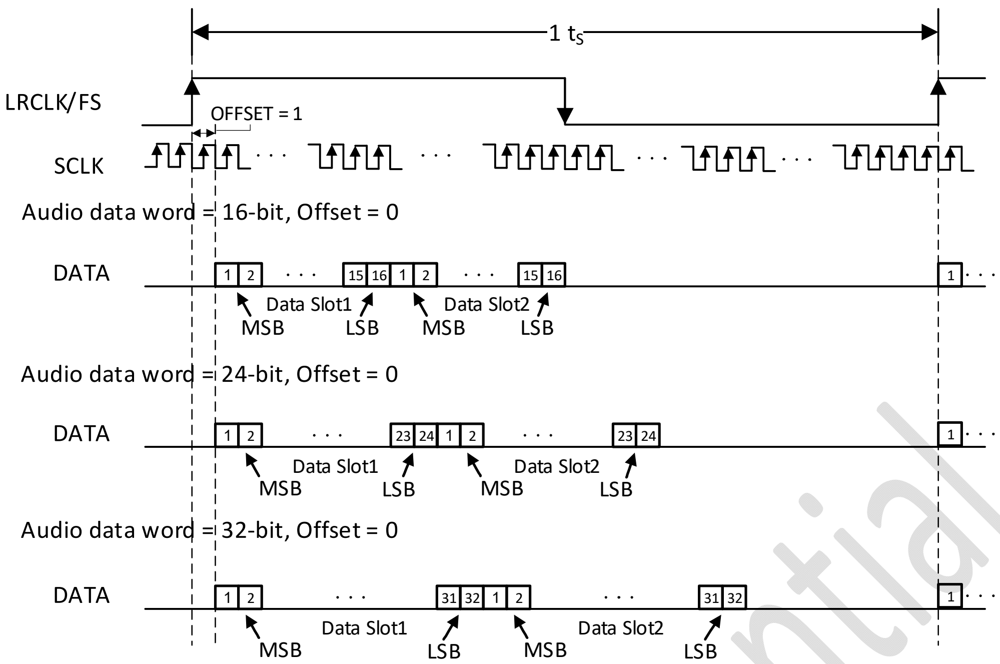


Figure 37 TDM 1 Audio Data Format



TDM Data Format with OFFSET = 1

In TDM Modes, Duty Cycle of LRCLK/FS should be 1× SCLK at minimum. Rising edge is considered frame start

Figure 38 TDM 2 Audio Data Format

10.4 Power Supplies

To facilitate system design, ACM8625P needs only a 3.3-V supply in addition to (4.5V~21V) power-stage supply. Two internal voltage regulators provide suitable voltage levels for the gate drive circuitry and internal circuitry. The external pins are provided only as a connection point for off-chip bypass capacitors to filter the supply. Connecting external circuitry to theses regulators may result in reduced performance and damage to the device. Additionally, all circuitry requiring a floating voltage supply, e.g., the high-side gate drive, is accommodated by built-in bootstrap circuitry requiring only a few external capacitors. In order to provide good electrical and acoustical characteristics, the PWM signal path for the output stage is designed as identical, independent half-bridges. For this reason, each half-bridge has separate bootstrap pins (BST_x). The gate drive voltages (VREG_AVDD) are derived from the PVDD voltage. Special attention should be paid to placing all decoupling capacitors as close to their associated pins as possible. In general, inductance between the power-supply pins and decoupling capacitors must be avoided. For a properly functioning bootstrap circuit, a small ceramic capacitor must be connected from each bootstrap pin (BST_x) to the power-stage output pin (OUT_x). When the power-stage output is low, the bootstrap capacitor is charged through an internal diode connected between the gate-drive regulator output pin (VREG_AVDD) and the bootstrap pin. When the power-stage output is high, the bootstrap capacitor potential is shifted above the output potential and thus provides a suitable voltage supply for the high-side gate driver.

10.5 Device Gain Setting

As seen in the figure below, the audio path of the ACM8625P consists of a digital audio input port, a digital audio path, a digital to PWM convertor, a gate driver stage, a Class D power stage, and the feedback loop which feeds the output information back into the digital to PWM block to correct for distortion sensed on the output pins. The total amplifier gain is comprised of digital gain in the digital audio path and the analog gain from the input of the analog modulator to the output of the speaker amplifier power stage.

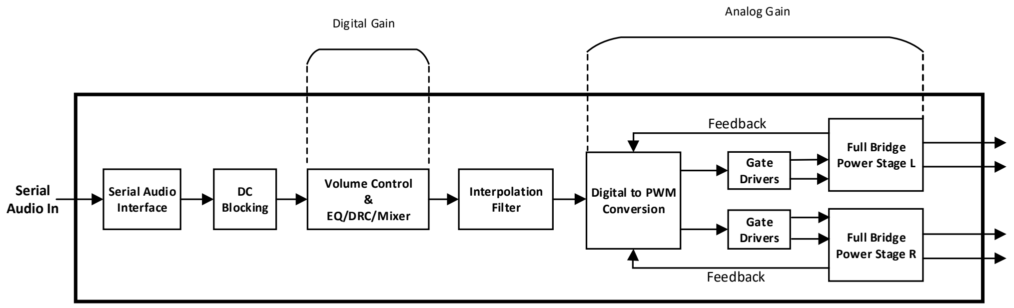


Figure 39 Gain Structure

As shown above, the first gain stage for the speaker amplifier is present in the digital audio path. It consists of the volume control and EQ/DRC/Mixer. The volume control is set to 0dB by default and EQ/DRC/Mixer is bypassed by default.

Amplifier analog gain settings are presented as the output level in dBV (dB related to 1Vrms) with a full-scale serial audio input (0dBFS) and the digital volume control set to 0dB.

V_{AMP}=Input +Digital Gain + Analog Gain dBV

Where:

- V_{AMP} is the amplifier output voltage in dBV_{RMS}
- Input is the digital input amplitude in dB with respect to 0dBFS
- Digital Gain is the digital volume control setting, -110dB to 24dB.
- Analog Gain is the analog gain setting (26.38dB, 25.88dB, 25.38dB to 10.88dB in 0.5dB step)

Table 2 outlines gain setting expressed in dBV_{RMS} and V_{PEAK}.

Table 4 Amplifier Gain Settings

Analog Gain (Register 0x02h in Page0)	FULL SCALE OUTPUT	
	dBV_{RMS}	V_{PEAK}
00000	26.38	29.5
00001	25.88	27.84
00010	25.38	26.3
00011	24.88	24.8
…	…	…
01110	19.38	13.17
01111	18.88	12.44
10000	18.38	11.74
…	…	…
11111	10.88	4.95

10.6 Device Protection

ACM8625P has built-in protection circuits including thermal, short-circuit, under-voltage detection, over-voltage detection, output DC detection, clock error detection circuits. Once these faults occur, ACM8625P reports fault via register 0x17h-0x19h in Page0 and these faults may pull the GPIO0/1 pin to DGND by proper setting in Register 0x0Ah and 0x0Ch in Page0. Clear these faults by writing Bit7 in register 0x01h in Page0 from 0 to 1.

1. Over temperature protection. When the internal junction temperature is higher than 160°C power stages will be turned off and ACM8625P will return to normal operating once the temperature drops to 150°C. The

temperature values may vary around 10%. Enable Over temperature protection auto-recovery by writing Register 0x11h (Bit 2) from 0 to 1.

2. Short-circuit protection. The short-circuit protection protects the output stage when the wires connect to loudspeakers are shorted to each other or GND/PVDD. For normal 21V operations, the current flowing through the power stage will be less than 7.5A for stereo configuration. Otherwise, the short-circuit detectors pull the $\overline{\text{FAULT}}$ pin (GPIO pin) to DGND, disabling the output stages.
3. PVDD over-voltage protection. Once the PVDD voltage is higher than 23V, ACM8625P turns off its loudspeaker power stages. When PVDD becomes lower than 22.6V, ACM8625P will return to normal operation.
4. PVDD under-voltage protection. Once the PVDD voltage is lower than 4.2V, ACM8625P turns off its loudspeaker power stages. When PVDD becomes higher than 4.35V, ACM8625P will return to normal operation.
5. Speaker DC Protection. Once the output differential voltage exceeds 1.9V (typical) for more than 620ms (typical) at the same polarity. ACM8625P will turn off its loudspeaker stages. Once this fault been removed, clear this fault by writing Bit7 in register 0x01h from 0 to 1 or device will keep output stages in Hi-Z state.
6. Clock error protection. When clock halt, non-supported BCLK to FSYNC/LRCLK ratio is detected, the device reports clock error in Register 0x18 in Page0. Once the fault been removed, device will return to normal operation.

10.7 Spread Spectrum

ACM8625P supports spread spectrum with triangle mode. Spread spectrum is used to minimize the EMI noise.
Enable spread spectrum in register 0x0Eh in Page 0, default is disable.
Enable Spread Spectrum Script with following sequence (Suitable for 384kHz/480kHz/576kHz switching frequency):

1. Step1, Write content 0x00 to Register address 0x00.
2. Step2, Write content 0x01 to Register address 0x0E.
3. Step3, Write content 0x01 to Register address 0x00.
4. Step4, Write content 0x0b to Register address 0x1A.
5. Step5, Write content 0x00 to Register address 0x00.

10.8 I²C Device Address

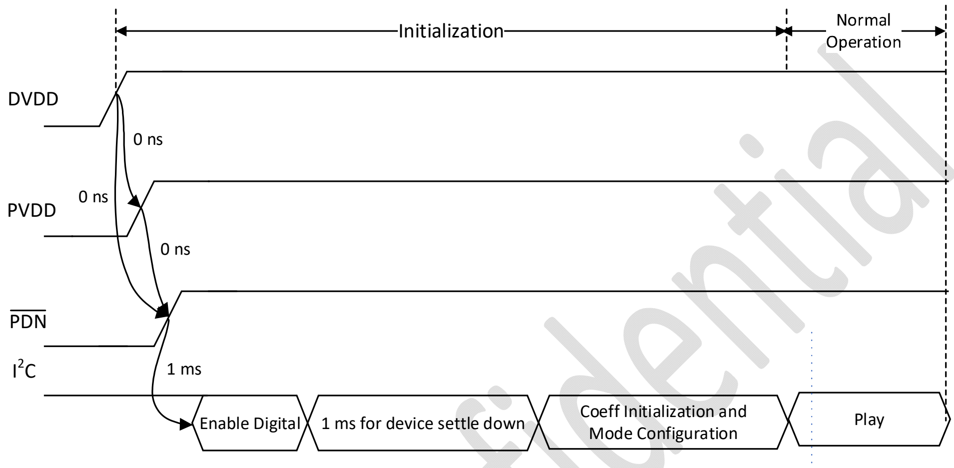
The ACM8625P device has 7 bits for I²C device address. The first five bits (MSBs) of the device address are factory preset to 01011 (0x5x). The next two bits of address byte are the device select bits which can be user-defined by ADR pin in Table 5.

Table 5 I²C Device Address Configuration

ADR PIN Configuration	MSBs					User Define		LSB	Device Write Address
4.7kΩ to DVDD	0	1	0	1	1	0	0	R/W	0x58
15kΩ to DVDD	0	1	0	1	1	0	1	R/W	0x5a
47kΩ to DVDD	0	1	0	1	1	1	0	R/W	0x5c
120kΩ to DVDD	0	1	0	1	1	1	1	R/W	0x5e

10.9 Start-up sequence

1. Configure ADR/GPIO2 pin with proper setting for I^2C device address.
2. Bring up power supplies.
3. Once all power supplies are stable, bring up the PDN pin HIGH 1ms before I^2C communication.
4. Configure the device via I^2C control port based on the user case (Make sure the PDN pin= HIGH before I^2C control port operating).
5. The device is now in normal operation.

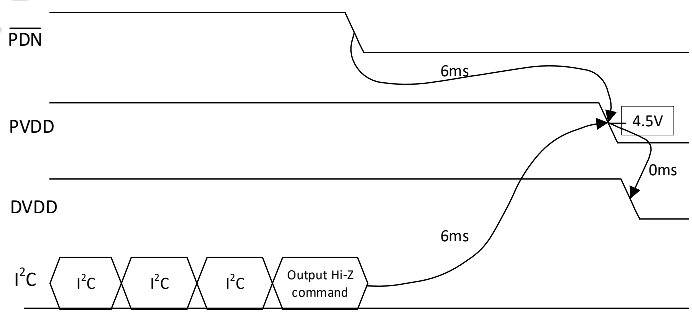


Notes:
1) 0ns means no sequence requirement
2) I^2C communication and internal Digital processing work in DVDD domain, no PVDD required

Figure 40 Start-up Sequence

10.10 Shutdown sequence

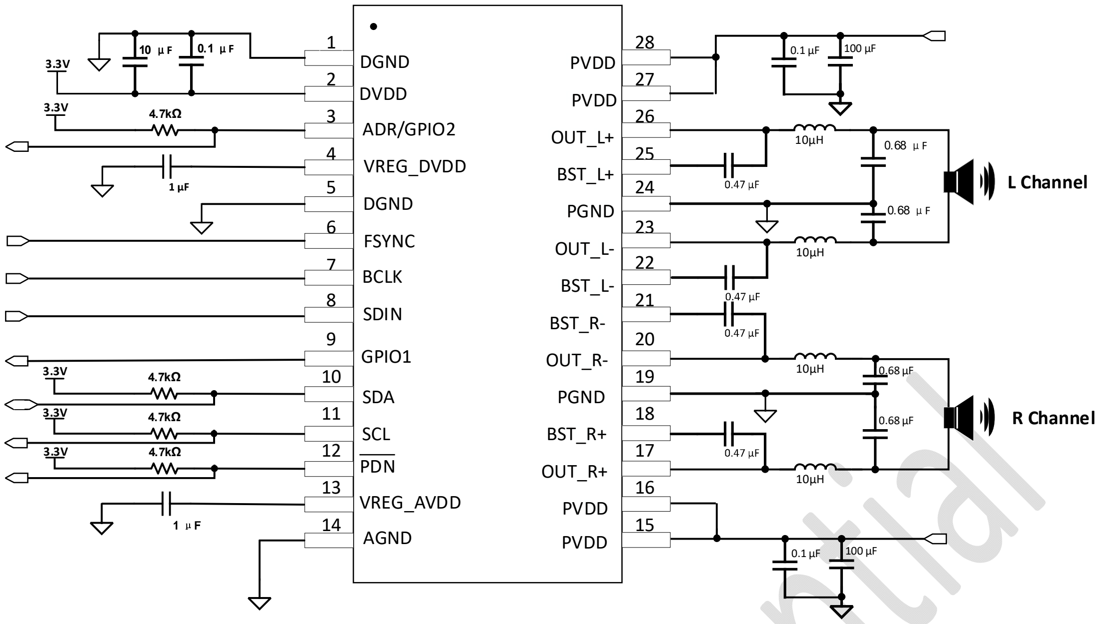
1. The device is in normal operation.
2. Configure the device in digital off state via register 0x04h or pull PDN low.
3. Wait at least 6ms (This time depends on the FSYNC rate, digital volume and digital volume ramp down rate).
4. Bring down power supplies.
5. The device is now fully shutdown and powered off.



- Before PVDD/DVDD power down, Class D Output driver needs to be disabled by PDN or by I^2C.
- At least 6ms delay needed based on LRCLK (Fs) = 48kHz,Digital volume ramp down update every sample period, decreased by 0.5dB for each update, digital volume =24dB.

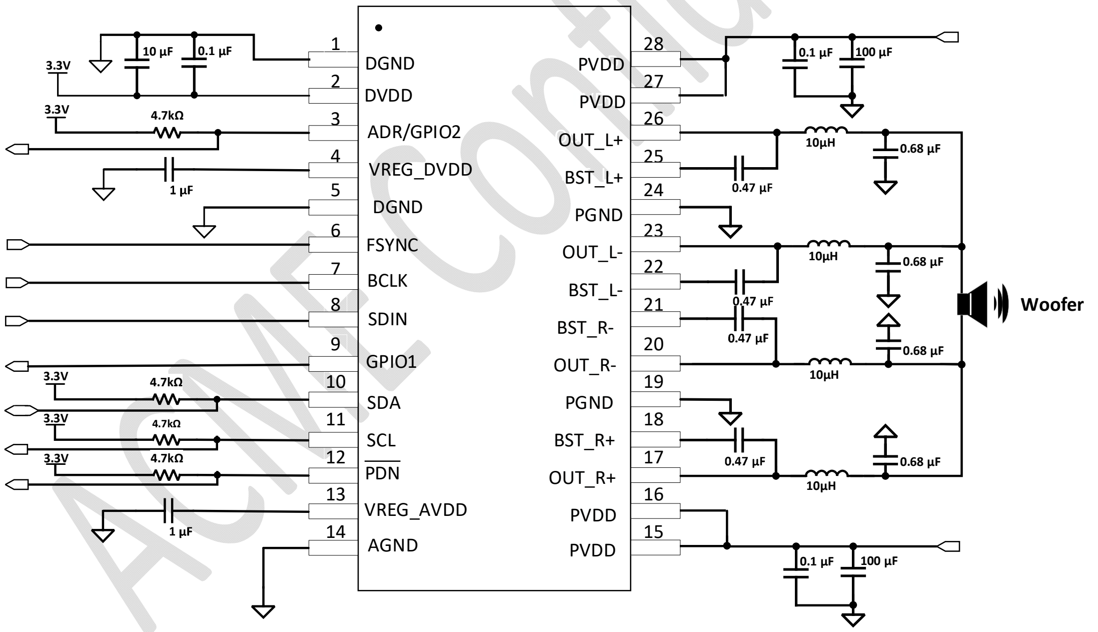
Figure 41 Shutdown Sequence

11. Application Circuit Example for Stereo



Note: Both 0.47uF or 0.22uF are suitable for BST caps.

12. Application Circuit Example for Mono



Note: Both 0.47uF or 0.22uF are suitable for BST caps.

13. Register Maps

13.1 Control Registers on Page0

Offset	Acronym	Register Name	Reset Value
0x01	AMP_CTRL1	F_{SW} PWM switching frequency, Fault clear, PBTL/BTL	0x00
0x02	AMP_CTRL2	Analog gain	0x00
0x03	AMP_CTRL3	Loop bandwidth, 2 PWM channels phase control	0x00
0x04	STATE_CTRL	Reset, Separate channel Hi-Z / Mute, State Control	0x00
0x05	PROCESSING_CTRL1	AGL, DRB, EQ, Post EQ, Sub-CH bypass control	0x12
0x06	PROCESSING_CTRL2	Processing flow selection and low power mode selection	0xF0
0x07	I2S_DATA_FORMAT1	I2S data format, length, FSYNC	0x02
0x08	I2S_DATA_FORMAT2	I2S Shift bits	0x00
0x09	I2S_DATA_FORMAT3	Reserved	0x05
0x0A	GPIO2_CTRL	SDOUT (GPIO2) enable and function selection	0x29
0x0B	GPIO1_CTRL	ADR (GPIO1) enable and function selection	0x2B
0x0C	GPIO1_FAULT_SEL	Clipping, OTW, OTSD, Clock Fault, PVDD UV/OV, DC, OC selection	0xFF
0x0D	GPIO2_FAULT_SEL	Clipping, OTW, OTSD, Clock Fault, PVDD UV/OV, DC, OC selection	0xFF
0x0E	SS_CTRL	Spread spectrum setting	0x00
0x0F	VOLUME_CTRL_L	Volume control for left channel	0xD0
0x10	VOLUME_CTRL_R	Volume control for right channel	0xD0
0x11	MSIC_CTRL	Fault latch selection, OTSD auto-recovery enable	0x03
0x12	I2S_CLK_FORMAT_RPT1	BCLK ratio (MSB), Sample rate detect	0x00
0x13	I2S_CLK_FORMAT_RPT2	BCLK ratio (LSB)	0x00
0x15	DIEID_RPT	DIE ID	0x00
0x16	STATE_RPT	State report	0x00
0x17	FAULT_RPT1	OTSD, PVDD OV/UV, DC, OC	0x00
0x18	FAULT_RPT2	Clock fault, EQs write error	0x00
0x19	FAULT_RPT3	Clipping, OTW	0x00
0x27	GPIO_PP_OD_CTRL	GPIO Open Drain Control	0x00
0x28	DIG_DSP_CTRL	DRC, Lookahead, Class-H bypass Control	0x00
0x7E	XOR_CHECKSUM	XOR Checksum	0x00
0x7F	CRC_CHECKSUM	CRC Checksum	0x00

12.1.1 Register 1 AMP_CTRL1 (Offset=1h) [Reset=0x00]

7	6	5	4	3	2	1	0
FAULT_CLR	RESERVED			FSW_SWL			PBTL
R/W	R			R/W			R/W

Bit	Field	Type	Reset	Description

7	FAULT_CLR	R/W	0	Once write this bit to 1, device will clear analog fault, this bit is auto-clear
6-4	RESERVED	R	000	These bits are reserved
3-1	FSW_SEL	R/W	000	000: 384kHz 001: 260kHz 010: 480kHz 011: 576kHz 100: 768kHz
0	PBTL	R/W	0	0: BTL Mode 1: PBTL Mode, PBTL can be set when device is in digital off state

12.1.2 Register 2 AMP_CTRL2 (Offset=2h) [Reset=0x00]

7	6	5	4	3	2	1	0
RESERVED			ANA_GAIN				
R			R/W				

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	000	These bits are reserved
4-0	ANA_GAIN	R/W	00000	Analog Gain Control, with 0.5dB per step. These bits control the analog gain. 00000: 0dB (29.5Vp/FS) 00001: -0.5dB 00010: -1dB ... 11111: -15.5dB

12.1.3 Register 3 AMP_CTRL3 (Offset=3h) [Reset=0x00]

7	6	5	4	3	2	1	0
RESERVED		CH_PHASE_CTL	RESERVED		BW_CTRL		
R		R/W	R		R/W		

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	00	These bits are reserved
5	CH_PHASE_CTRL	R/W	0	0: out phase 1: in phase
2-0	BW_CTRL	R/W	000	000: 75kHz 001: 90kHz 010: 105kHz 011: 125kHz 100: 155kHz 101: 180kHz

				110: 220kHz 111: 265kHz

12.1.4 Register 4 STATE_CTRL (Offset=4h) [Reset=0x00]

7	6	5	4	3	2	1	0
RST_REG	REST_MOD	CH_L_HIZ	CH_R_HIZ	MUTE_L	MUTE_R	CTRL_STATE	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Bit	Field	Type	Reset	Description
7	RST_REG	R/W	0	Register Reset 0: Normal 1: Reset Register
6	RST_MOD	R/W	0	Signal path Reset 0: Normal 1: Reset Signal path
5	CH_L_HIZ	R/W	0	Force Channel L's output driver into Hi-Z state 0: Normal State 1: Change L channel's output driver into Hi-Z state
4	CH_R_HIZ	R/W	0	Force Channel R's output driver into Hi-Z state 0: Normal State 1: Change R channel's output driver into Hi-Z state
3	MUTE_L	R/W	0	MUTE L Channel 0: Normal 1: Mute L Channel
2	MUTE_R	R/W	0	MUTE R Channel 0: Normal 1: Mute R Channel
1-0	CTRL_STATE	R/W	00	00: Digital Off 01: Analog off 10: Driver Off (Hiz) 11: Play

12.1.5 Register 5 PROCESSING_CTRL1 (Offset=5h) [Reset=0x12]

7	6	5	4	3	2	1	0
AGL_BP	DRB_BP	EQ_BP	RESERVED	POST_EQ_BP	RESERVED	SUB_CH_BP	PROCESSING_BP
R/W	R/W	RW	R	R/W	R	R/W	R/W

Bit	Field	Type	Reset	Description
7	AGL_BP	R/W	0	0: Enable AGL 1: Bypass AGL
6	DRB_BP	R/W	0	0: Enable DRB

Bit	Field	Type	Reset	Description
				1: Bypass DRB
5	EQ_BP	RW	0	0: Enable EQ 1: Bypass EQ
4	RESERVED	R	0	This bit is reserved
3	POST_EQ_BP	R/W	0	0: Enable Post-EQ 1: Bypass Post-EQ
2	RESREVED	R	0	This bit is reserved
1	SUB_CH_BP	R/W	1	0: Enable Sub Channel Processing 1: Bypass Sub Channel Processing
0	PROCESSING_BP	R/W	0	0: Enable audio effect tuning 1: Bypass all audio effect tuning

12.1.6 Register 6 PROCESSING_CTRL2 (Offset=6h) [Reset=0xF0]

7	6	5	4	3	2	1	0
RESERVED				POWER_SAVE_DOWN	PLL_CLK_DIV		REAL_96KHZ
R				R/W	R/W		R/W

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	1111	These bits are reserved
3	POWER_SAVE_DOWN	R/W	0	0: when have clock fault, device will not shut down analog and digital, only shut down driver 1: when have clock fault, device will shut down analog and digital and driver
2-1	PLL_CLK_DIV	R/W	0	00: high PLL frequency 01: middle PLL frequency 10: low PLL frequency 11: low PLL frequency
0	REAL_96KHZ	R/W	0	0: 48kHz internal processing 1: 96kHz internal processing

12.1.7 Register 7 I2S_DATA_FORMAT1 (Offset=7h) [Reset=0x02]

7	6	5	4	3	2	1	0
44K_INPUT	44K_EN	I2S_DATA_FORMATI		I2S_FSYNC_PULSE		I2S_WORD_LENGTH	
R/W	R/W	R/W		R/W		R/W	

Bit	Field	Type	Reset	Description
7	44K_INPUT	R/W	0	0: 48K/96K/192K input 1: 44.1K/88.2K/176.4K input
6	44K_EN	R/W	0	0: disable 44k input 1: enable 44k input

Bit	Field	Type	Reset	Description
5-4	I2S_DATA_FORMAT	R/W	00	00: I2S 01: TDM/DSP 10: RTJ 11: LTJ
3-2	I2S_FSYNC_PULSE	R/W	00	01: FSYNC pulse <8 BCLK. If the high width of LRCLK/FSYNC in TDM/DSP mode is less than 8 cycles of BCLK, these two bits need set to 01. Others: These bits are reserved
1-0	I2S_WORD_LENGTH	R/W	10	I2S Word length. These bits control both input and output audio interface sample word lengths for DAC operation. 00: 16 bits 01: 20 bits 10: 24 bits 11: 32 bits

12.1.8 Register 8 I2S_DATA_FORMAT2 (Offset=8h) [Reset=0x00]

7	6	5	4	3	2	1	0
I2S_LEFT_BITS_SHIFT							
R/W							

Bit	Field	Type	Reset	Description
7-0	I2S_LEFT_BIT_SHIFT	R/W	00000000	Control the offset of Left Channel audio data in the audio frame for both input and output. The offset is defined as the number of BLCK from the starting (MSB) of audio frame to the starting of the desired audio sample. 00000000: offset = 0 BCLK (no offset) 00000001: offset = 1 BCLK ……… 11111111: offset = 256 BCLK

12.1.9 Register 9 I2S_DATA_FORMAT3 (Offset=9h) [Reset=0x00]

7	6	5	4	3	2	1	0
RESERVED							
R							

Bit	Field	Type	Reset	Description
7-0	RESERVED	R	00000000	These bits are reseved.

12.1.10 Register 10 GPIO1_CTRL (Offset=0Ah) [Reset=0x29]

7	6	5	4	3	2	1	0
RESERVED		GPIO1_OE	GPIO1_FUNC_SEL				
R		R/W	R/W				

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	00	These bits are reserved
5	GPIO1_OE	R/W	1	0: GPIO1 is input 1: GPIO1 is output
4-0	GPIO1_FUNC_SEL	R/W	01001	DEFAULT is SDOUT 0000: off(low) 0001: digital off 0010: analog off 0011: driver off 0100: mute right 0101: mute left 0110: clock invalid flag(clock error or clock missing) 0111: pll lock flag 1000: GPIO1 as WARNZ output 1001: serial audio interface data output(SDOUT) 1011: GPIO1 as FAULTZ output 1100: resetz

12.1.11 Register 11 GPIO2_CTRL (Offset=0Bh) [Reset=0x2B]

7	6	5	4	3	2	1	0
RESERVED		GPIO2_OE	GPIO1_FUNC_SEL				
R		R/W	R/W				

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	00	These bits are reserved
5	GPIO2_OE	R/W	1	0: GPIO2 is input 1: GPIO2 is output
4-0	GPIO2_FUNC_SEL	R/W	01011	DEFAULT is FAULT pin 0000: off(low) 0001: digital off 0010: analog off 0011: driver off 0100: mute right 0101: mute left 0110: clock invalid flag(clock error or clock missing) 0111: pll lock flag

Bit	Field	Type	Reset	Description
				1000: gpio1 as WARNZ output 1001: serial audio interface data output(SDOUT) 1011: GPIO2 as FAULTZ output 1100: resetz

12.1.12 Register 12 GPIO1_FAULT_SEL (Offset=0Ch) [Reset=0xFF]

7	6	5	4	3	2	1	0
CLIP	OTW	OTSD	CLK_FAULT	PVDD_UV	PVDD_OV	DC	OC
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Field	Type	Reset	Description
7	CLIP	R/W	1	0: Mask; 1: Report
6	OTW	R/W	1	0: Mask; 1: Report
5	OTSD	R/W	1	0: Mask; 1: Report
4	CLK_FAULT	R/W	1	0: Mask; 1: Report
3	PVDD_UV	R/W	1	0: Mask; 1: Report
2	PVDD_OV	R/W	1	0: Mask; 1: Report
1	DC	R/W	1	0: Mask; 1: Report
0	OC	R/W	1	0: Mask; 1: Report

12.1.13 Register 13 GPIO2_FAULT_SEL (Offset=0Dh) [Reset=0xFF]

7	6	5	4	3	2	1	0
CLIP	OTW	OTSD	CLK_FAULT	PVDD_UV	PVDD_OV	DC	OC
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Field	Type	Reset	Description
7	CLIP	R/W	1	0: Mask; 1: Report
6	OTW	R/W	1	0: Mask; 1: Report
5	OTSD	R/W	1	0: Mask; 1: Report
4	CLK_FAULT	R/W	1	0: Mask; 1: Report
3	PVDD_UV	R/W	1	0: Mask; 1: Report
2	PVDD_OV	R/W	1	0: Mask; 1: Report
1	DC	R/W	1	0: Mask; 1: Report
0	OC	R/W	1	0: Mask; 1: Report

12.1.14 Register 14 SS_CTRL (Offset=0Eh) [Reset=0x00]

7	6	5	4	3	2	1	0
RESERVED						RDM_EN	TRI_EN
R						R/W	R/W

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	00000	These bits are reserved
1	RDM_EN	R/W	0	0: Random SS disable 1: Random SS enable
0	TRI_EN	R/W	0	0: Triangle SS disable 1: Triangle SS enable

12.1.15 Register 15 VOLUME_CTRL_L (Offset=0Fh) [Reset=0xD0]

7	6	5	4	3	2	1	0
VOL_L							
R/W							

Bit	Field	Type	Reset	Description
7-0	VOL_L	R/W	11010000	Volume control for left channel. 00000000: -104dB .... 11010000: 0dB 11010001: 0.5dB 11111111: 24dB

12.1.16 Register 16 VOLUME_CTRL_R (Offset=10h) [Reset=0xD0]

7	6	5	4	3	2	1	0
VOL_R							
R/W							

Bit	Field	Type	Reset	Description
7-0	VOL_R	R/W	11010000	Volume control for right channel. 00000000: -104dB .... 11010000: 0dB 11010001: 0.5dB 11111111: 24dB

12.1.17 Register 17 MISC_CTRL (Offset=11h) [Reset=0x03]

7	6	5	4	3	2	1	0
RESERVED					OTSD_AUTO_REC	GPIO2_FAULT_LATCH	GPIO1_FAULT_LATCH
R					R/W	R/W	R/W

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	0000	
2	OTSD_AUTO_REC	R/W	0	0: OT auto-recovery disable 1: OT auto-recovery enable
1	GPIO2_FAULT_LATCH	R/W	1	0: GPIO2 report fault not latched 1: GPIO2 report fault latched
0	GPIO1_FAULT_LATCH	R/W	1	0: GPIO1 report fault not latched 1: GPIO1 report fault latched

12.1.18 Register 18 I2S_CLK_FORMAT_RPT1 (Offset=12h) [Reset=0x00]

7	6	5	4	3	2	1	0
RESERVED		BCLK_RATIO_HIGH		FS_DET			
R		R		R			

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	00	These bits are reserved
5-4	BCLK_RATIO_HIGH	R	00	These bits indicate the BCLK ratio, the number of BCLK in one audio frame. BCLK=32FS-512FS MSB Bit [9-8].
3-0	FS_DET	R	0000	These bits indicate the currently detected audio sample rate. 0110: 32KHZ 1000: 44.1KHZ 1001: 48KHZ 1010: 88.2KHZ 1011: 96KHZ 1100: 176.4KHZ 1101: 192KHZ

12.1.19 Register 19 I2S_CLK_FORMAT_RPT2 (Offset=13h) [Reset=0x00]

7	6	5	4	3	2	1	0
BCLK_RATIO							
R							

Bit	Field	Type	Reset	Description
7-0	BCLK_RATIO	R	00000000	These bits indicate the BCLK ratio, the number of BCLK in one audio frame. 00000000: 00000001: … 11111111:

12.1.20 Register 20 DIEID_RPT (Offset=15h) [Reset=0x00]

7	6	5	4	3	2	1	0
DIEID_RPT							
R							

Bit	Field	Type	Reset	Description
7-0	DIE_ID	R	00000000	DIE ID

12.1.21 Register 21 STATE_RPT (Offset=16h) [Reset=0x00]

7	6	5	4	3	2	1	0
RESERVED						STATE_RPT	
R						*R*	

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	000000	These bits are reserved
1-0	STATE_RPT	R	00	00: Digital Off 01: Analog Off 10: Driver Off (Hiz) 11: Play

12.1.22 Register 22 FAULT_RPT1(Offset=17h) [Reset=0x00]

7	6	5	4	3	2	1	0
RESERVED	OTSD	PVDD_OV	PVDD_UV	CH2_DC	CH1_DC	CH2_OC	CH1_OC
R	R	R	R	R	R	R	R

Bit	Field	Type	Reset	Description
7	RESERVED	R	0	This bit is reserved
6	OTSD	R	0	0: Normal 1: Over temperature shutdown fault report
5	PVDD_OV	R	0	0: Normal 1: PVDD over-voltage fault report
4	PVDD_UV	R	0	0: Normal 1: PVDD under-voltage fault report
3	CH2_DC	R	0	0: Normal 1: CH2 speaker DC fault report
2	CH1_DC	R	0	0: Normal 1: CH1 speaker DC fault report
1	CH2_OC	R	0	0: Normal 1: CH2 over-current fault report
0	CH1_OC	R	0	0: Normal 1: CH1 over-current fault report

12.1.23 Register 23 FAULT_RPT2(Offset=18h) [Reset=0x00]

7	6	5	4	3	2	1	0
RESERVED					CLK_FAULT	RESERVED	
R					R	R	

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	00000	This bit is reserved
2	CLK_FAULT	R	0	0: Normal 1: Clock fault report
1-0	RESERVED	R	0	This bit is reserved

12.1.24 Register 24 FAULT_RPT3(Offset=19h) [Reset=0x00]

7	6	5	4	3	2	1	0
RESERVED					CH2_CLIP	CH1_CLIP	OTW
R					R	R	R

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	00000	This bit is reserved
2	CH2_CLIP	R	0	0: Normal 1: Channel 2 clipping
1	CH1_CLIP	R	0	0: Normal 1: Channel 1 clipping
0	OTW	R	0	0: Normal 1: Over temperature warning

12.1.25 Register 25 GPIO_PP_OD_CTRL (Offset=27h) [Reset=0x00]

7	6	5	4	3	2	1	0
RESERVED				GPIO3_OD	GPIO2_OD	GPIO1_OD	RESERVED
R				RW	RW	RW	RW

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	00000	These bits are reserved
3	GPIO3_OD	RW	0	0: Disabled 1: Enabled
2	GPIO2_OD	RW	0	0: Disabled 1: Enabled
1	GPIO1_OD	RW	0	0: Disabled 1: Enabled
0	RESERVED	R	0	0: Disabled 1: Enabled

12.1.25 Register 26 DIG_DSP_CTRL (Offset=28h) [Reset=0x00]

7	6	5	4	3	2	1	0
RESERVED				DRC_BP	Lookahead_BP	Class-H_BP	Class-H POST_EN
R				RW	RW	RW	RW

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	00000	These bits are reserved
3	DRC_BP	RW	0	0: DRC enabled 1: Bypass DRC
2	Lookahead_BP	RW	0	0: Lookahead Buffer enabled

Bit	Field	Type	Reset	Description
				1: Bypass Lookahead Buffer
1	Class-H_BP	RW	0	0: Class-H enabled 1: Disable Class-H
0	Class-H POST_EN	RW	0	0: Disabled 1: Class-H Post Enable

12.1.25 Register 27 XOR_CHECKSUM(Offset=7Eh) [Reset=0x00]

7	6	5	4	3	2	1	0
XOR_CHECKSUM							
R							

Bit	Field	Type	Reset	Description
7-0	XOR_CHECKSUM	R	0	XOR checksum result

12.1.26 Register 28 CRC_CHECKSUM(Offset=7Fh) [Reset=0x00]

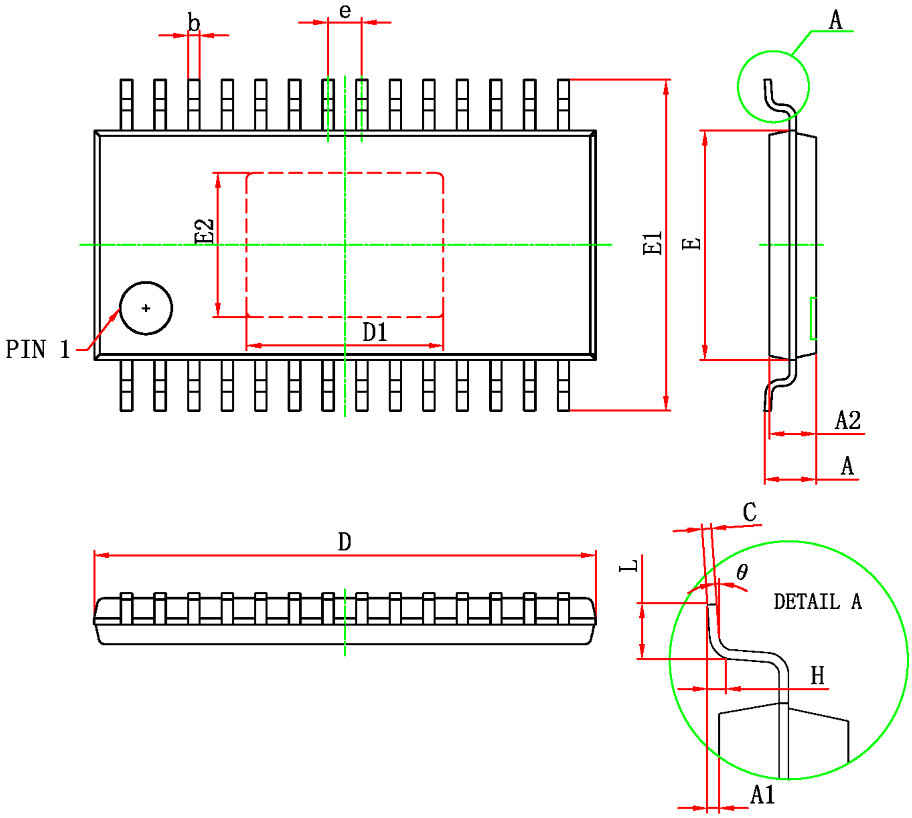
7	6	5	4	3	2	1	0
CRC_CHECKSUM							
R							

Bit	Field	Type	Reset	Description
7-0	CRC_CHECKSUM	R	0	CRC checksum result

14. Package Dimensions

Orderable Device	Package Type	MPQ	MOQ	Eco Plan	MSL Level	Device Marking
ACM8625P	TSSOP28 Tape and Reel	3000	3000	RoHS Compliant Lead-Free Finish	MSL3	ACM8625P

TSSOP28/PP PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
D	9. 600	9. 800	0. 378	0. 386
D1	3. 710	3. 910	0. 146	0. 154
E	4. 300	4. 500	0. 169	0. 177
b	0. 190	0. 300	0. 007	0. 012
c	0. 090	0. 200	0. 004	0. 008
E1	6. 250	6. 550	0. 246	0. 258
E2	2. 700	2. 900	0. 106	0. 122
A		1. 100		0. 043
A2	0. 800	1. 000	0. 031	0. 039
A1	0. 020	0. 150	0. 001	0. 006
e	0. 65 （BSC）		0. 026 (BSC)	
L	0. 500	0. 700	0. 02	0. 028
H	0.25(TYP)		0.01(TYP)	
θ	1°	7°	1°	7°