

AM4362N-T1-PF-VB Datasheet N-Channel 30-V (D-S) MOSFET

PRODUCT SUMMARY						
V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A) ^a	Q _g (Typ.)			
30	0.004 at V _{GS} = 10 V	18	6.8 nC			
	0.005 at V _{GS} = 4.5 V	16	0.0110			

SO-8

Top View

8 D

D

6 D

5 D

S

S

S

G

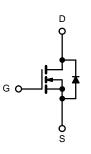
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FEATURES

- Halogen-free
- TrenchFET[®] Power MOSFET
- Optimized for High-Side Synchronous Rectifier Operation
- 100 % R_g Tested
- 100 % UIS Tested

APPLICATIONS

Notebook CPU Core
High-Side Switch



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS	S T _A = 25 °C, unles	s otherwise no	ted		
Parameter		Symbol	Limit	Unit	
Drain-Source Voltage	V _{DS}	30	V		
Gate-Source Voltage		V _{GS}			± 20
	T _C = 25 °C		18		
Continuous Drain Current (T _J = 150 °C)	T _C = 70 °C		16		
$Continuous Drain Current (1) = 150^{\circ} C)$	T _A = 25 °C	I _D –	15 ^{b, c}	٨	
	T _A = 70 °C		13 ^{b, c}		
Pulsed Drain Current		I _{DM}	50	A	
Continuous Source-Drain Diode Current	T _C = 25 °C	1	3.8		
	T _A = 25 °C	I _S –	2.1 ^{b, c}		
Single Pulse Avalanche Current	L = 0.1 mH	I _{AS}	22	1	
L =		E _{AS}	24	mJ	
	T _C = 25 °C		4.5		
Maximum Davias Disaination	T _C = 70 °C	Б	2.8	14/	
Maximum Power Dissipation	T _A = 25 °C	P _D –	2.5 ^{b, c}	W	
	T _A = 70 °C		1.6 ^{b, c}		
Operating Junction and Storage Temperature Ra	T _J , T _{stg}	- 55 to 150	°C		

THERMAL RESISTANCE RATINGS						
Parameter		Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient ^{b, d}	$t \le 10 \text{ s}$	R _{thJA}	38	50	°C/W	
Maximum Junction-to-Foot (Drain)	Steady State	R _{thJF}	22	28		

Notes:

a. Base on T_C = 25 °C.

b. Surface Mounted on 1" x 1" FR4 board.

c. t = 10 s. d. Maximum under Steady State conditions is 85 °C/W.

SPECIFICATIONS T_{J} = 25 °C, unless otherwise noted							
Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static							
Drain-Source Breakdown Voltage	V _{DS}	$V_{GS} = 0 V, I_{D} = 250 \mu A$	30			V	
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	I _D = 250 μA		28		mV/°C	
V _{GS(th)} Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	iΒ = 200 μA		- 6			
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_D = 250 \ \mu A$	1.0		3.0	V	
Gate-Source Leakage	I _{GSS}	$V_{DS} = 0 V, V_{GS} = \pm 20 V$			± 100	nA	
Zara Cata Valtaga Drain Current	1	$V_{DS} = 30 \text{ V}, \text{ V}_{GS} = 0 \text{ V}$			1	μA	
Zero Gate Voltage Drain Current	IDSS	V_{DS} = 30 V, V_{GS} = 0 V, T_{J} = 55 °C			10		
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$	20			А	
	Б	V _{GS} = 10 V, I _D = 11 A		0.004		Ω	
Drain-Source On-State Resistance ^a	R _{DS(on)}	$V_{GS} = 4.5 \text{ V}, \text{ I}_{D} = 10 \text{ A}$		0.005			
Forward Transconductance ^a	9 _{fs}	V _{DS} = 15 V, I _D = 11 A		52		S	
Dynamic ^b					I	1	
Input Capacitance	C _{iss}			820		pF	
Output Capacitance	C _{oss}	V _{DS} = 15 V, V _{GS} = 0 V, f = 1 MHz		195			
Reverse Transfer Capacitance	C _{rss}			73			
Total Gate Charge		V _{DS} = 15 V, V _{GS} = 10 V, I _D = 11 A		15	23	nC	
	Qg			6.8	10.2		
Gate-Source Charge	Q _{gs}	V_{DS} = 15 V, V_{GS} = 5 V, I_{D} = 11 A		2.5			
Gate-Drain Charge	Q _{gd}			2.3			
Gate Resistance	Rg	f = 1 MHz	0.36	1.8	3.6	Ω	
Turn-On Delay Time	t _{d(on)}			16	24	-	
Rise Time	t _r	V_{DD} = 15 V, R_L = 1.4 Ω		12	18		
Turn-Off Delay Time	t _{d(off)}	${\rm I}_{\rm D}{\cong}9$ A, ${\rm V}_{\rm GEN}$ = 4.5 V, ${\rm R}_{\rm g}$ = 1 Ω		16	24		
Fall Time	t _f			10	20		
Turn-On Delay Time	t _{d(on)}			8	16	ns	
Rise Time	t _r	V_{DD} = 15 V, R_L = 1.4 Ω		10	20	-	
Turn-Off Delay Time	t _{d(off)}	$I_D \cong$ 9 A, V_{GEN} = 10 V, R_g = 1 Ω		16	24		
Fall Time	t _f			8	15		
Drain-Source Body Diode Characteris	tics						
Continuous Source-Drain Diode Current	ا _S	T _C = 25 °C			25	^	
Pulse Diode Forward Current ^a	I _{SM}				50	A	
Body Diode Voltage	V _{SD}	I _S = 9 A		0.8	1.2	V	
Body Diode Reverse Recovery Time	t _{rr}			15	30	ns	
Body Diode Reverse Recovery Charge	Q _{rr}			6	12	nC	
Reverse Recovery Fall Time	t _a	$I_F = 9 \text{ A}, \text{ dI/dt} = 100 \text{ A/}\mu\text{s}, \text{ T}_J = 25 ^\circ\text{C}$		8			
Reverse Recovery Rise Time	t _b			7	1	ns	

Notes:

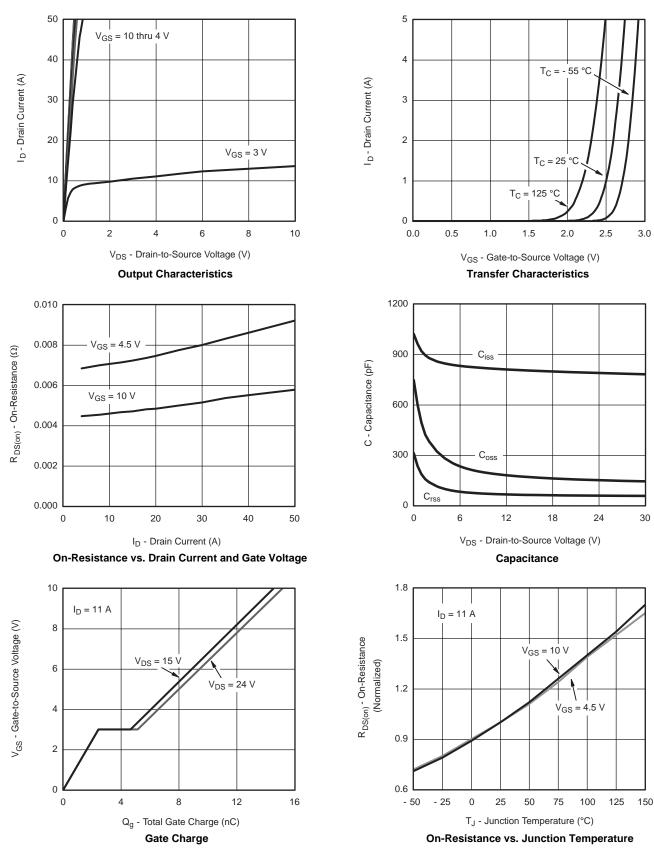
a. Pulse test; pulse width \leq 300 µs, duty cycle \leq 2 %.

b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

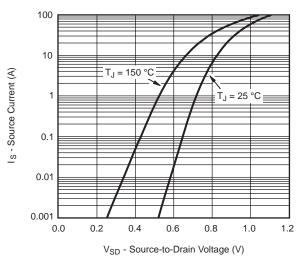
VBsemi Bsemi.com

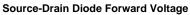


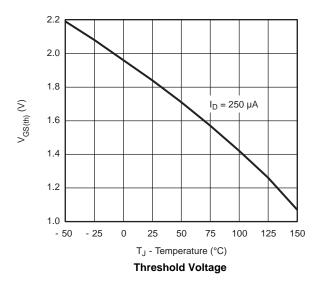


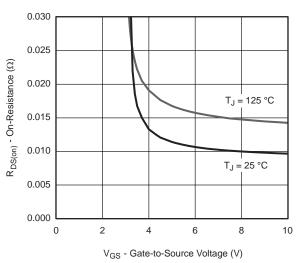
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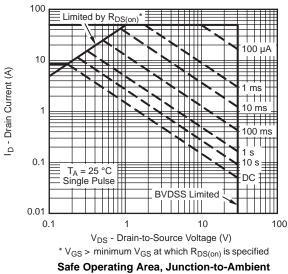




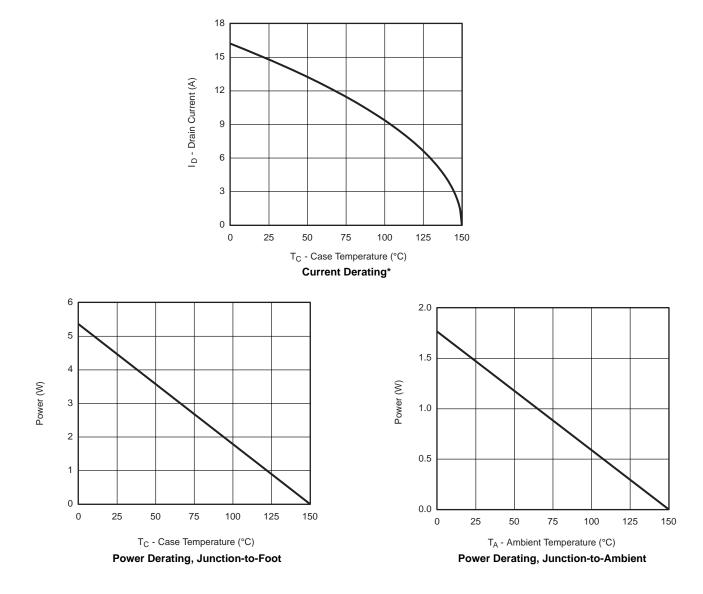
On-Resistance vs. Gate-to-Source Voltage





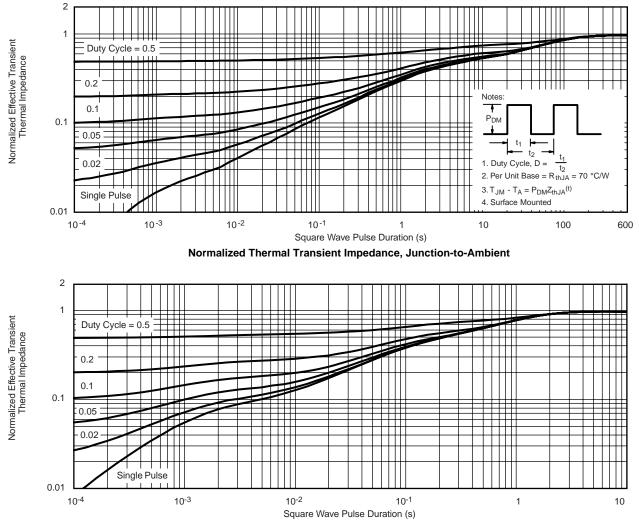






* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.





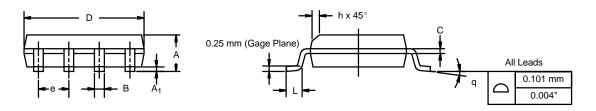
Normalized Thermal Transient Impedance, Junction-to-Foot



SOIC (NARROW): 8-LEAD

JEDEC Part Number: MS-012





	MILLIM	IETERS	INCHES		
DIM	Min	Max	Min	Max	
A	1.35	1.75	0.053	0.069	
A ₁	0.10	0.20	0.004	0.008	
В	0.35	0.51	0.014	0.020	
С	0.19	0.25	0.0075	0.010	
D	4.80	5.00	0.189	0.196	
E	3.80	4.00	0.150	0.157	
е	1.27 BSC		0.050 BSC		
н	5.80	6.20	0.228	0.244	
h	0.25	0.50	0.010	0.020	
L	0.50	0.93	0.020	0.037	
q	0°	8°	0°	8°	
S	0.44	0.64	0.018	0.026	
ECN: C-06527-Rev. I, 11-Sep-06 DWG: 5498					



RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads Dimensions in Inches/(mm)



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