

# AM4990NE-T1-PF-VB Datasheet Dual N-Channel 100-V (D-S) MOSFET

PRODUCT SUMMARY					
V <sub>DS</sub> (V)	$R_{DS(on)}\left(\Omega\right)$	I <sub>D</sub> (A) <sup>d</sup>	Q <sub>g</sub> (Typ.)		
100	0.063 at V <sub>GS</sub> = 10 V	5.8	9 nC		
	0.084 at V <sub>GS</sub> = 6 V	4.8	9110		

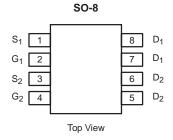
#### **FEATURES**

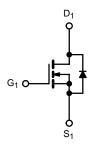
- Halogen-free According to IEC 61249-2-21 Available
- TrenchFET<sup>®</sup> Power MOSFET
- 100 % UIS Tested

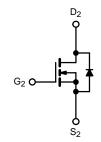
# RoHS COMPLIANT HALOGEN

#### **APPLICATIONS**

- High Frequency Boost Converter
- LED Backlight for LCD TV







N-Channel MOSFET

N-Channel MOSFET

<b>ABSOLUTE MAXIMUM RATIN</b>	IGS T <sub>A</sub> = 25 °C,	unless other	wise noted		
Parameter		Symbol	Limit	Unit	
Drain-Source Voltage	V <sub>DS</sub>	100	V		
Gate-Source Voltage	$V_{GS}$	± 20	V		
	T <sub>C</sub> = 25 °C		5.8		
Continuous Drain Current (T <sub>.1</sub> = 150 °C)	T <sub>C</sub> = 70 °C	1 , [	4.4		
Continuous Diam Current (1) = 130 °C)	T <sub>A</sub> = 25 °C	l o	3.4 <sup>a, b</sup>		
	T <sub>A</sub> = 70 °C		2.5 <sup>a, b</sup>	Α	
Pulsed Drain Current	I <sub>DM</sub>	20	A		
Ocaliana Company Basis Bis de Ocasas	T <sub>C</sub> = 25 °C	I-	5		
Continuous Source-Drain Diode Current	T <sub>A</sub> = 25 °C	ls -	2.1 <sup>a, b</sup>		
Single Avalanche Current	L = 0.1 mH	I <sub>AS</sub>	19		
Single Avalanche Energy L = 0.1 mH		E <sub>AS</sub>	18	mJ	
	T <sub>C</sub> = 25 °C		5		
Maximum Dawar Dissination	T <sub>C</sub> = 70 °C	1 6	3.2	w	
Maximum Power Dissipation	T <sub>A</sub> = 25 °C	P <sub>D</sub>	2.5 <sup>a, b</sup>	VV	
	T <sub>A</sub> = 70 °C	1	1.6 <sup>a, b</sup>		
Operating Junction and Storage Temperatur	T <sub>J</sub> , T <sub>stq</sub>	- 55 to 150	°C		

THERMAL RESISTANCE RATINGS							
Parameter	Symbol	Typical	Maximum	Unit			
Maximum Junction-to-Ambient <sup>b, c</sup>	t ≤ 10 s	$R_{thJA}$	37	50	°C/W		
Maximum Junction-to-Foot (Drain)	Steady State	R <sub>thJF</sub>	17	21	O/ VV		

#### Notes

- a. Surface Mounted on 1" x 1" FR4 board.
- b. t = 10 s.
- c. Maximum under Steady State conditions is 85 °C/W.
- d.  $T_C = 25$  °C.



Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit
Static						•
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	100			V
V <sub>DS</sub> Temperature Coefficient	$\Delta V_{DS}/T_{J}$	I = 250 uA		120		mV/°C
V <sub>GS(th)</sub> Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	$I_D = 250 \mu A$		- 9		
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}$ , $I_D = 250 \mu A$	2		4.5	V
Gate-Source Leakage	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA
Zana Oata Walkana Buain Ourseat	I <sub>DSS</sub>	V <sub>DS</sub> = 100 V, V <sub>GS</sub> = 0 V			1	
Zero Gate Voltage Drain Current		V <sub>DS</sub> = 100 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55 °C	<del>                                     </del>		10	μΑ
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$	20			Α
_		$V_{GS} = 10 \text{ V}, I_D = 3.4 \text{ A}$		0.063		+
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	$V_{GS} = 6 \text{ V}, I_D = 2.8 \text{ A}$		0.084	Ω	
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 3.4 A		10		S
Dynamic <sup>b</sup>						I
Input Capacitance	C <sub>iss</sub>			600		pF
Output Capacitance	C <sub>oss</sub>	$V_{DS} = 50 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		90		
Reverse Transfer Capacitance	C <sub>rss</sub>			50		
Total Gate Charge	Q <sub>g</sub>	$V_{DS} = 50 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 3.4 \text{ A}$		13.5	20	
				9	13.5	nC
Gate-Source Charge	$Q_{gs}$	$V_{DS} = 50 \text{ V}, V_{GS} = 6 \text{ V}, I_D = 3.4 \text{ A}$		3		
Gate-Drain Charge	Q <sub>gd</sub>			4.6		
Gate Resistance	$R_{g}$	f = 1 MHz		1		Ω
Turn-On Delay Time	t <sub>d(on)</sub>			15	25	
Rise Time	t <sub>r</sub>	$V_{DD}$ = 50 V, $R_L$ = 14.3 $\Omega$		12	20	-
Turn-Off Delay Time	t <sub>d(off)</sub>	$I_D\cong 3.5$ A, $V_{GEN}$ = 6 V, $R_g$ = 1 $\Omega$		12	20	
Fall Time	t <sub>f</sub>			10	15	
Turn-On Delay Time	t <sub>d(on)</sub>			10	15	ns
Rise Time	t <sub>r</sub>	$V_{DD}$ = 50 V, $R_L$ = 14.3 $\Omega$		12	20	
Turn-Off Delay Time	t <sub>d(off)</sub>	$I_D\cong 3.5$ A, $V_{GEN}$ = 10 V, $R_g$ = 1 $\Omega$		15	25	
Fall Time	t <sub>f</sub>			10	15	
<b>Drain-Source Body Diode Characteristi</b>	cs					l
Continuous Source-Drain Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25 °C			5	
Pulse Diode Forward Current	I <sub>SM</sub>				20	Α
Body Diode Voltage	$V_{SD}$	I <sub>S</sub> = 3.5 A, V <sub>GS</sub> = 0 V		0.8	1.2	V
Body Diode Reverse Recovery Time	t <sub>rr</sub>			45	70	ns
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>	L 05 A dl/dt 100 A/v- T 05 °C		80	120	nC
Reverse Recovery Fall Time	ta	$I_F = 3.5 \text{ A}, \text{ dI/dt} = 100 \text{ A/}\mu\text{s}, T_J = 25 ^{\circ}\text{C}$		33		
Reverse Recovery Rise Time		t <sub>b</sub>		12		ns

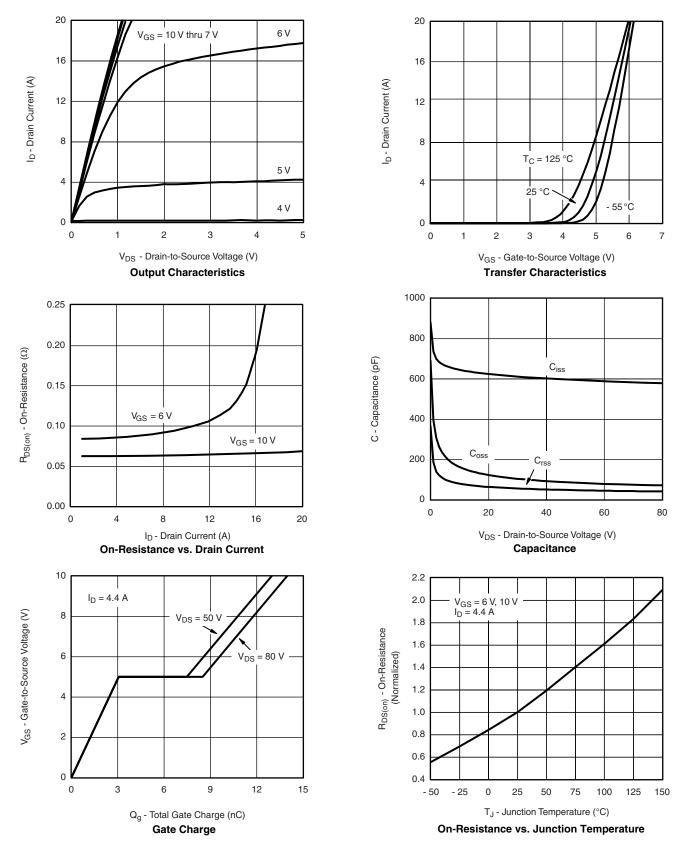
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- a. Pulse test; pulse width  $\leq$  300  $\mu s,$  duty cycle  $\leq$  2 % b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

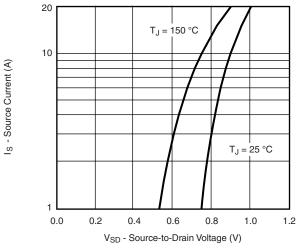


#### TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

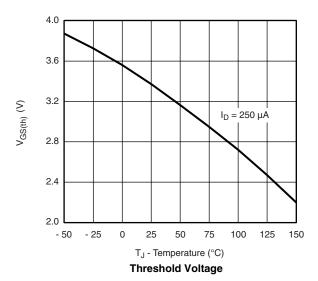


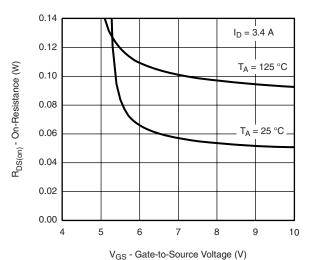


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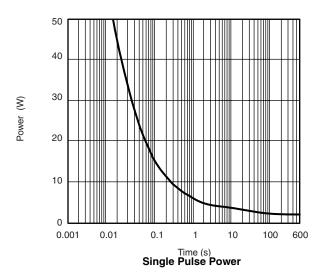


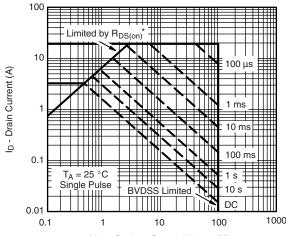
#### Source-Drain Diode Forward Voltage





On-Resistance vs. Gate-to-Source Voltage



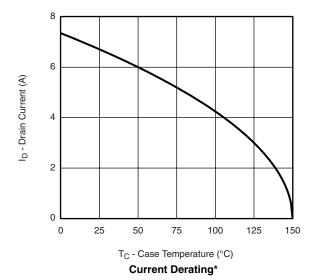


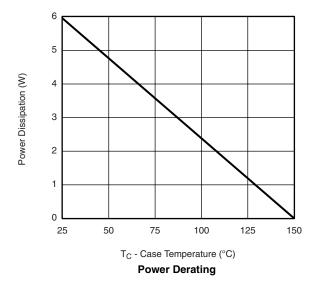
 $\label{eq:VDS} V_{DS} \text{ - Drain-to-Source Voltage (V)} \\ \text{* V}_{GS} \text{ > minimum V}_{GS} \text{ at which } R_{DS(on)} \text{ is specified} \\$ 

Safe Operating Area, Junction-to-Ambient



### TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



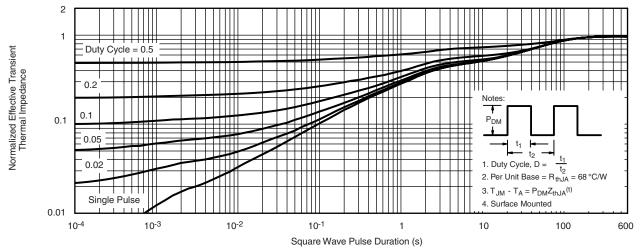


<sup>\*</sup> The power dissipation  $P_D$  is based on  $T_{J(max)} = 150$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

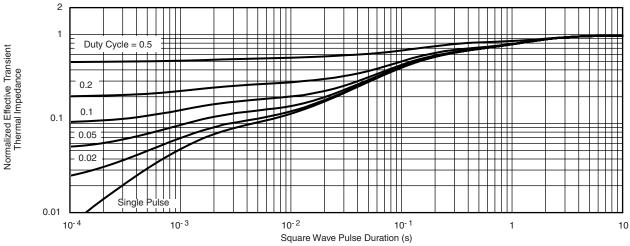
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#### TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



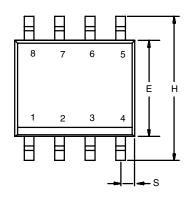
Normalized Thermal Transient Impedance, Junction-to-Ambient

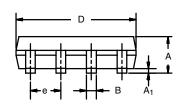


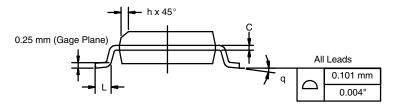
Normalized Thermal Transient Impedance, Junction-to-Foot



SOIC (NARROW): 8-LEAD JEDEC Part Number: MS-012







	MILLIM	IETERS	INC	HES	
DIM	Min	Max	Min	Max	
Α	1.35	1.75	0.053	0.069	
A <sub>1</sub>	0.10	0.20	0.004	0.008	
В	0.35	0.51	0.014	0.020	
С	0.19	0.25	0.0075	0.010	
D	4.80	5.00	0.189	0.196	
E	3.80	4.00	0.150	0.157	
е	1.27 BSC		0.050 BSC		
Н	5.80	6.20	0.228	0.244	
h	0.25	0.50	0.010	0.020	
L	0.50	0.93	0.020	0.037	
q	0°	8°	0°	8°	
S	0.44	0.64	0.018	0.026	
ECN: C 06527 Pay L 11 Cap 06					

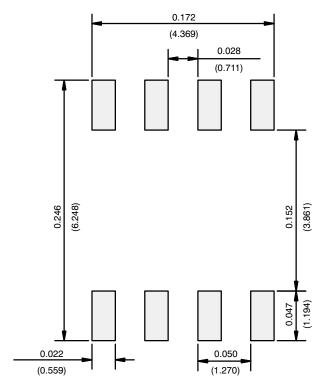
ECN: C-06527-Rev. I, 11-Sep-06

DWG: 5498

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### **RECOMMENDED MINIMUM PADS FOR SO-8**



Recommended Minimum Pads Dimensions in Inches/(mm)



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