

APM9988QA-VB Datasheet

Dual N-Channel 20 V (D-S) MOSFET

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)	Q_g (TYP.)
20	0.0120 at $V_{GS} = 4.5$ V	25	12 nC
	0.0160 at $V_{GS} = 2.5$ V	20	
	0.0190 at $V_{GS} = 1.8$ V	16	

FEATURES

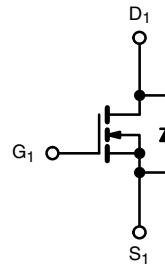
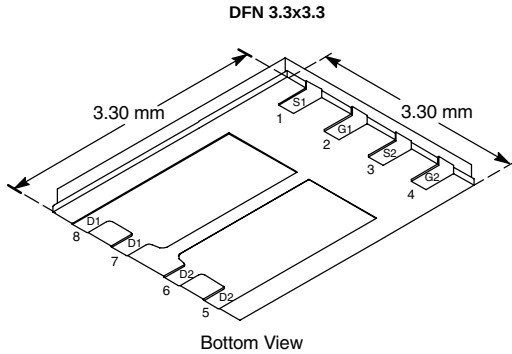
- TrenchFET® power MOSFET

APPLICATIONS

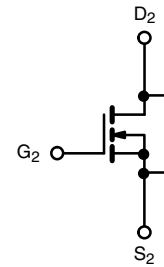
- DC/DC
- Notebook system power
- POL



RoHS
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N-Channel MOSFET



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	20	V
Gate-Source Voltage	V_{GS}	± 8	
Continuous Drain Current ($T_J = 150$ °C)	I_D	25	A
		23.8	
		10 a, b	
		8 a, b	
Pulsed Drain Current	I_{DM}	40	mJ
Continuous Source-Drain Diode Current	I_S	19	
		2.2 a, b	
Single Pulse Avalanche Current	I_{AS}	15	
Single Pulse Avalanche Energy	E_{AS}	11	
Maximum Power Dissipation	P_D	23	W
		14.8	
		2.6 a, b	
		1.7 a, b	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to +150	°C
Soldering Recommendations (Peak Temperature) c, d		260	

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum Junction-to-Ambient	R_{thJA}	38	48	°C/W
Maximum Junction-to-Case (Drain)	R_{thJC}	4.3	5.4	

Notes

- a. Package limited, $T_C = 25$ °C.
 b. Surface Mounted on 1" x 1" FR4 board.
 c. $t = 10$ s.
 d. Maximum under Steady State conditions is 110 °C/W.

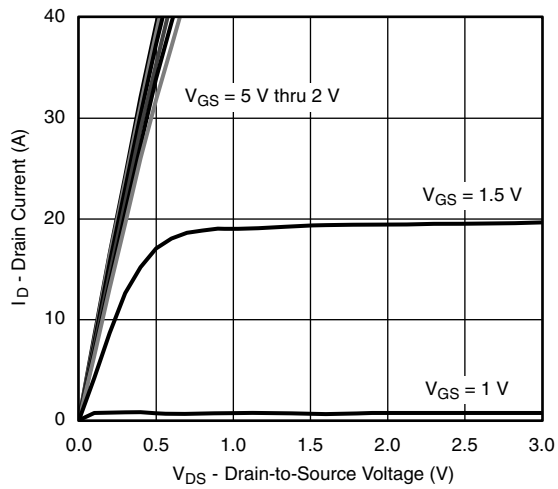
SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	20	-	-	V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	I _D = 250 μA	-	22	-	mV/°C
V _{GS(th)} Temperature Coefficient	ΔV _{GS(th)} /T _J		-	-3	-	
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	0.4	-	1	V
Gate-Source Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 8 V	-	-	± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 20 V, V _{GS} = 0 V	-	-	1	μA
		V _{DS} = 20 V, V _{GS} = 0 V, T _J = 55 °C	-	-	10	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	20	-	-	A
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 4.5 V, I _D = 10 A	-	0.0120		Ω
		V _{GS} = 2.5 V, I _D = 9 A	-	0.0160		
		V _{GS} = 1.8 V, I _D = 8.2 A	-	0.0190		
Forward Transconductance ^a	g _{fs}	V _{DS} = 10 V, I _D = 10 A	-	47	-	S
Dynamic ^b						
Input Capacitance	C _{iss}	V _{DS} = 10 V, V _{GS} = 0 V, f = 1 MHz	-	1220	-	pF
Output Capacitance	C _{oss}		-	180	-	
Reverse Transfer Capacitance	C _{rss}		-	80	-	
Total Gate Charge	Q _g	V _{DS} = 15 V, V _{GS} = 8 V, I _D = 10 A	-	21	32	nC
		V _{DS} = 15 V, V _{GS} = 4.5 V, I _D = 10 A	-	12	18	
Gate-Source Charge	Q _{gs}		-	2	-	
Gate-Drain Charge	Q _{gd}		-	1.3	-	
Gate Resistance	R _g	f = 1 MHz	-	1.8	3.6	Ω
Turn-On Delay Time	t _{d(on)}	V _{DD} = 10 V, R _L = 1.25 Ω I _D ≅ 8 A, V _{GEN} = 4.5 V, R _g = 1 Ω	-	10	15	ns
Rise Time	t _r		-	10	15	
Turn-Off Delay Time	t _{d(off)}		-	35	55	
Fall Time	t _f		-	10	15	
Turn-On Delay Time	t _{d(on)}	V _{DD} = 10 V, R _L = 1.25 Ω I _D ≅ 8 A, V _{GEN} = 8 V, R _g = 1 Ω	-	10	15	
Rise Time	t _r		-	10	15	
Turn-Off Delay Time	t _{d(off)}		-	25	40	
Fall Time	t _f		-	10	15	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C	-	-	19	A
Pulse Diode Forward Current	I _{SM}		-	-	40	
Body Diode Voltage	V _{SD}	I _S = 8 A, V _{GS} = 0 V	-	0.81	1.2	V
Body Diode Reverse Recovery Time	t _{rr}	I _F = 8 A, dI/dt = 100 A/μs, T _J = 25 °C	-	20	30	ns
Body Diode Reverse Recovery Charge	Q _{rr}		-	15	25	nC
Reverse Recovery Fall Time	t _a		-	12.5	-	ns
Reverse Recovery Rise Time	t _b		-	7.5	-	

Notes

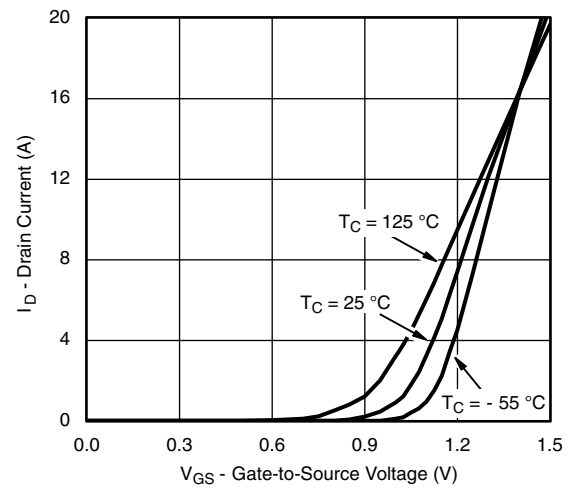
- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$
 b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

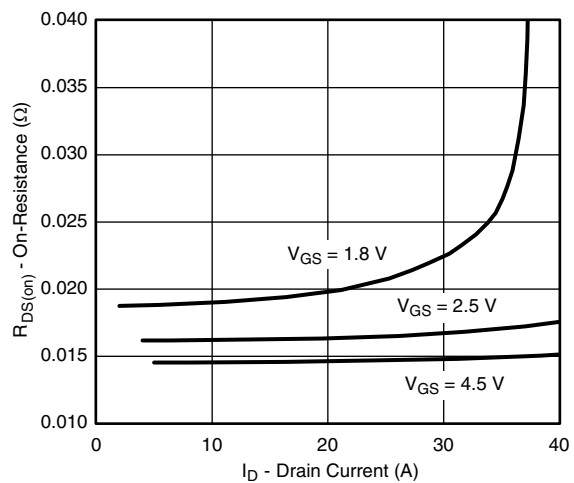
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



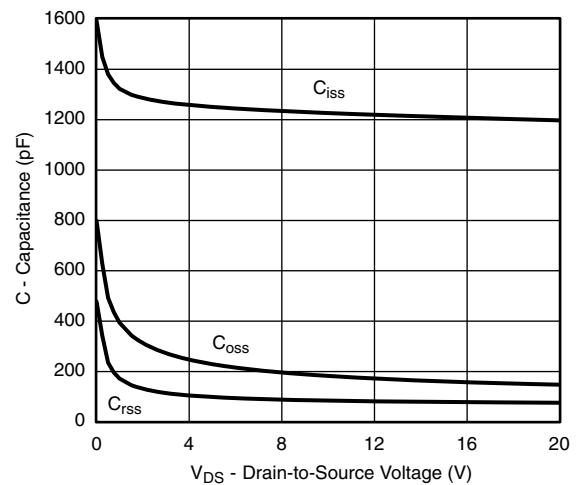
Output Characteristics



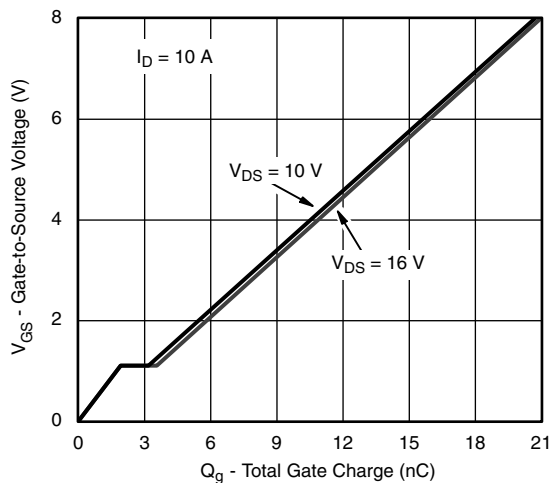
Transfer Characteristics



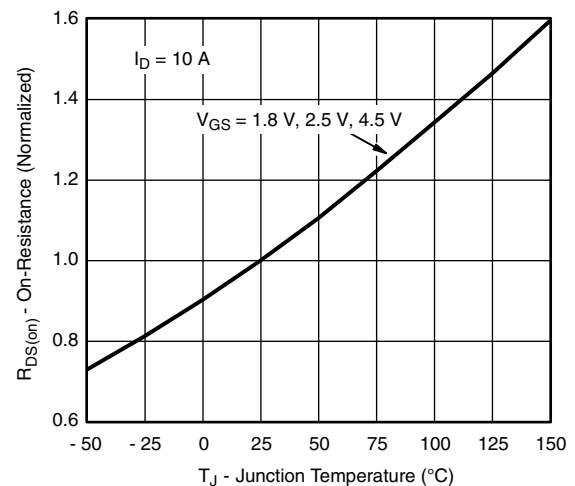
On-Resistance vs. Drain Current and Gate Voltage



Capacitance

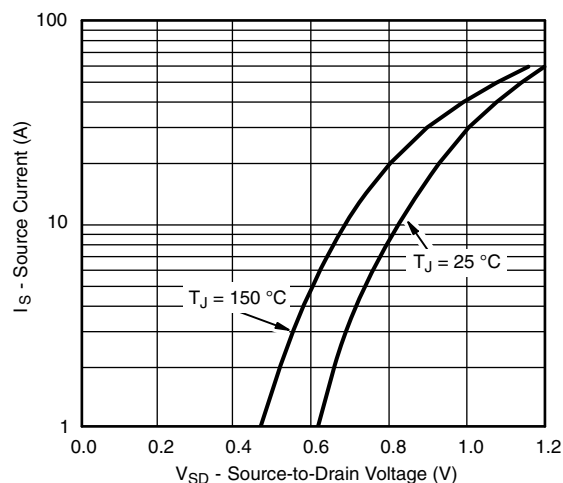


Gate Charge

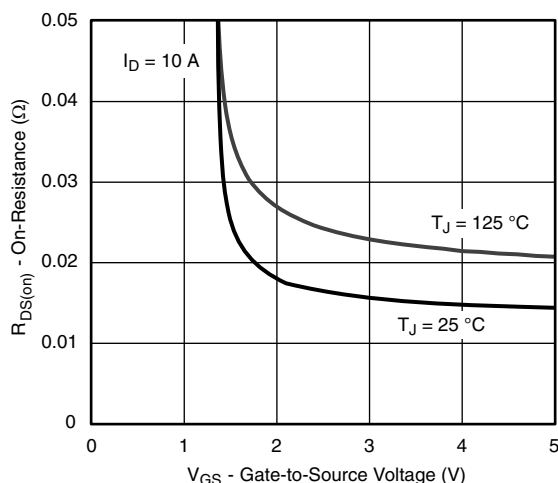


On-Resistance vs. Junction Temperature

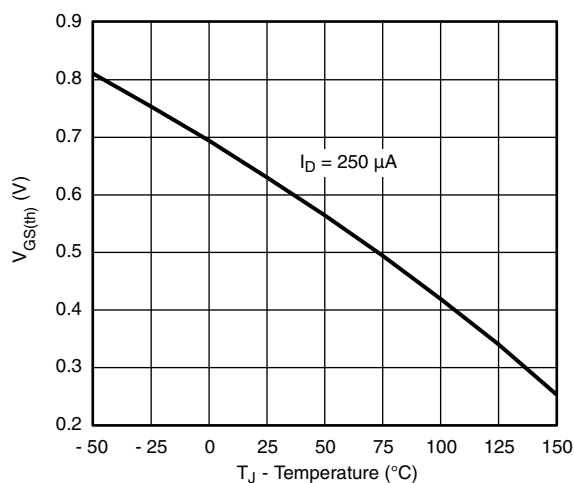
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



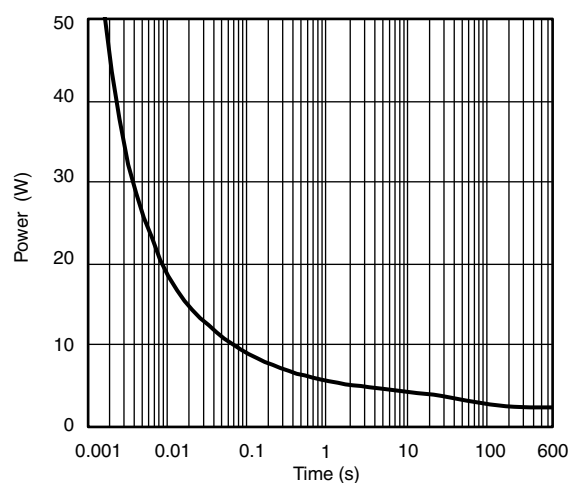
Source-Drain Diode Forward Voltage



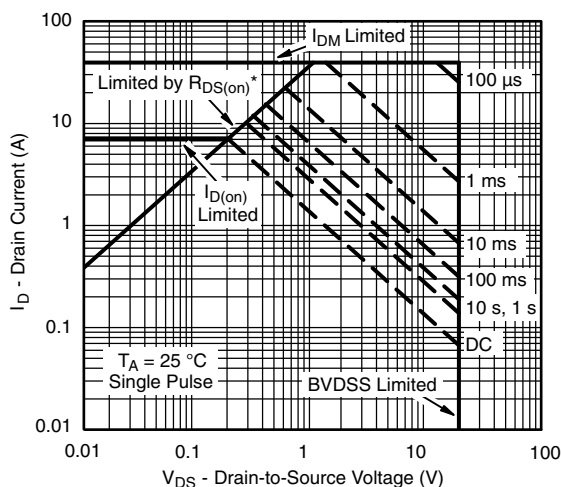
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



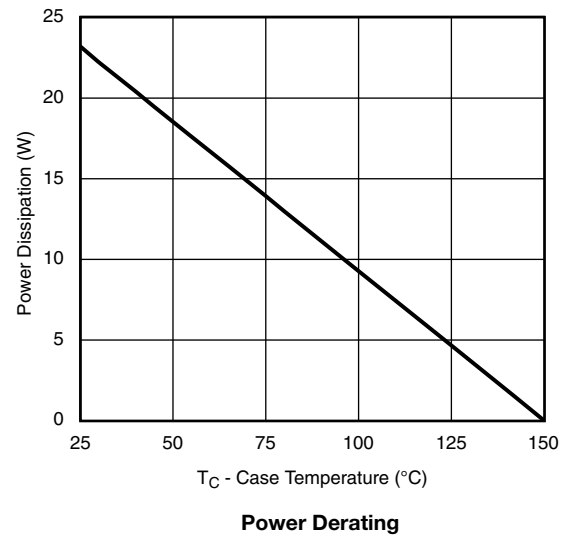
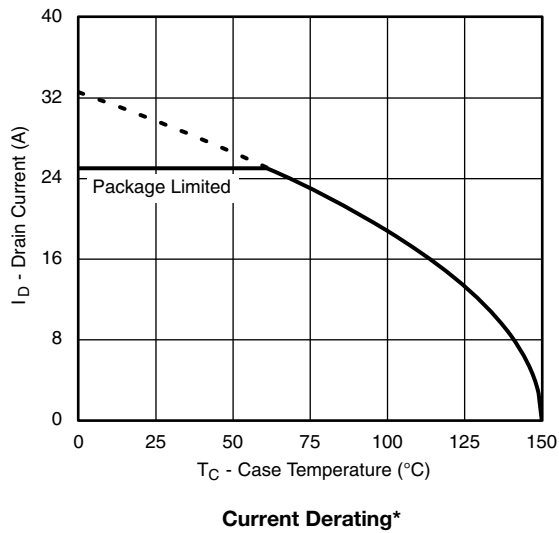
Single Pulse Power, Junction-to-Ambient



* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

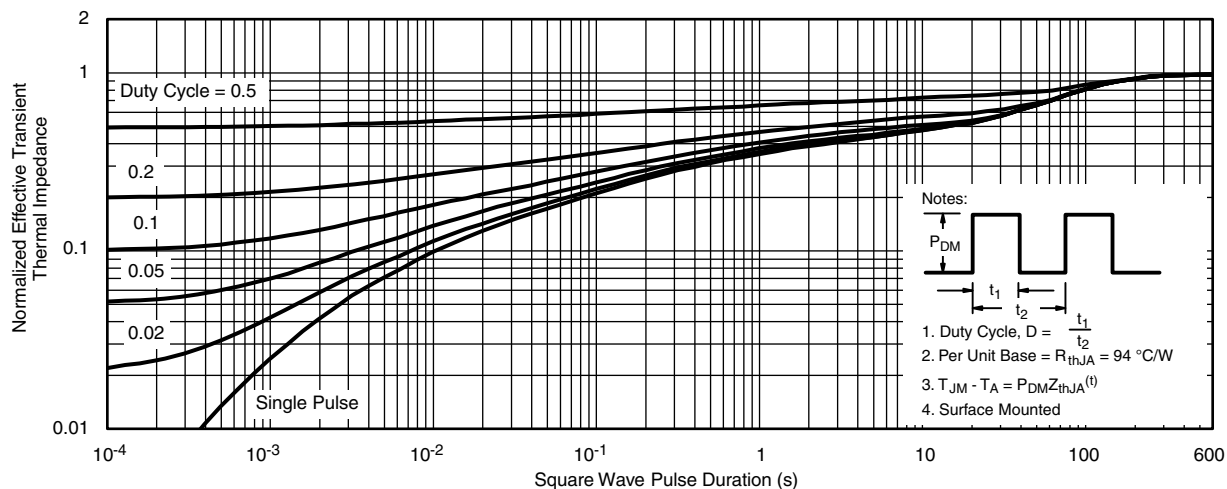
Safe Operating Area, Junction-to-Ambient

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

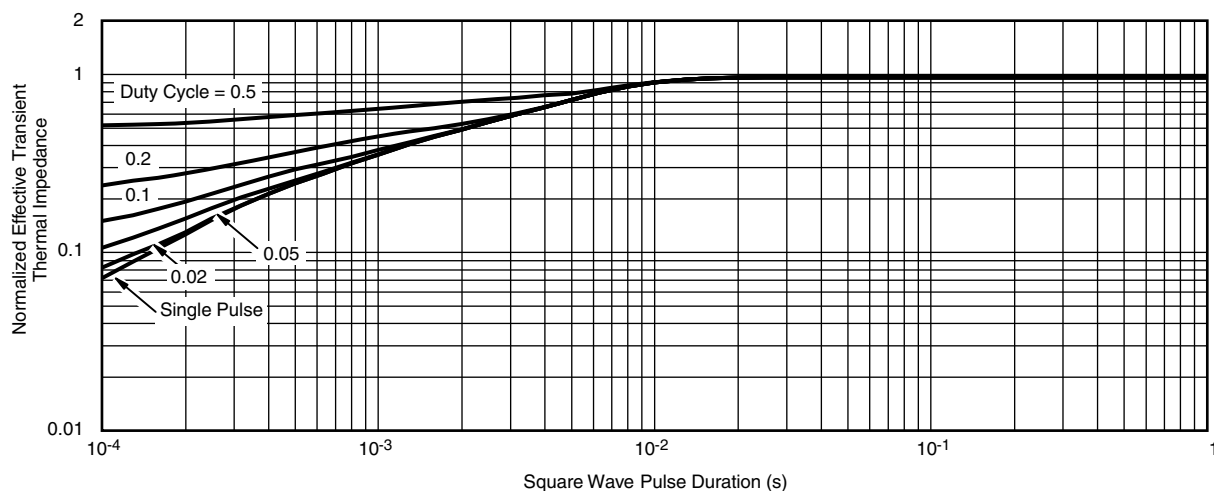


* The power dissipation P_D is based on T_J (max.) = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

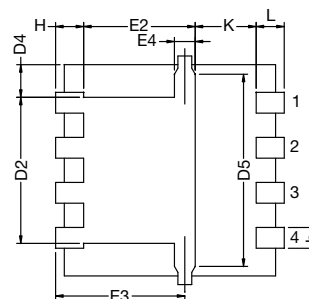
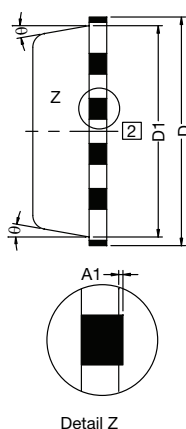
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case



Technical drawing of a four-lane microplate. The diagram shows a rectangular plate with four horizontal lanes labeled 1, 2, 3, and 4 on the right side. Dimensions are indicated by arrows and labels: H is the height of the first lane; $D4$ is the width of the first lane; $D2$ is the height of the second lane; $D3(2x)$ is the width of the second lane; $D1$ is the height of the third lane; $D2$ is the height of the fourth lane; $D6$ is the width of the fourth lane; $K1$ is the height of the fifth lane; $E2$ is the width of the sixth lane; $E4$ is the width of the seventh lane; K is the height of the eighth lane; L is the total width of the plate. A triangle with the letter H is shown on the left side.

Backside view of dual pad

1. Inch will govern
2. Dimensions exclusive of mold gate burrs
3. Dimensions exclusive of mold flash and cutting burrs

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