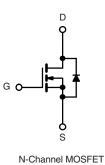


AUIRFR2407TRPBF-VB Datasheet N-Channel 100-V (D-S) MOSFET

PRODUCT SUMMARY					
V _{DS} (V)	R_{DS(on)} (Ω)	I _D (A) ^a	Q _g (Typ.)		
100	0.0185 at V _{GS} = 10 V	45	38 nC		

G D S Top View

TO-252



FEATURES

- TrenchFET[®] Power MOSFET
- + 100 % $\rm R_g$ and UIS Tested

APPLICATIONS

- Primary Side Switch
- Isolated DC/DC Converter



Parameter		Symbol	Limit	Unit	
Drain-Source Voltage	V _{DS}	100	V		
Gate-Source Voltage		V _{GS}	± 20	v	
	T _C = 25 °C		45 ^a		
Continuous Drain Current (T 150 °C)	T _C = 100 °C		30		
Continuous Drain Current ($T_J = 150 \ ^{\circ}C$)	T _A = 25 °C	I _D	9.2 ^b		
	T _A = 100 °C		6.8 ^b	_	
Pulsed Drain Current		I _{DM}	140	— A	
Continuous Courses Drain Diada Current	T _C = 25 °C		45 ^a		
Continuous Source-Drain Diode Current	T _A = 25 °C	I _S	2 ^b		
Single Pulse Avalanche Current	L = 0.1 mH	I _{AS}	35		
Avalanche Energy	L = 0.1 mm	E _{AS}	101	mJ	
	T _C = 25 °C		136.4		
Mauianum Davier Diasia atian	T _C = 100 °C		68.2		
Maximum Power Dissipation	T _A = 25 °C	P _D	3 ^b	W	
	T _A = 100 °C		1.5 ^b		
Operating Junction and Storage Temperature Range		T _J , T _{stq}	- 55 to 175	°C	

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^b	Steady State	R _{thJA}	40	50	°C/W
Maximum Junction-to-Case	Sleady State	R _{thJC}	0.85	1.1	0/11

Notes:

a. Package limited.

b. Surface mounted on 1" x 1" FR4 board.

SPECIFICATIONS ($T_J = 25^{\circ}$	C, unless o	otherwise noted)					
Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static							
Drain-Source Breakdown Voltage	V _{DS}	$V_{GS} = 0 \text{ V}, \text{ I}_{D} = 250 \mu\text{A}$	100			V	
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	1 - 2504		110		mV/°C	
V _{GS(th)} Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	I _D = 250 μA		- 12.5			
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_D = 250 \ \mu A$	2.5		5	V	
Gate-Source Leakage	I _{GSS}	$V_{DS} = 0 V, V_{GS} = \pm 20 V$			± 100	nA	
Zara Cata Valtaga Drain Current	1	$V_{DS} = 100 \text{ V}, V_{GS} = 0 \text{ V}$	1		1		
Zero Gate Voltage Drain Current	IDSS	V_{DS} = 100 V, V_{GS} = 0 V, T_{J} = 125 °C			50	- μΑ	
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$	30			А	
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 10 V, I _D = 15 A		0.0185		Ω	
Forward Transconductance ^a	9 _{fs}	V _{DS} = 15 V, I _D = 15 A		33		S	
Dynamic ^b							
Input Capacitance	C _{iss}			2400		pF	
Output Capacitance	C _{oss}	$V_{DS} = 50 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		230			
Reverse Transfer Capacitance	C _{rss}			80			
Total Gate Charge	Qg			38	70	nC	
Gate-Source Charge	Q _{gs}	$V_{DS} = 50 \text{ V}, \text{ V}_{GS} = 10 \text{ V}, \text{ I}_{D} = 50 \text{ A}$		14			
Gate-Drain Charge	Q _{gd}			12			
Gate Resistance	R _g	f = 1 MHz		1.6	2.5	Ω	
Turn-On Delay Time	t _{d(on)}			12	20	- ns	
Rise Time	t _r	V_{DD} = 50 V, R_{L} = 1 Ω		10	20		
Turn-Off Delay Time	t _{d(off)}	$I_D \cong 50$ Å, $V_{GEN} = 10$ V, $R_g = 1$ Ω		18	35		
Fall Time	t _f			8	15		
Drain-Source Body Diode Characteri	stics						
Continuous Source-Drain Diode	ا _S	T _C = 25 °C			35	A	
Pulse Diode Forward Current ^a	I _{SM}				100		
Body Diode Voltage	V _{SD}	I _S = 15 A		0.85	1.5	V	
Body Diode Reverse Recovery Time	t _{rr}			80	120	ns	
Body Diode Reverse Recovery Charge	Q _{rr}			160	240	nC	
Reverse Recovery Fall Time	ta	l _F = 50 A, dl/dt = 100 A/μs, T _J = 25 °C		57			
Reverse Recovery Rise Time	t _b	-1 1		23		ns	

Notes:

a. Pulse test; pulse width \leq 300 µs, duty cycle \leq 2 %.

b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

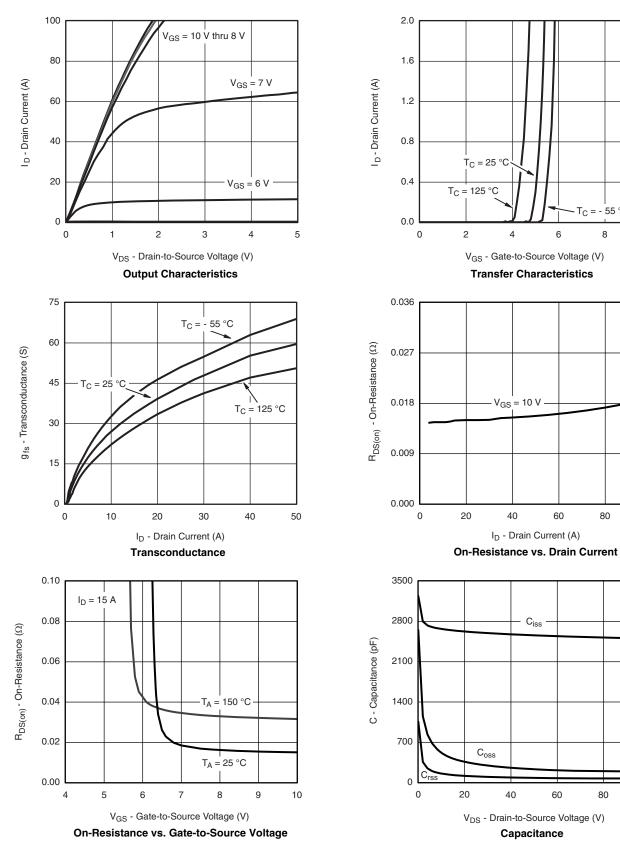
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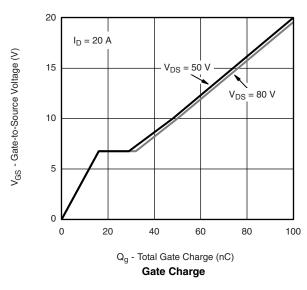


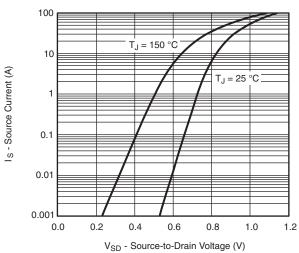
T_C = - 55 °C

TYPICAL CHARACTERISTICS (25 °C, unless otherwise note)

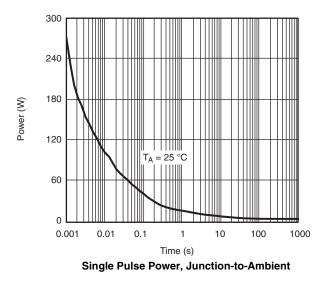


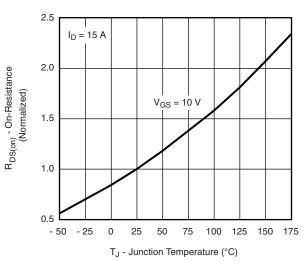




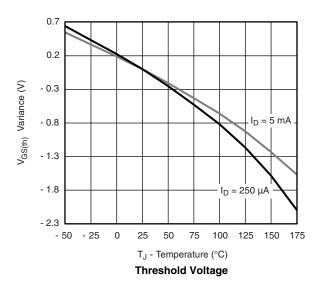


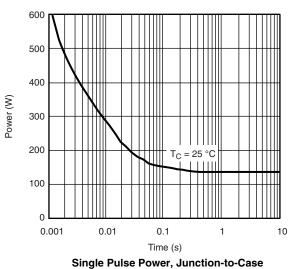




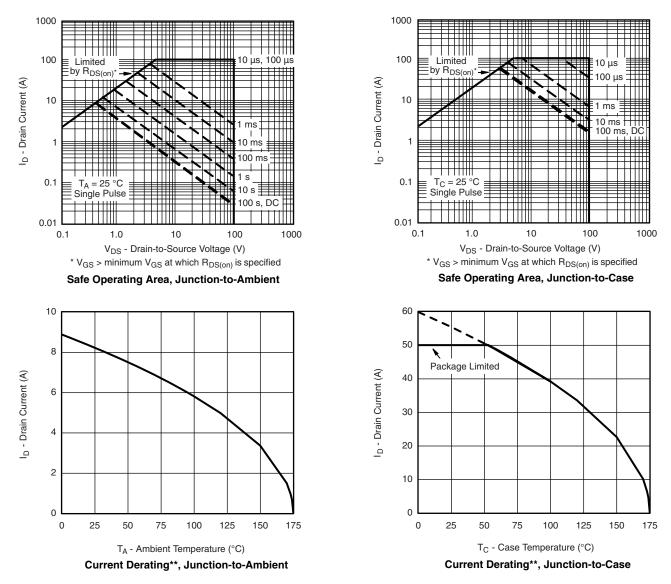


On-Resistance vs. Junction Temperature



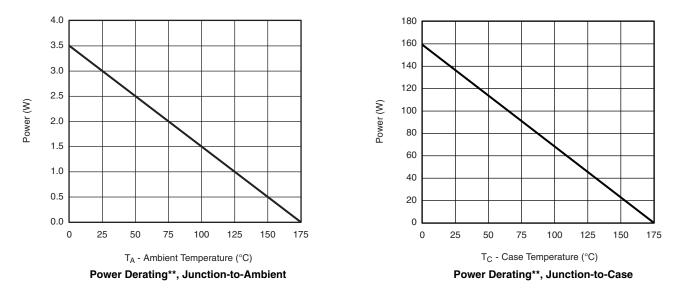






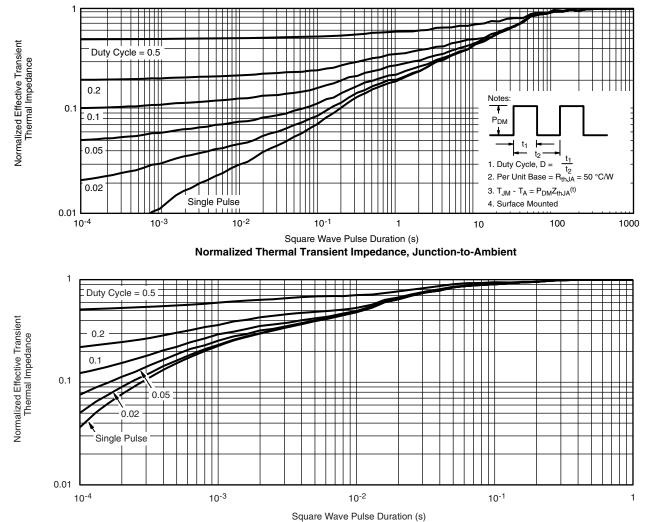
** The power dissipation P_D is based on $T_{J(max.)} = 175$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.





** The power dissipation P_D is based on $T_{J(max)} = 175$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.





Normalized Thermal Transient Impedance, Junction-to-Case



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