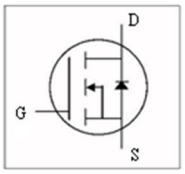
KGEY 金易半 Kingeavysemi

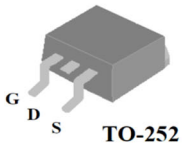
KE6801Y0U

N-CHANNEL ENHANCEMENT MODE POWER MOSFET

- Simple Driver Requirement
- Low On-resistance
- RoHS Compliant & Halogen-Free



BVDSS	100V
RDS(ON)Typ	5.3mΩ
ID	75A



TO-252

Description

KE6801 is from Kingeavy innovated design and silicon process technology to achieve the lowest possible on- resistance and fast switching performance. It provides the designer with an extreme efficient device for use in a wide range of power applications.

Absolute Maximum Ratings@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	100	V
V_{GS}	Gate-Source Voltage	±20	V
I_D@T_C=25℃	Drain Current, V_{GS} @ 10V	75	A
I_D@Tc=100℃	Drain Current, V_{GS} @ 10V	35	A
I_{DM}	Pulsed Drain Current[1]	150	A
P_D@T_A=25℃	Total Power Dissipation	2.1	W
P_D@Tc=25℃	Total Power Dissipation	35	W
P_D@Tc=100℃	Total Power Dissipation	14	W
E_{AS}	Avalanche Energy, Single pulse[4]	65	mJ
T_{STG}	Storage Temperature Range	-55 to 150	℃
T_J	Operating Junction Temperature Range	150	℃

Thermal Data

Symbol	Parameter	Value	Unit
Rthj-c	Maximum Thermal Resistance, Junction-case	3.5	℃/W
Rthj-a	Maximum Thermal Resistance, Junction-ambient[3]	60	℃/W

Electrical Characteristics@T_j=25 oC(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250uA	100	-	-	V
RDS(ON)	Static Drain-Source On-Resistance2	V_{GS}=10V, I_D=20A	-	5.3	5.8	mΩ
		V_{GS}=4.5V, I_D=20A	-	7.3	10	mΩ
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250uA	1	2	3	V
g_{fs}	Forward Transconductance	V_{DS}=5V, I_D=20A	-	58	-	S
I_{DSS}	Drain-Source Leakage Current	V_{DS}=80V, V_{GS}=0V	-	-	1	uA
I_{GSS}	Gate-Source Leakage	V_{GS}=±20V, V_{DS}=0V	-	-	±100	nA
Q_g	Total Gate Charge	I_D=20A V_{DS}=50V V_{GS}=10V	-	64	-	nC
Q_{gs}	Gate-Source Charge		-	11	-	nC
Q_{gd}	Gate-Drain ("Miller") Charge		-	16	-	nC
$t_{d(on)}$	Turn-on Delay Time	V_{DS}=50V I_D=1A R_G=6Ω V_{GS}=10V	-	16	-	ns
t_r	Rise Time		-	32	-	ns
$t_{d(off)}$	Turn-off Delay Time		-	52	-	ns
t_f	Fall Time		-	85	-	ns
C_{iss}	Input Capacitance	V_{GS}=0V V_{DS}=50V f=1.0MHz	-	3643	-	pF
C_{oss}	Output Capacitance		-	1061	-	pF
Crss	Reverse Transfer Capacitance		-	40	-	pF
Rg	Gate Resistance	f=1.0MHz	-	0.54	-	Ω

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{SD}	Forward On Voltage2	I_S=10A, V_{GS}=0V	-	0.8	1.1	V
t_{rr}	Reverse Recovery Time	I_S=10A, V_R=50V dI/dt=100A/μs	-	37.2	-	ns
Q_{rr}	Reverse Recovery Charge		-	35	-	nC

Notes:

1.Pulse width limited by Max. junction temperature.

2.Pulse Test

3.Surface mounted on 1 in^2 2oz copper pad of FR4 board, t <10sec ; 60℃W when mounted on min. copper pad.

4.Starting Tj=25℃ Vdd=50V,L=0.1mH,Rg=25Ω.

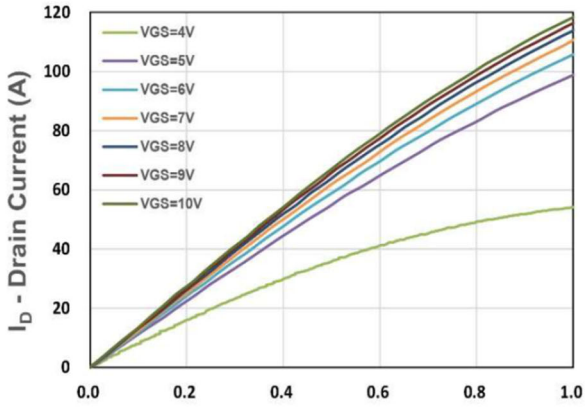


Figure 1. Output Characteristics

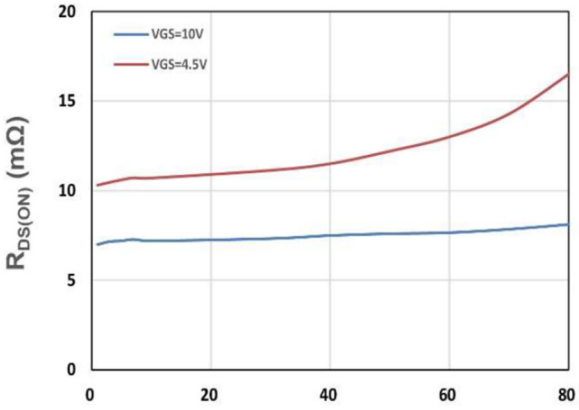


Figure 2. On-Resistance vs. ID

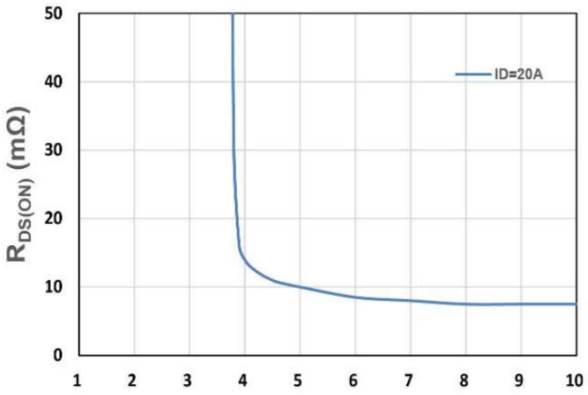


Figure 3. On-Resistance vs. VGS

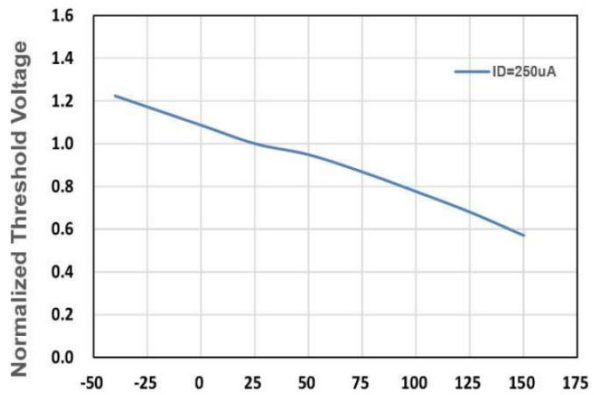


Figure 4. Gate Threshold Voltage

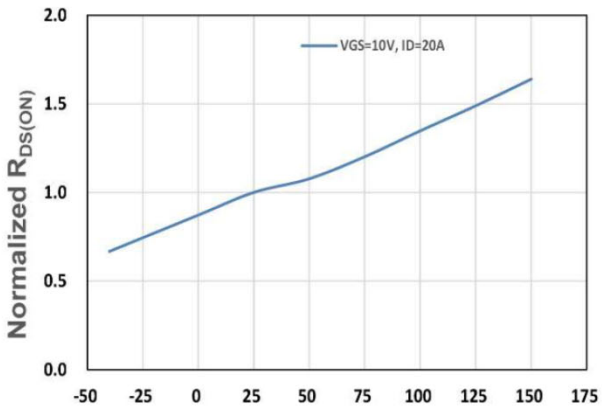


Figure 5. Drain-Source On Resistance

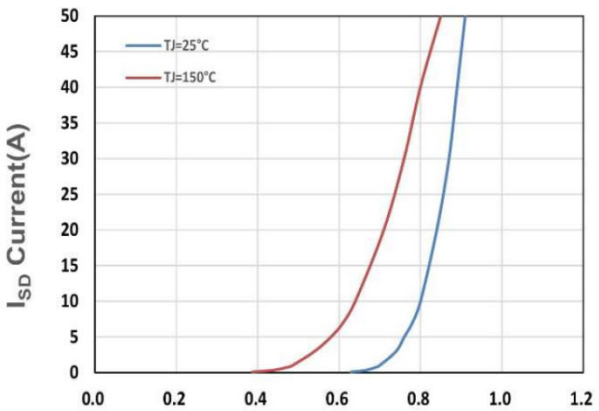
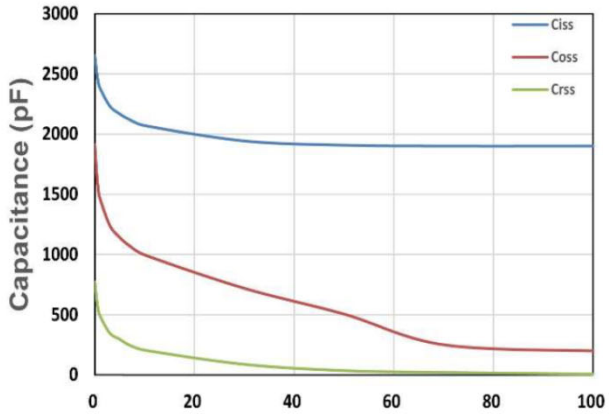
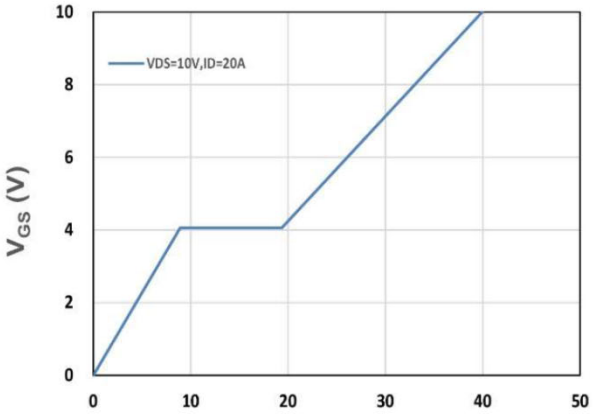


Figure 6. Source-Drain Diode Forward



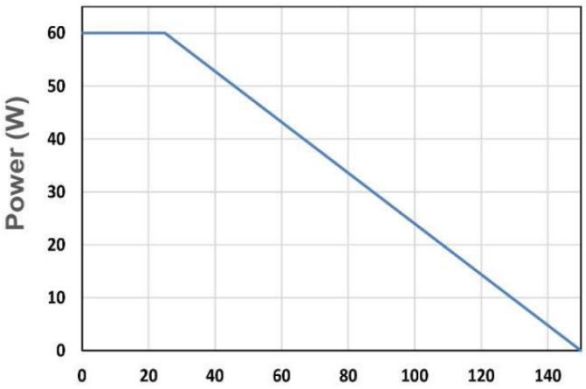
V_{DS} - Drain - Source Voltage (V)

Figure 7. Capacitance



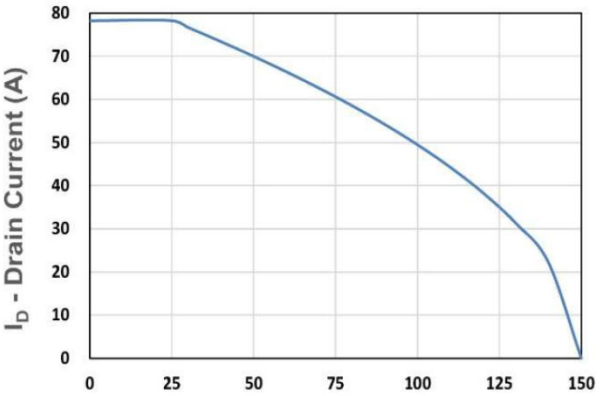
Qg, Total Gate Charge (nC)

Figure 8. Gate Charge Characteristics



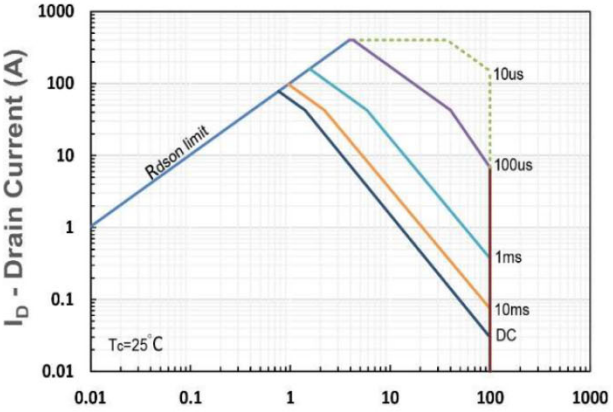
Tc - Junction Temperature (°C)

Figure 9. Power Dissipation



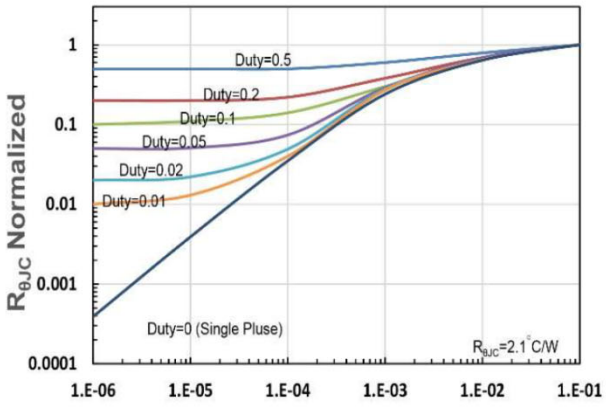
T_C - Junction Temperature (°C)

Figure 10. Drain Current



V_{DS} - Drain-Source Voltage (V)

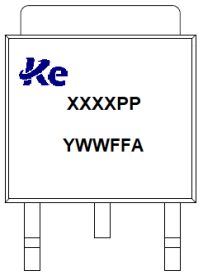
Figure 11. Safe Operating Area



t_1,Square Wave Pulse Duration(s)

Figure 12. RθJC Transient Thermal Impedance

Marking Information



Package	TO-252	
XXXX	Part Number	
PP	Package Code	
Y	Year	F=2020 , G=2021, ……
WW	Weeks	Ex. 10/27=44weeks, 11/3=45weeks
FF	Wafer lot	Lot No.
A	Serial	Serial No.
Dot	First pin	

Package Outline : TO-252 : (mm)