GENERAL DESCRIPTION

OB2005xK-G is a high performance and tightly integrated secondary side synchronous rectifier for switch mode power supply system. It combines a much lower voltage drop N-channel MOSFET to emulate the traditional diode rectifier at the secondary side of Flyback converter, which can reduce heat dissipation, increases output current capability and efficiency and simplify thermal design. OB2005xK-G can support low system output voltage down to 2V at constant current mode. With its versatility and optimization, OB2005xK-G can be used in various switch mode power supply topologies including secondary-side control topology and primary-side control topology. The drain-to-source voltage of SR MOSFET is sensed to control the turn on and off of the SR MOSFET. To reduce SR falling time and turn off the integrated N-channel SR switch in proximity of the zero current transition, soft gate is implemented in OB2005xK-G, which would pull down the gate voltage level before being turned off completely.

OB2005xK-G is offered in SOP8 package.

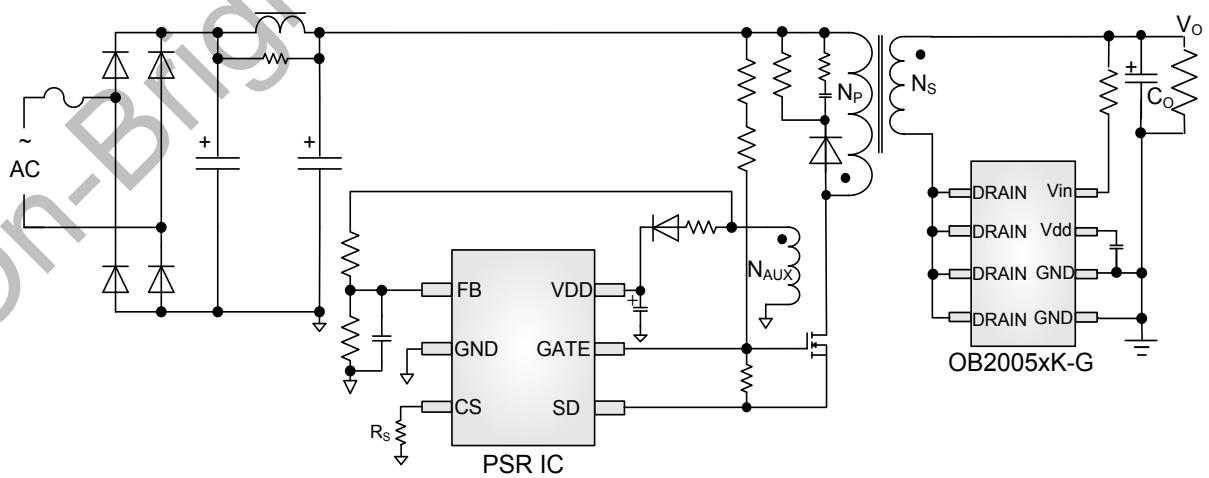
FEATURES

- Secondary-side synchronous rectifier optimized for 5V output sysem
- Suitable for DCM, QR operation
- Soft gate drive for fast and zero current turn-off
- Accurate secondary side MOSFET Vds sensing
- Vds slope detection effectively avoid the ring impact induced by parasitic elements
- Up to 200kHz operation frequency
- VDD UVLO protection

APPLICATIONS

- AC/DC 5V adaptors
- Cell phone charger
- 5V Bias supply
- Low voltage rectification circuits

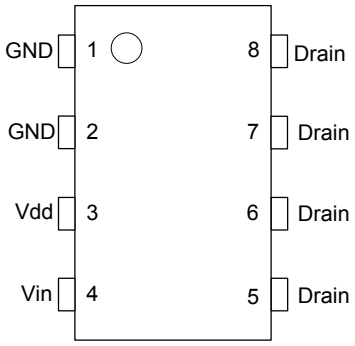
TYPICAL APPLICATION



GENERAL INFORMATION

Pin Configuration

The OB2005xK-G is offered in SOP8 package, shown as below.



Ordering Information

Part Number	Description
OB2005VKCP-G	SOP8, Halogen-free in Tube
OB2005VKCPA-G	SOP8, Halogen-free in T&R

Package Dissipation Rating

Package	RθJA(℃/W)	RθJC(℃/W)
SOP8	90	25

Absolute Maximum Ratings

Parameter	Value
Vin pin	-0.6V to 7V
Vdd pin	-0.6V to 7V
Drain pin	-2.5V to BVdss Note3
Min/Max Operating Junction Temperature TJ	-40 to 150 ℃
Operating Ambient Temperature T_A	-20 to 85 ℃
Min/Max Storage Temperature Tstg	-55 to 150 ℃
Lead Temperature (Soldering, 10secs)	260 ℃

Note1: -0.6V is self-clamped

Note2: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.

Note3: -2.5V applies to minimum duty cycle during normal operation only.

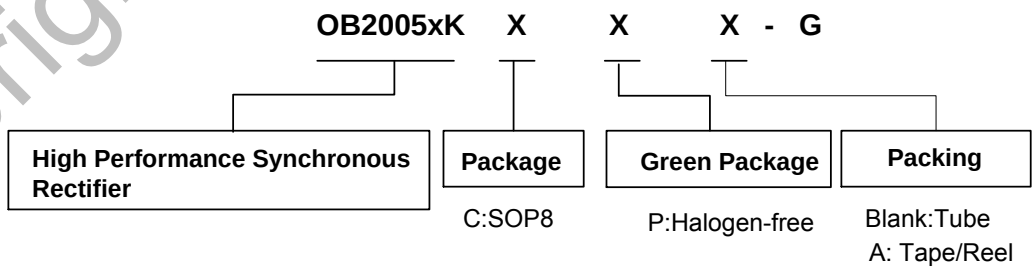
Recommended Operating Range

Symbol	Parameter	Min/Max
VDD	VDD Supply Voltage	4V to 5.5V

Output Power Table

Part Number	Maximum Output Current
OB2005VK-G	2A Note1

Note1: Maximum practical continuous power in a charger designed with sufficient drain pattern as a heat sink, at 40℃ ambient.



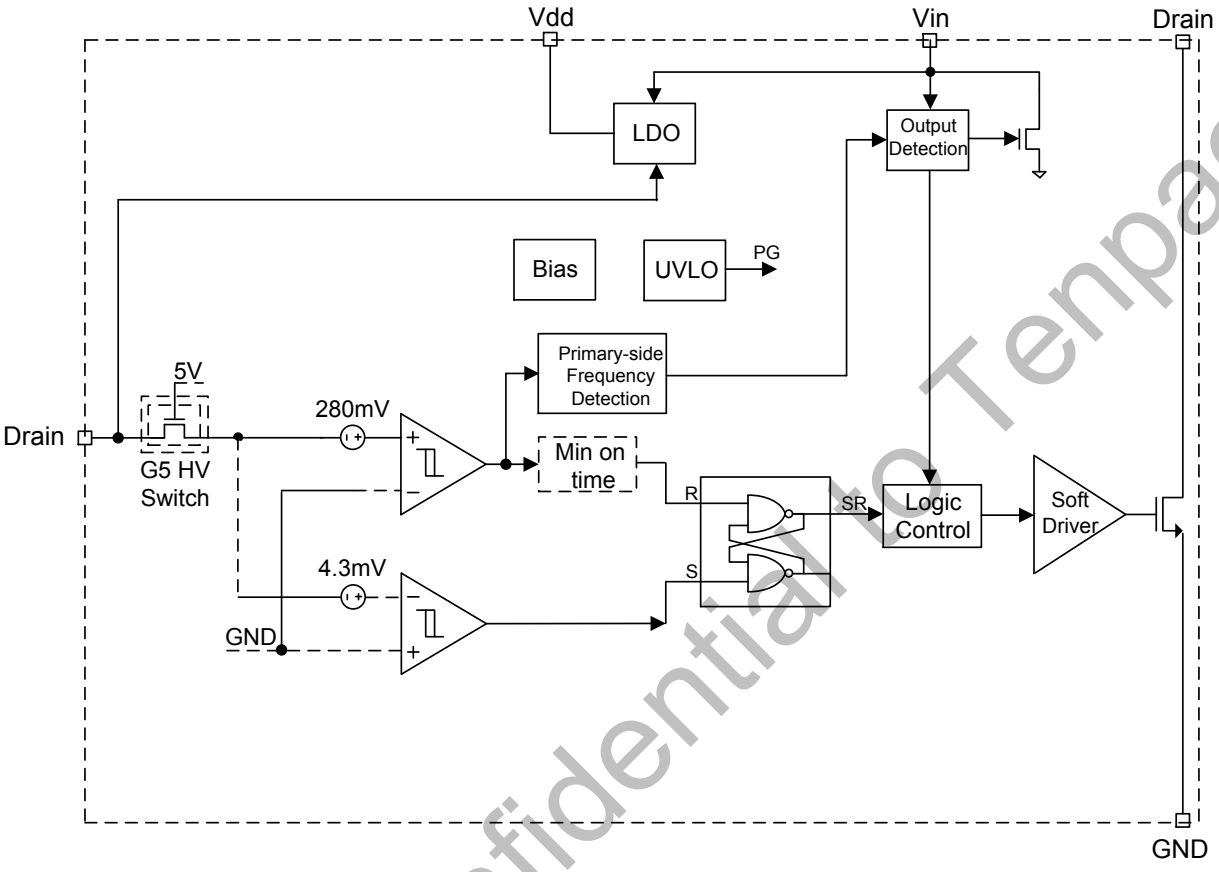
Marking Information

Y:Year Code
WW:Week Code(01-52)
ZZZ:Lot Code
C:SOP8 Package
P:Halogen-free Package
K:Character Code
S:Internal Code(Optional)

TERMINAL ASSIGNMENTS

Pin Name	I/O	Description
GND	P	Ground
Drain	I/O	SR Mosfet drain pin. This pin is connected to secondary-side winding of transformer
VDD	P	Power Supply
Vin	I	System output voltage detection, 10ohm resistor connected to Vin pin is recommended

BLOCK DIAGRAM



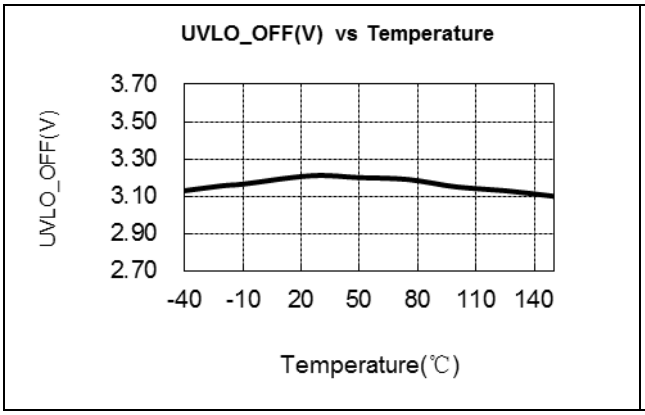
ELECTRICAL CHARACTERISTICS

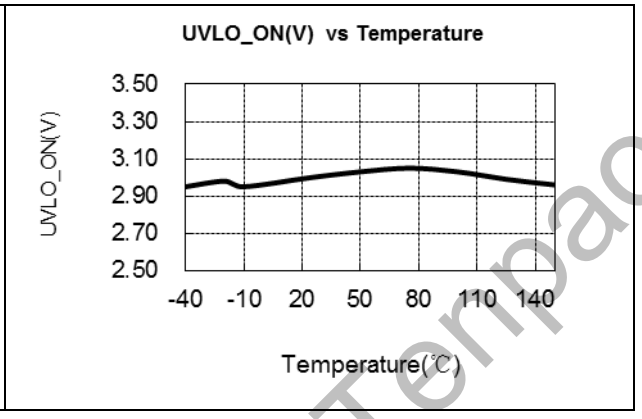
(T_A = 25℃, Vin=5V, unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
Supply Voltage (Vin)						
I_Vin_operation	Operation current	Frequency@Drain=65KHz,Vdd=5V		1.2	1.5	mA
		Frequency@Drain=2KHz,Vdd=5V		0.16	0.3	mA
Vdd_regulation_mini	Minimum Vdd regulation voltage			4.0		V
Vdd_regulation	Vdd regulation voltage			4.3		V
UVLO(ON)	Vdd Under Voltage Lockout Entry		2.8	3.0	3.2	V
UVLO(OFF)	Vdd Under Voltage Lockout Exit (Recovery)		3.0	3.2	3.4	V
Drain Section						
Vth_SR_act	SR MOSFET turn on threshold voltage detection at Drain			-280		mV
Vth_SR_deact	SR MOSFET turn off threshold voltage detection at Drain			-4.3		mV
Vds_regulation	Vds regulation voltage			-38		mV
Tvds_slope_det_widown	Vds slope detection time window			160		nS
T_minimum_on	SR MOSFET minimum on time			2.1		us
Tdelay_on	SR MOSFET turn-on propagation delay	SR MOSFET turn-on fast path		50		ns
		SR MOSFET turn-on slow path		210		ns
Tdelay_off	SR MOSFET turn-off propagation delay				30	ns
Vin_sr_disable	Vin voltage @ SR disable			1.8		V

SR Mosfet Section						
Parameter / **Product**	**BVdss(V)** MOSFET Drain-Source Breakdown Voltage			**Rds,on(mΩ)** On resistance		
	Min	Typ.	Max	Min	Typ.	Max
OB2005VK-G	40				22	

CHARACTERIZATION PLOTS





Operation Description

OB2005xK-G is a high performance and versatile synchronous rectifier. It drives a much lower voltage drop N-channel MOSFET to emulate the traditional diode rectifier, which can reduce heat dissipation, increase output current capability and efficiency, and simplify the thermal design.

Startup and under voltage lockout (UVLO)

OB2005xK-G implements UVLO function during startup. When Vdd rises above UVLO(off), refer to Fig.1 the IC wakes up from under voltage lock out state and enter normal operation. When Vdd drops below UVLO(on), refer to Fig.2 the IC enter under voltage lock out state again and the SR gate is pulled low by 51K resistor on chip. In addition, there is a hysteresis window between UVLO(off) and UVLO(on) to make system work reliably.

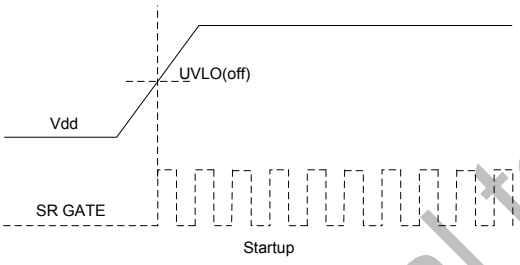


Fig.1 System start up timing diagram

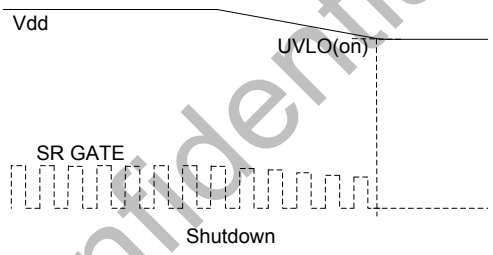


Fig.2 System shut down timing diagram

Synchronization rectifier

OB2005xK-G controls the turn-on and turn-off of synchronization rectifier MOSFET (SR MOSFET) by detection of drain-source voltage of SR MOSFET. When demagnetization of transformer starts, the secondary-side current will flow through the body diode of SR MOSFET and the voltage at the drain will drop to below -700mV (typical). As soon as OB2005xK-G detects this negative voltage, the driver voltage is pulled high to turn on the SR MOSFET .

After the SR MOSFET is turned on, the drain voltage of SR MOSFET begins to rise based on its Rdson and secondary-side current. The drain voltage becomes higher with demagnetization goes on. When the drain voltage rises above SR turn off threshold -4.3mv (typical), the gate of SR MOSFET will be pulled down to ground very quickly after short turn-off delay, refer to Fig.3.

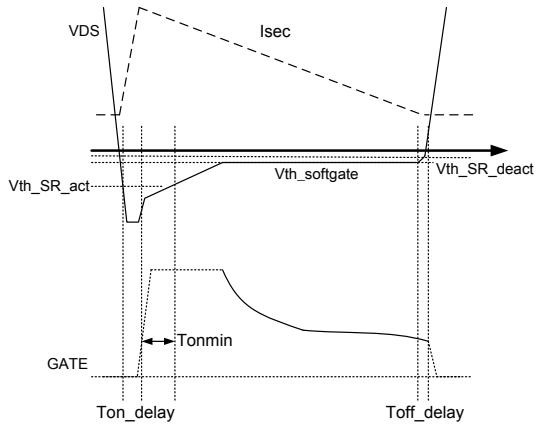


Fig.3 Synchronous Rectification Operation

Soft Gate Control

Once the SR MOSFET is turned on, the gate drive voltage would vary depending on Vds voltage. With the decrease of the secondary-side current, the VDS will rise above Vds_regulation -38mV (typical), and the soft gate control would be enabled. Then the gate voltage is pulled lower to enlarge the Rds(on) of the synchronous MOSFET, therefore VDS is adjusted to remain at -38mV during the rest of demagnetization time. The soft gate scheme can guarantee zero current turn-off and save the pull-down time resulting in higher turn-off speed.

Minimum on time

To avoid effectively false turn-off due to high frequency interference caused by parasitic element at the start of secondary-side demagnetization, OB2005xK-G offers a blanking time(minimum turn-on time) of 2.1μs.

PCB Layout Consideration

The following rules should be followed in OB2005xK-G PCB Layout:

The Area of Power Loop: The area of the secondary current loop including the OB2005xK-G and the output capacitor should be as small as possible to reduce EMI radiation. And the PCB trace must be wide and short for thermal consideration, refer to Fig.4.

Bypass Capacitor: The bypass capacitor on Vdd should be placed as close as possible to the Vdd pin. And the negative node of Vdd capacitor should be connected directly to the GND pin

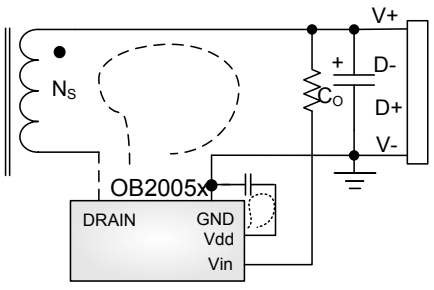
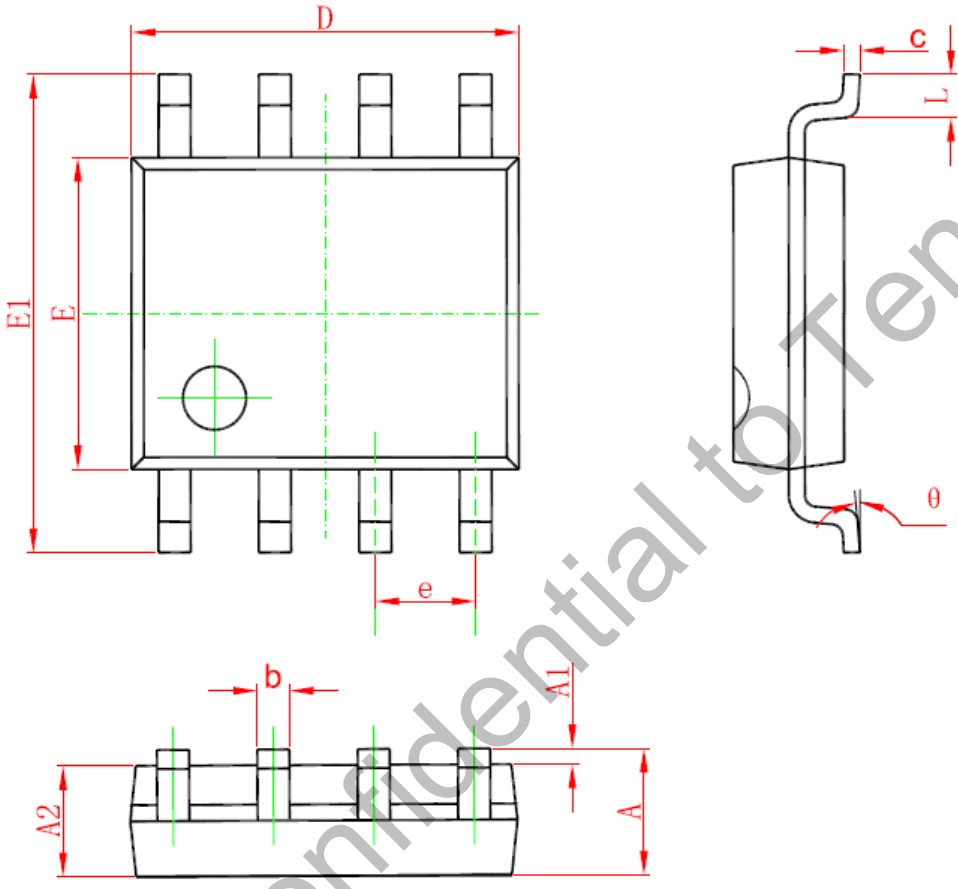


Fig.4 Proper Loop at the Secondary Side of the Flyback with OB2005xK-G

PACKAGE MECHANICAL DATA
SOP8 PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.050	0.250	0.002	0.010
A2	1.250	1.650	0.049	0.065
b	0.310	0.510	0.012	0.020
c	0.100	0.250	0.004	0.010
D	4.700	5.150	0.185	0.203
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

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