SC8812A High Efficiency, Synchronous, Bi-Directional Buck-Boost Charger Controller with I2C Interface

1 Description

SC8812A is a synchronous buck-boost charger controller which can support reverse discharging operation. It can support up to 26V battery voltage, so can be used to effectively manage the charging process for 1~4 cell Li-ion batteries no matter adapter voltage is higher, lower or equal to battery voltage. When a system needs to generate an output from the battery, SC8812A can also discharge the cells and delivers desired output up to 36V.

Through its I2C interface, user can set the charging / discharging mode easily, and program the charging current, charging voltage, reserve output voltage, current limits, switching frequency and other parameters flexibly. Besides that, SC8812A supports fast charging handshake. It also integrates 10-bit ADC, so user can read the VBUS / VBAT voltage and current in real time, simplifying the system design.

SC8812A supports internal current limit, over voltage protection, output short protection and over temperature protections to ensure safety under abnormal conditions.

The SC8812A is in a 32 pin 4x4 QFN package.

2 Features

- Buck-Boost Battery Charger for 1 to 4 Cell Batteries
- Charging Management including Trickle Charge, CC Charge, CV Charge and Charge Termination
- Buck-Boost Reverse Discharging Mode
- Wide V_{BAT} Range: 2.7 V to 26 V, 40V sustainable
- Wide V_{BUS} Range: 2.7 V to 36 V, 40V sustainable
- I2C Programmable Charging Current and Voltage
- I2C Programmable Discharging Output Voltage
- I2C Programmable Input / Output Current Limit
- I2C Programmable Switching Frequency
- High Efficiency Buck-Boost Conversion
- DP/DM Handshake for Fast Charging
- 10-bit ADC Resources
- Charging Status Indication
- Event Detections, including Automatic Adapter Insert and Automatic Load Insert Detection
- Power Path Control
- Under Voltage Protection, Over Voltage Protection, Over Current Protection, Short Circuit Protection and Thermal Shutdown Protection
- QFN-32 Package

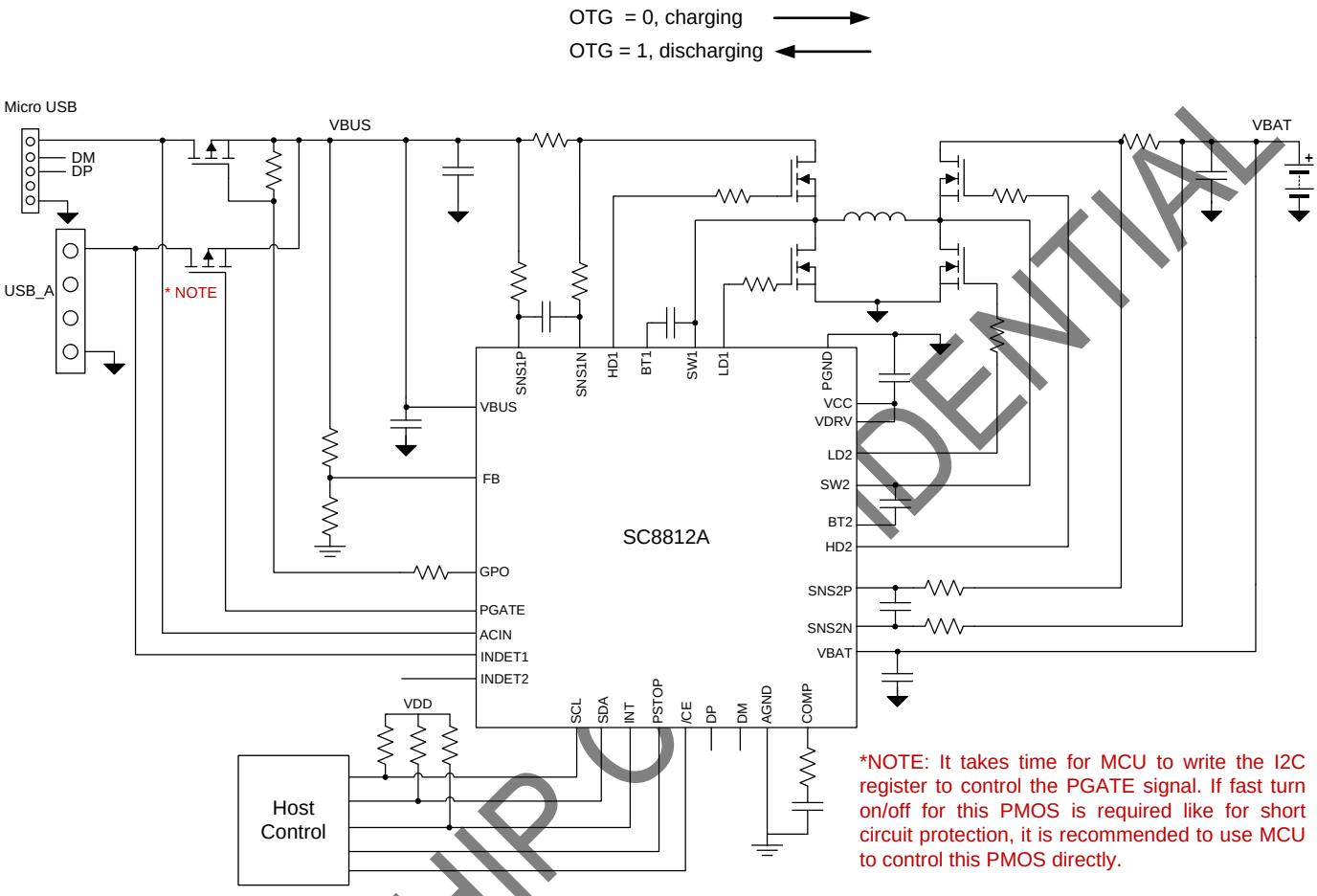
3 Applications

- Power Bank with Fast Charge Function
- USB Power Delivery
- Type C Hub
- Industrial Power Supplies

4 Device Information

Part Number	Package	Dimension
SC8812AQDER	32 pin QFN	4.0mm x 4.0mm x 0.75mm

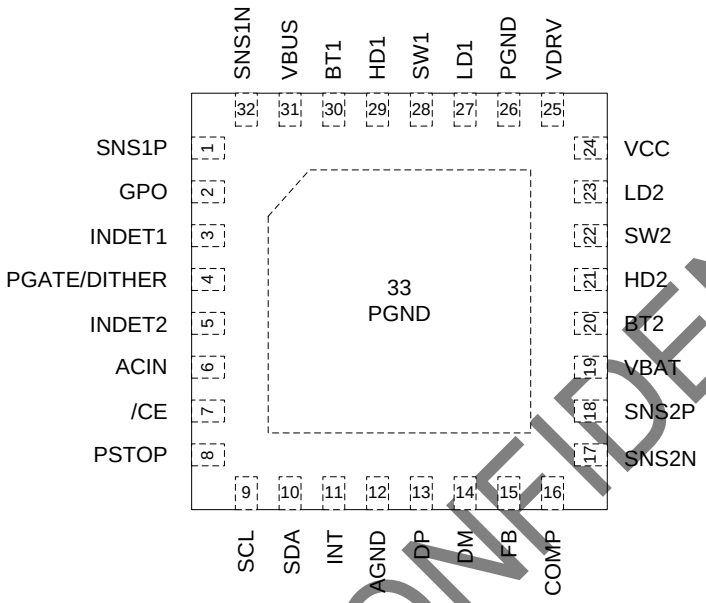
5 Typical Application Circuit



*NOTE: It takes time for MCU to write the I2C register to control the PGATE signal. If fast turn on/off for this PMOS is required like for short circuit protection, it is recommended to use MCU to control this PMOS directly.

6 Terminal Configuration and Functions

Top View



TERMINAL		I/O	DESCRIPTION
NUMBER	NAME		
1	SNS1P	I	Positive input of a current sense amplifier. Connect to one pad of the current sense resistor (typical 10 mΩ) on the power path to sense the current into or out from VBUS.
2	GPO	O	Open drain output for general purpose. It is controlled by GPO_CTRL bit. User can use this pin to drive external PMOS with a pull up resistor.
3	INDET1	I	Connect this pin to a USB-A port to detect the load insertion event. When an insertion event is detected, the IC sets INDET1 bit and outputs an INT interrupt pulse to inform MCU.
4	PGATE/DITHER	IO	PMOS gate driver controlled by PGATE bit, used to control the external PMOS on the power path. This pin can be configured through I2C for switching frequency dithering function. Connect a ceramic capacitor (typical 100nF) from this pin to ground when for frequency dither function.
5	INDET2	I	Connect this pin to a USB-A port to detect the load insertion event. When an insertion event is detected, the IC sets INDET2 bit and outputs an INT interrupt pulse to inform MCU.
6	ACIN	I	Connect this pin to AC adapter input node or micro-USB port to detect an AC adapter insertion event. When an insertion event is detected, the IC sets AC_OK bit and outputs an INT interrupt pulse to inform MCU.
7	/CE	I	Chip enable control. Pull this pin to logic low to enable the IC; pull this pin to logic high to disable the IC. This pin is internally pulled low.
8	PSTOP	I	Power stop control. Pull this pin to logic low to enable the power blocks; pull this pin to logic high to disabled the power blocks, and the IC enters into Standby mode. In Standby mode, only the AC adapter and load insert detection functions and the I2C circuits keep working.

			This pin is internally pulled low.
9	SCL	I	I2C interface clock. Connect SCL to the logic rail through a pull up resistor (typical 10 kΩ). The IC works as a slave, and the I2C address is 0x74H.
10	SDA	I/O	I2C interface data. Connect SDA to the logic rail through a pull up resistor (typical 10 kΩ).
11	INT	O	An open drain output for interrupt signal. The IC sends a logic low pulse at INT pin to inform the host if an interrupt event happens.
12	AGND	I/O	Analog ground. Connect PGND and AGND together at the thermal pad under IC.
13	DP	IO	Positive data line for USB interface. Can be controlled by MCU to implement the handshaking with adapter to realize fast charging.
14	DM	IO	Negative data line for USB interface. Can be controlled by MCU to implement the handshaking with adapter to realize fast charging.
15	FB	I	Feedback node for VBUS voltage. Connect a resistor divider from VBUS to FB to set the VBUS discharging output voltage in external way. The FB reference can also be programmed through I2C.
16	COMP	I	Connect resistor and capacitor at this pin to compensate the control loop.
17	SNS2N	I	Negative input of a current sense amplifier. Connect to one pad of the current sense resistor (typical 10 mΩ) on the power path to sense the current into or out from battery.
18	SNS2P	I	Positive input of a current sense amplifier. Connect to the other pad of the current sense resistor (typical 10 mΩ) on the power path to sense the current into or out from battery.
19	VBAT	I	Power supply to the IC. Connect to the battery positive node. Place a 1 μF capacitor from this pin to PGND as close to the IC as possible.
20	BT2	I	Connect a 100nF capacitor between BT2 pin and SW2 pin to bootstrap a bias voltage for high side MOSFET driver.
21	HD2	O	Gate driver output to control the external high side power MOSFET.
22	SW2	I/O	Switching node. Connect to the inductor.
23	LD2	O	Gate driver output to control the external low side power MOSFET.
24	VCC	O	Output of an internal 6V linear regulator. Connect a 1 μF capacitor from VCC pin to PGND as close to the IC as possible.
25	VDRV	I	Power supply input for internal driver circuits. Connect VCC to this pin directly
26	PGND	I/O	Power ground. Connect PGND and AGND together at the PGND thermal pad under IC.
27	LD1	O	Gate driver output to the external low side MOSFET.
28	SW1	I/O	Switching Node. Connect to the inductor.
29	HD1	O	Gate driver output to the external high side MOSFET.
30	BT1	I	Connect a 100nF capacitor between BT1 pin and SW1 pins to bootstrap a bias voltage for high side MOSFET driver.
31	VBUS	I	Power supply to the IC. Connect to the VBUS rail. Place a 1 μF capacitor from this pin to PGND as close to the IC as possible.

32	SNS1N	I	Negative input of a current sense amplifier. Connect to one pad of the current sense resistor (typical 10 mΩ) on the power path to sense the current into or out from VBUS.
33	Thermal Pad		PGND thermal pad. Connect PGND and AGND together at the thermal pad under IC.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	Unit
Voltage range at terminals(2)	LD2, VCC, VDRV, LD1, DP, DM HD1 to SW1, BT1 to SW1, BT2 to SW2, HD2 to SW2	-0.3	6.5	V
	PSTOP	-0.3	6	V
	SCL, SDA, INT, COMP	-0.3	5	V
	FB	-0.3	30	V
	VBUS, SNS1N, SNS1P, GPO, PGATE, INDET1, INDET2, ACIN, SNS2N, SNS2P, VBAT, SW2, SW1, /CE	-0.3	40	V
	VBUS to SNS1P, SNS1N	-0.3	11	V
	VBAT to SNS2P, SNS2N	-0.3	11	V
	SNS1P to SNS1N	-10	10	V
	SNS2P to SNS2N	-10	10	V
	BT1, HD1, BT2, HD2	-0.3	45	V
	BT1 to HD1, BT2 to HD2	-0.3	6.5	V
T_J	Operating junction temperature range	-40	150	°C
T_{stg}	Storage temperature range	-65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

7.2 Thermal Information

THERMAL RESISTANCE(1)		QFN-32 (4mmX4mm)	UNIT
θ_{JA}	Junction to ambient thermal resistance	35	°C/W
θ_{JC}	Junction to case resistance	7	°C/W

(1) Measured on JESD51-7, 4-layer PCB.

7.3 Handling Ratings

PARAMETER	DEFINITION		MIN	MAX	UNIT
ESD(1)	Human body model (HBM) ESD stress voltage(2)	All pins except DP and DM	-2	2	kV
		DP, DM	-8	8	kV
	Charged device model (CDM) ESD stress voltage(3)		-750	750	V

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges into the device.

(2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.4 Recommended Operating Conditions

		MIN	MAX	UNIT

V_{BUS}	VBUS voltage range	2.7	36	V
V_{BAT}	VBAT voltage range	2.7	26	V
C_{BUS}, C_{BAT}	VBUS Capacitance, VBAT capacitance	30		µF
L	Inductance	2.2	10	µH
$R_{SNS1/2}$	Current Sensing Resistor	5	10	mΩ
T_A	Operating ambient temperature	-40	85	°C
T_J	Operating junction temperature	-40	125	°C

7.5 Electrical Characteristics

T_J= 25°C and V_{BUS} = 5V, V_{BAT} = 10.8V unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE						
V_{UVLO_VBUS}	VBUS under-voltage lockout threshold	Rising edge		2.5	2.7	V
		Hysteresis		170		mV
V_{UVLO_VBAT}	VBAT under-voltage lockout threshold	Rising edge		2.4	2.6	V
		Hysteresis		170		mV
I_{Q_VBAT}	Quiescent current into VBAT	VBUS = 5V PSTOP = L, non-switching		2.4	4	mA
		VBUS = 5V PSTOP = L, after charging termination		2.4	4	mA
I_{Q_VBUS}	Quiescent current into VBUS	PSTOP = L, non-switching		25	40	μA
I_{SB_VBAT}	Standby current into VBAT	VBUS open PSTOP = H, AD_START = 0		17	40	μA
		VBUS open PSTOP = H, AD_START = 1		0.65	1.2	mA
I_{SB_VBUS}	Standby current into VBUS	PSTOP = H, AD_START = 0		12	50	μA
I_{SD_VBAT}	Shutdown current into VBAT	/CE = H, VBUS = open		10	20	μA
VCC, DIRVER AND POWER SWITCH						
V_{CC}	VCC regulation voltage	PSTOP = L, VBUS = 9V	5.75	6	6.25	V
		PSTOP = L, VBUS = 5V	4.95	4.98	5	V
		PSTOP = H			3	V
I_{VCC_LIM}	VCC current limit	PSTOP = L VBUS = 5V, VCC = 4V	20	27	34	mA
		PSTOP = H			1	mA
R_{HS/LS_PU}	High/low side MOS driver pull up resistor			4		Ω
R_{HS/LS_PD}	High/low side MOS driver pull down resistor			1		Ω
REFERENCE VOLTAGE IN CHARGING MODE						
V_{BATS_int}	VBATS accuracy for internal setting, over VBATS target	VCELL_SET=000~111	-0.5		0.5	%
$V_{TRICKLE\_int}$	Trickle charge threshold voltage for internal setting	Cell number = N VCELL_SET = 000~1111, TRICKLE_SET = 0	2.73*N	2.94*N	3.15*N	V
		Cell number = N VCELL_SET = 000~1111, TRICKLE_SET = 1	2.31*N	2.52*N	2.73*N	V
V_{EOC}	EOC voltage threshold, over VBAT target		97%	98%	99%	
V_{RECH}	Recharge threshold voltage, over VBAT target		94.8%	95.8%	96.8%	
V_{INREG}	VINREG reference voltage	4.5V target VINREG_SET = 0x2C, VINREG_RATIO = 0	4.3	4.5	4.7	V
		15V target	14.7	15	15.3	V

		VINREG_SET = 0x95, VINREG_RATIO = 0				
		4.48V target VINREG_SET = 0x6F, VINREG_RATIO = 1	4.4	4.5	4.6	V
		10V target VINREG_SET = 0xF9, VINREG_RATIO = 1	9.8	10	10.2	V
V_{BAT_OVP}	VBAT OVP threshold, over VBAT target	VBAT_SEL = 0/1	103%	105.5%	108%	
V_{CLAMP}				125		mV
REFERENCE VOLTAGE IN DISCHARGING MODE						
V_{FB}	FB reference voltage for external setting	FB_SEL = 1, VBUSREF_E_REF target from 0.5V to 2.048V	-2%		2%	
V_{BUS}	VBUS reference voltage accuracy for internal setting	FB_SEL = 0 VBUS_RATIO = 1 (5x) VBUS = 3.6 ~10.24V	-2%		2%	
		FB_SEL = 0 VBUS_RATIO = 0 (12.5x) VBUS = 9 ~ 24V	-2%		2%	
V_{BUS_OVP}	VBUS OVP threshold, rising edge	VBUSREF_I_SET = 1V VBUSREF_E_SET = 1V	107.3%	110%	113%	
	Hysteresis	VBUSREF_I_SET = 1V VBUSREF_E_SET = 1V		3%		
CURRENT LIMIT						
I_{BUS_LIM}	IBUS current limit accuracy	Charging mode, 6A target IBUS_RATIO = 01 (6x) IBUS_LIM = 0x7F	-10%		10%	
		Charging mode, 3A target IBUS_RATIO = 10 (3x) IBUS_LIM = 0x7F	-10%		10%	
		Discharging mode, 6A target IBUS_RATIO = 01 (6x) IBUS_LIM = 0x7F	-10%		10%	
		Discharging mode, 3A target IBUS_RATIO = 10 (3x) IBUS_LIM = 0x7F	-10%		10%	
I_{BAT_LIM}	IBAT current limit accuracy	Charging mode, 6A target IBAT_RATIO = 0 (6x) IBAT_LIM = 0xFF	-10%		10%	
		Charging mode, 12A target IBAT_RATIO = 1 (12x) IBAT_LIM = 0xFF	-10%		10%	
		Discharging mode, 6A target IBAT_RATIO = 0 (6x) IBAT_LIM = 0xFF	-15%		15%	
		Discharging mode, 12A target IBAT_RATIO = 1 (12x) IBAT_LIM = 0xFF	-15%		15%	
$I_{TRICKLE}$	Trickle charge current, over IBAT_LIM setting			10%		

	Trickle charge current, over IBUS_LIM setting			22%		
I_{EOC}	EOC current threshold, over IBUS_LIM / IBAT_LIM setting	EOC_SET= 0		4%		
		EOC_SET= 1		10%		
ERROR AMPLIFIER						
Gm_{EA}	Error amplifier gm		0.12	0.15	0.18	mS
R_{OUT}	Error amplifier output resistance (1)			20		MΩ
I_{SINK_COMP}	COMP sink current	LOOP_SET = 0/1		25		μA
I_{SRC_COMP}	COMP source current	LOOP_SET = 0		18		μA
		LOOP_SET = 1		32		μA
I_{BIAS_FB}	FB pin input bias current	FB_SEL = 1 FB in regulation			50	nA
SWITCHING						
f_{SW}	Switching frequency	FREQ_SET = 00 (150kHz)	140	155	170	kHz
		FREQ_SET = 01 (300kHz)	270	305	330	kHz
		FREQ_SET = 11 (450kHz)	400	450	500	kHz
POWER PATH MANAGEMENT						
R_{PU_PGATE}	PGATE pin pull up resistor	EN_PGATE = 0		20		kΩ
R_{PD_PGATE}	PGATE pin pull down resistor	EN_PGATE = 1		6		kΩ
V_{CLAMP}	Clamp voltage from VBUS to PGATE pin	EN_PGATE = 1	6.9	7.35	7.7	V
R_{RD_GPO}	GPO pin pull down resistor	GPO_CTRL = 1		6		kΩ
DETECTION						
V_{AC_DET}	AC detection threshold		2.9	3.1	3.4	V
V_{SHORT}	Short circuit detection threshold		0.95	1	1.05	V
I2C AND LOGIC CONTROL						
R_{PD}	PSTOP pin internal pull down resistor		0.75	1	1.25	MΩ
V_{IL}	PSTOP, SCL, SDA input low voltage				0.4	V
V_{IH}	PSTOP, SCL, SDA input high voltage		1.2			V
I_{SINK_INT}	INT pin sink current	V_{INT} = 0.4V	0.3	0.375	0.45	mA
$I_{SINK\_SCL/SDA}$	SCL/SDA pin sink current	$V_{SCL/SDA}$ = 0.4V		100		mA
t_{PULSE}	Interrupt pulse width (logic low)		0.6	1	1.5	ms
SOFTSTART						
$t_{deglitch}$	Deglitch time for charging	PSTOP = L, OTG_SET = 0 VBUS = 5V, from PSTOP low to IC starting charging		220		ms
t_{SS}	Internal soft-start time	VBUS from 0V to 5V in discharging mode VBUS_Ratio = 1 (5x)		12		ms
DP/DM						
R_{SHORT}	Short resistance between DP and DM	SHORT_CTRL = 1	18		22	Ω
V_{SRC}	Source voltage at DP/DM pin	DP/DM_CTRL = 01, VDP/DM_SET = 00	0.5	0.6	0.7	V

		DP/DM_CTRL = 01, VDP/DM_SET = 01	1.1	1.2	1.3	V
		DP/DM_CTRL = 01, VDP/DM_SET = 10	2.65	2.75	2.85	V
		DP/DM_CTRL = 01, VDP/DM_SET = 11	2.65	2.75	2.85	V
$I_{SRC\_DP/DM}$	Source capability at DP/DM pin	DP/DM_CTRL = 01, VDP/DM_SET = 00/11	250			μA
$I_{SINK\_DP/DM}$	Sink current at DP/DM pin	DP/DM_CTRL = 10	80	105	130	μA
$V_{COMP\_DP/DM}$	Comparison threshold at DP/DM pin	0.325V threshold	0.25	0.325	0.4	V
		0.84V threshold	0.8	0.84	0.88	V
		2.05V threshold	1.8	2.05	2.3	V
$R_{PD\_DP/DM}$	DP/DM pull down resistor	DP/DM_CTRL = 11	14.25	20.2	24.5	kΩ
THERMAL SHUTDOWN						
T_{SD}	Thermal shutdown temperature (1)			165		°C
	Thermal shutdown hysteresis (1)			15		°C

8 Detailed Description

8.1 Charging Mode

Charging mode and discharging mode is selected by EN_OTG bit.

When EN_OTG bit is 0, the IC works in charging mode. The current flows from VBUS to VBAT to charge the battery cells.

When in charging mode, the IC charges the battery cells according to below typical charging profile. When battery voltage is lower than trickle charge threshold, the IC charges the cells with small charging current; when cell voltage is higher than the threshold, the IC enters into Constant Current charging phase, and charges the cells with constant current set by IBUS limit or IBAT limit. When the cell voltage reaches the termination voltage target, the IC enters into Constant Voltage charge phase, and charges the cells with gradually decreased current until the current is lower than termination current threshold. Once termination voltage and termination current conditions are satisfied, the IC enters into End of Charge phase. In this phase the IC can either terminate the charging or keep charging the cells.

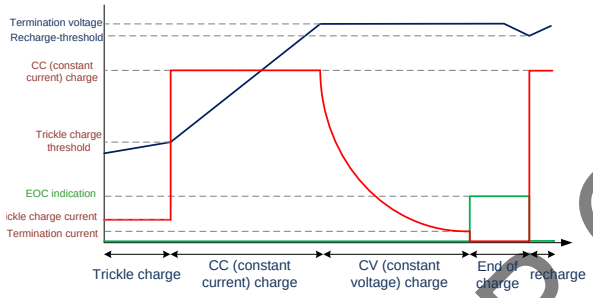


Figure 1 Typical Charging Profile

8.1.1 Trickle Charge

The trickle charge voltage threshold can be set to 60% or 70% of 4.2V/cell by TRICKLE_SET bit. When in trickle charge phase, the charging current is reduced to a small value for the good of battery cells. If ICHAR_SEL bit is 0, the IBUS is reduced to 22% of the IBUS current limit set value; if ICHAR_SEL bit is 1, the IBAT is reduced to 10% of IBAT current limit set value.

If trickle charging phase is not needed, the user can set DIS_TRICKLE bit to 1 to disable it.

8.1.2 CC Charge (Constant Current Charge)

When cell voltage is higher than the trickle threshold, the IC charges the battery cells with constant current set by IBUS limit or IBAT limit, which are set respectively through IBUS_LIM_SET and IBAT_LIM_SET registers. The current limit value can be changed dynamically, and is also related to the current sense resistor and ratio bits. Please see Register Map section for details.

In charging mode, the IC regulates the current which reaches its current limit value first. For example, if IBUS current limit is set to 3A, IBAT limit is set to 10A, and when IBUS reaches 3A, IBAT is only 6A, which is much lower than IBAT limit 10A, then the IC limits the IBUS at 3A.

It is not allowed to set any of the current limits to 0A. Keep the minimum current limit above 0.3A.

8.1.3 CV Charge (Constant Voltage Charge)

The battery target voltage can be set internally, by CSEL bits and VCELL_SET bits. The CSEL bits set the battery cell numbers connected in series, and VCELL_SET bits set the battery voltage per cell. For example, if the battery cells are in xp2s connection (several cells are connected in parallel, and two cells in series) and the cell voltage is 4.3V, the user should set CSEL to 01 (2S), and set VCELL_SET bits to 011 (4.3V).

When the battery cell voltage reaches 98% of the cell target voltage, the IC enters into CV charge phase. In this phase, the VBAT voltage is regulated at target value, and the charging current reduces gradually.

8.1.4 EOC (End of Charge)

When both of below voltage condition and current condition for EOC detection are satisfied, the IC enters into EOC phase, and informs the MCU through EOC interrupt bit.

1. the cell voltage is higher than 98% of set value
2. the IBUS or IBAT current (decided by ICHAR_SEL bit) is lower than 1/10 or 1/25 (decided by EOC_SET bit) of its current limit value

In EOC phase, the IC can terminate the charging process or keep charging the battery cells, which can be set by DIS_TERM bit. If IC keeps charging, it regulates the battery cell voltage at set value.

8.1.5 Recharge

If the IC terminates the charging process after EOC is detected, the battery voltage may drop slowly due to leakage or operation current from battery cells. Once the VBAT voltage drops below 95% of the set voltage, the EOC bit is cleared, and the IC enters into CC charge phase and recharges the battery.

8.1.6 Self-adaptive Charging Current (VINREG)

The IC features dynamic power management. The allowed minimum VBUS operation voltage is VINREG threshold, which can be set by VINREG_SET register and VINREG_RATIO bit dynamically. During charging, if the IBUS charging current is higher than adapter's current capability, the adapter will be overloaded and the VBUS voltage is pulled low. Once the IC detects the VBUS voltage drops at VINREG threshold, it reduces the charging current automatically and regulates the VBUS voltage at VINREG threshold.

8.1.7 Battery Impedance Compensation

The IC provides the function of battery impedance compensation. User can set the impedance through IRCOMP

bits, then the VBAT target voltage in CV phase is compensated as

VBAT_cmp = VBAT_set + min(IBAT·IRCOMP, VCLAMP)

Where,

VBAT_cmp is the compensated battery voltage target; VBAT_set is the originally set battery termination target; IBAT is the charging current at battery side; IRCOMP is the resistance compensation value set by IRCOMP bits; VCLAMP is the allowed maximum compensation value, fixed at 125mV.

User should carefully evaluate the real battery impedance. If the value set by IRCOMP bits is higher than the real value, it will cause battery over-charge.

8.2 Discharging Mode

When EN_OTG bit is set to1, the IC enters into discharging mode. In discharging mode, the battery (VBAT) is discharged and the current flows from VBAT to VBUS.

If FB_SEL is set to 0, the VBUS output voltage is set internally, through VBUSREF_I_SET and VBUSREF_I_SET2 registers and the VBUS_RATIO bit. The VBUS can be changed dynamically, and the recommended VBUS voltage range is from 3V to 36V. When VBUS is lower than 10.24V, it is suggested to set the VBUS_RATIO to 5x, and so the minimum changing step is 10mV/step; when VBUS is higher than 10.24V, VBUS_RATIO should be set to 12.5x, and the minimum changing step is 25mV/step.

If FB_SEL is set to 1, the VBUS voltage target is set externally, that is, by the resistor divider connected at FB pin, and can be calculated as below.

$$VBUS = VBUSREF\_E \times \left(1+\frac{R_{UP}}{R_{DOWM}}\right)$$

Even if VBUS is set externally, the user can still change the VBUS voltage dynamically by changing the reference voltage VBUSREF_E through VBUSREF_E_SET and VBUSREF_E_SET2 registers. The default VBUSREF_E is 1V, and recommended VBUSREF_E voltage range is from 0.7V to 2.048V.

Please see Register Map section for details.

The IBUS current limit and IBAT current limit are still functional in discharging mode and can be changed dynamically.

It is not allowed to set any of the current limits to 0A. The minimum current limit is suggested above 0.3A.

8.2.1 Soft Start

The IC integrates soft-start control to generate VBUS voltage in discharging mode. When VBUS is lower than V_{SHORT} (typ. 1V), both IBUS and IBAT current limits are fold back to 1/10 of the setting value. Meanwhile, the IC ramps up the internal reference voltage gradually (~10ms) to avoid inrush current.

If there is a load at VBUS at the beginning of the startup, the IC may fail to boost the VBUS voltage beyond V_{SHORT} due to the 1/10 current limits for both IBUS and IBAT. If startup with loading is required, user shall set the DIS_ShortFoldBack bit to 1 to disable the current limit fold back function. After startup, the user can set DIS_ShortFoldBack bit back to 0, so to enable this function for short circuit protection. See VBUS Short Protection section for details.

8.2.2 Slew Rate Setting

When the VBUS voltage is changed dynamically through reference voltage (VBUSREF_I_SET and VBUSREF_I_SET2 registers or VBUSREF_E_SET and VBUSREF_E_SET2 registers), the reference voltage change rate can be controlled through SLEW_SET bits. For example, the VBUS is set in internal way with 5x ratio, and the VBUSREF_I = 1V at first (VBUS = 5V), then the user sets the VBUSREF_I voltage to 1.6V to get 8V output. If the slew rate is 2mV/ µs, the VBUS voltage will increase to 8V in 600mV / 2mV/µs = 300µs.

8.2.3 PFM Operation

The IC supports PFM operation in discharging mode by setting EN_PFM bit to 1. In PWM mode, the IC always works with constant switching frequency for the whole load range. This helps achieve the best output voltage performance, but the efficiency is low at light load condition because of the high switching loss.

In PFM mode, the IC still works with constant switching frequency under heavy load condition, but under light load condition, the IC automatically changes to pulse frequency modulation operation to reduce the switching loss. The efficiency can be improved under light load condition while output voltage ripple will be a little larger compared with PWM operation. Below figure shows the output voltage behavior of PFM mode.

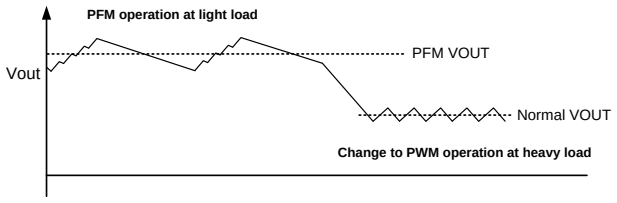


Figure 2 PFM mode illustration

8.3 ADC for Voltage and Current Monitor

The IC integrates a 10-bit ADC, so the IC can monitor the VBUS/VBAT voltages and IBUS/IBAT current no matter in charging mode or discharging mode. The ADC function is enabled after AD_START bit is set to 1. When ADC is enabled in standby mode, the IC will 0.5mA~1mA operation current. Please see Register Map section for details.

8.4 Power Path Management

The IC offers power path management function at PGATE and GPO pins. The PGATE pin can be used to drive PMOS connected at VBUS. The PGATE pin is connected to a 6 kΩ

pull down resistor internally when EN_PGATE is set to 1, and the maximum voltage between VBUS and PGATE is clamped at 7.35V; when EN_PGATE is set to 0, PGATE pin is connected to VBUS rail through a 20 kΩ pull up resistor internally

The GPO pin is an open drain output, so external pull up resistor is needed. When GPO_CTRL bit is set to 0, GPO outputs high impedance; when GPO_CTRL is set to1, GPO is pulled down internally and the pull down resistance is 6 kΩ.

User can use PGATE pin and GPO pin to control the isolation MOSFETs between adapter input and USB output as shown in Typical Application Circuit. However, the MCU or system controller controls the bits through I2C interface, which takes time for communication, so the PMOS may not be turned on/off very quickly. In the application where the isolation PMOS needs to be controlled very fast, it is suggested to use the I/O pins of MCU to control the PMOS on/off directly.

8.5 Phone Insert Detection

If connecting INDETx pin to USB-A port as shown in Typical Application Circuit, the IC can detect the phone detection. Once the IC detects a phone is inserted, it sets the INDETx interrupt bit to inform MCU. The INDETx bit is cleared after it is read by MCU.

8.6 Adapter Attachment / Detachment Detection

If connecting ACIN pin to Micro-USB port as shown in Typical Application Circuit, the IC can detect the attachment / detachment of the adapter.

Once the ACIN pin voltage is higher than 3V, which means the adapter is inserted, the IC sets the AC_OK interrupt bit to inform MCU about the attachment. If the ACIN pin voltage is lower than 3V, which means the adapter is removed, the IC clears AC_OK bit to inform the MCU about the detachment.

8.7 Switching and Frequency Dithering

The IC switches in fixed frequency which can be adjusted through FREQ_SET bits. The switching dead time can also be set through DT_SET pins. Please see Register Map section for details.

The IC also offers frequency dithering function. This function can be enabled by setting EN_DITHER bit to 1. When the function is enabled, the switching frequency is not fixed, but varies within +/- 5% range. For example, if the switching frequency is set to 300kHz (FREQ_SET = 01), the frequency will change from 285kHz to 315kHz gradually and then back to 285kHz back and forth. The time it varies from the lowest to the highest frequency or from highest to lowest frequency can be controlled by a capacitor connected at PGATE/DITHER pin as below equation shows. For example, if 100nF capacitor is connected, the time is 1.2 ms.

$$T\_dither = \frac{120\ mV \times C}{10\ \mu A}$$

When EN_DITHER is set to 1, the PGATE driver function is disabled, and the PGATE/DITHER pin only operates for dithering function.

8.8 VCC Regulator and Driver Supply

The IC integrates a regulator and generates a 6V voltage at VCC pin with typically 27 mA driving capability. The regulator is powered by the higher voltage of VBUS or VBAT.

When in Standby mode (PSTOP is pulled high), the VCC regulator is shutdown, so VCC voltage is reduced and has very limited current capability. It is not suggested to use VCC in Standby mode.

The internal driving circuit is powered from VDRV pin, and user should provide a supply at VDRV pin to power the circuit. The user can connect VCC to VDRV directly, or connect an external power supply to VDRV.

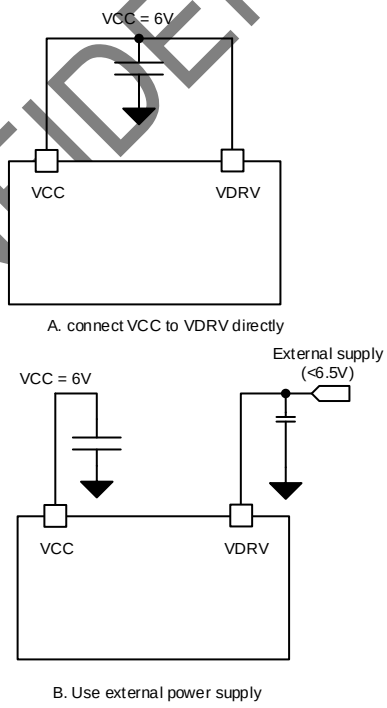


Figure 3 Supply for VDRV

8.9 Standby Mode

When /CE signal is low and PSTOP signal is high, the IC enters into Standby mode. In this mode, the IC stops switching to save the quiescent current. The other functions are still valid, and the MCU can still control the IC through I2C. However, if ADC function is enabled in Standby mode, the quiescent current will be increased to 0.5mA~1mA.

8.10 Shutdown Mode

When /CE signal is high, the IC enters into Shutdown mode. In this mode, the IC stops working and disables the I2C interface to save the power. When /CE signal is pulled low, the IC goes into Standby mode or Active mode. /CE signal is pulled down by internal resistor.

8.11 Protection

8.11.1 VBUS Over Voltage Protection

User can enabled / disable VBUS over voltage protection in discharging mode by DIS_OVP bit. When OVP is enabled, the IC stops switching when VBUS is higher than the target voltage by 10%.

8.11.2 VBAT Over Voltage Protection

The IC implements VBAT over voltage protection in both charging mode and discharging mode. Once the VBAT voltage is higher than target voltage by 10%, the IC stops switching.

8.11.3 VBUS Short Protection

In discharging mode, if the VBUS voltage is detected lower than V_{SHORT} (typ. 1V), the IC sets the VBUS_SHORT interrupt bit to inform the MCU. In the same time, it reduces IBUS current limits to 22% of the set values and IBAT current limits to 10% at the same time to protect the IC. If DIS_ShortFoldBack bit is set to 1, the current limits will not be reduced.

8.11.4 Over Temperature Protection

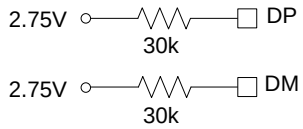
When the IC detects the junction temperature is higher than 165°C, the IC stops switching to protect the chip, and sets the OTP interrupt bit to inform the MCU. It resumes switching once the temperature drops below 15°C.

8.12 DP/DM Handshake

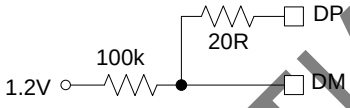
The IC integrates DP/DM physical interface. When controlled by MCU, it can realize dedicated charging port controller function or fast charge function for USB-A port in discharging mode. Besides working as output port interface, if the DP and DM pins are connected to charging port (Micro-B port or Type-C port with DP/DM), it can realize fast charge function and induces high VBUS voltage from the adapter in charging mode.

The MCU can control the DP/DM pin in different ways: 1. float the pin, 2. set the pin to source/output 0.6V/1.2V/2.75V voltage with certain output impedance, 3. sink current at the pin, 4. pulled down the pin, 5. short the DP and DM pins together. The IC can also monitor the DP/DM pin's voltage level and update the status to MCU through I2C. Please see Register Map section for details.

Below show the typical configurations for dedicated charging port function.



A. Divider mode for Apple device



B. 1.2V mode for Samsung device

Figure 4 Deticated charging port interface

To support the divider mode for Apple device as above, the MCU can set the DP/DM bits as below:

- DP_CTRL = 01 (source voltage at DP)
- DM_CTRL = 01 (source voltage at DM)
- VDP_SET = 10 (output 2.75V with 30k impedance)
- VDM_SET = 10 (output 2.75V with 30k impedance)
- SHORT_CTRL = 0 (disconnect DP and DM)

To support the divider mode for Samsung device, the MCU can set the DP/DM bits as below:

- DP_CTRL = 00 (float)
- DM_CTRL = 01 (source voltage at DM)
- VDP_SET = xx
- VDM_SET = 01 (output 1.2V with 100k impedance)
- SHORT_CTRL = 1 (short DP/DM together)

User can control the DP/DM following the fast charge protocol to realize the fast charge for charging or discharging.

8.13 I2C and Interrupt

8.13.1 I2C Interface

The IC features I2C interface, so the MCU or controller can control the IC flexibly. The 7-bit I2C address of the chip is 0x74 (8-bit address is 0xE8 for write command, 0xE9 for read command). The SDA and SCL pins are open drain and must be connected to the positive supply voltage via a current source or pull-up resistor. When the bus is free, both lines are HIGH. The I2C interface supports both standard mode (up to 100kbits) and fast mode (up to 400k bits with 5 kΩ pull up resistor at SCL pin and SDA pin respectively).

8.13.1.1 Data Validity

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. One clock pulse is generated for each data bit transferred.

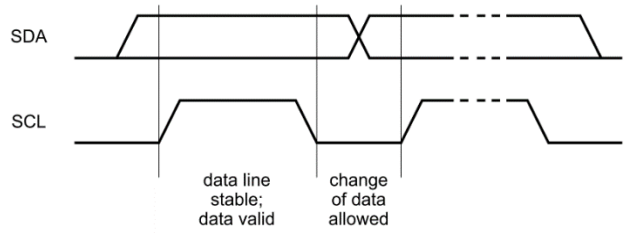


Figure 5 Bit transfer on the I2C bus

8.13.1.2 START and STOP Conditions

All transactions begin with a START (S) and are terminated by a STOP (P). A HIGH to LOW transition on the SDA line while SCL is HIGH defines a START condition. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition.

START and STOP conditions are always generated by the master. The bus is considered to be busy after the START condition. The bus is considered to be free again a certain time after the STOP condition.

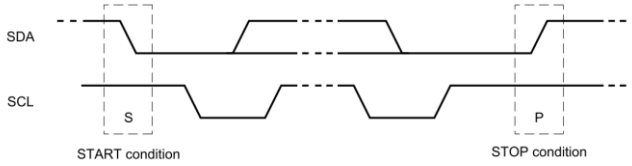


Figure 6 START and STOP conditions

8.13.1.3 Byte Format

Every byte put on the SDA line must be eight bits long. The number of bytes that can be transmitted per transfer is unrestricted. Each byte must be followed by an Acknowledge bit. Data is transferred with the Most Significant Bit (MSB) first. If a slave cannot receive or transmit another complete byte of data until it has performed some other function, for example servicing an internal interrupt, it can hold the clock line SCL LOW to force the master into a wait state. Data transfer then continues when the slave is ready for another byte of data and releases clock line SCL.

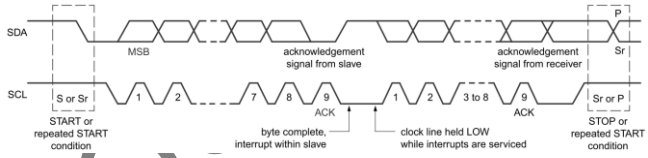


Figure 7 Data transfer on the I2C bus

8.13.1.4 Acknowledge (ACK) and Not Acknowledge (NACK)

The acknowledge takes place after every byte. The acknowledge bit allows the receiver to signal the transmitter that the byte was successfully received and another byte may be sent. During data is transferred, the master can either be the transmitter or the receiver. No matter what it is, the master generates all clock pulses, including the acknowledge ninth clock pulse.

The transmitter releases the SDA line during the acknowledge clock pulse, so the receiver can pull the SDA line LOW and it remains stable LOW during the HIGH period of this clock pulse.

When SDA remains HIGH during this ninth clock pulse, this is defined as the Not Acknowledge signal. The master can then generate either a STOP condition to abort the transfer, or a repeated START condition to start a new transfer.

8.13.1.5 The slave address and R/W bit

Data transfers follow the format shown in below. After the START condition (S), a slave address is sent. This address is seven bits long followed by an eighth bit which is a data direction bit (R/W) — a 'zero' indicates a transmission (WRITE), a 'one' indicates a request for data (READ). A data transfer is always terminated by a STOP condition (P) generated by the master. However, if a master still wishes to communicate on the bus, it can generate a repeated START condition (Sr) and address another slave without first generating a STOP condition.

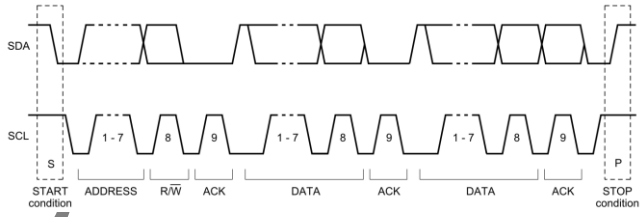


Figure 8 A complete data transfer

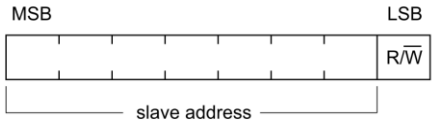


Figure 9 The first byte after the START procedure

8.13.1.6 Single Read and Write

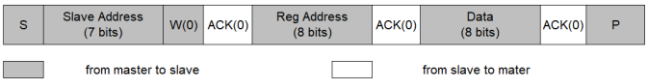


Figure 10 Single Wite

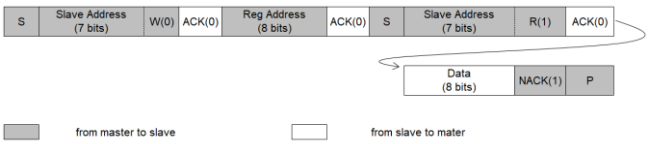


Figure 11 Single Read

If the register address is not defined, the charger IC send back NACK and go back to the idle state.

8.13.1.7 Multi-Read and Multi-Write

The IC supports multi-read and multi-write for continuous registers.

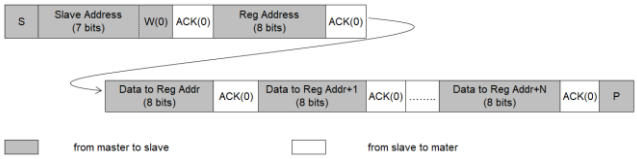


Figure 12 Multi-Write

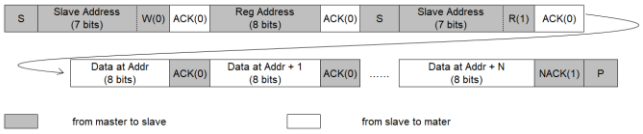


Figure 13 Multi-Read

8.13.2 Interrupt

When DM_L/AC_OK/VBUS_SHORT/OTP/EOC is set to 1, or clear to 0, the IC sends an interrupt pulse as below at INT pin to inform MCU. But only when INDET2/INDET1 is set to 1, the IC sends an interrupt pulse. It is summarized as below:

Status Signal	Interrupt Triggering Mechanism
DM_L	Rising edge or falling edge triggers 1ms_pulse INT
AC_OK	Rising edge or falling edge triggers 1ms_pulse INT
INDET2	Only rising edge triggers 1ms_pulse INT
INDET1	Only rising edge triggers 1ms_pulse INT
VBUS_SHORT	Logic high triggers continuous INT
OTP	Rising edge or falling edge triggers 1ms_pulse INT
EOC	Rising edge or falling edge triggers 1ms_pulse INT
Reserved	

The interrupt pulse at INT pin is as follow:

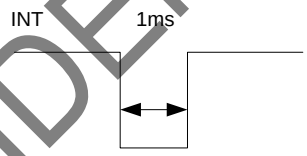


Figure 14 Interrupt pulse at INT pin

The INDET bit is read and clear type. Except INDET, all other bits in Status register represent the real time status. User can mask the interrupt output of any bit by setting its corresponding bit in Mask register. When the mask bit is set, the corresponding status bit is still set, but the IC doesn't send the interrupt at INT pin.

9 Application Information

9.1 Capacitor Selection

The switching frequency of the IC is in the range of 150kHz ~ 450kHz. Since MLCC ceramic capacitor has good high frequency filtering with low ESR, above 60μF X5R or X7R capacitors with higher voltage rating then operating voltage with margin is recommended. For example, if the highest operating Vin/Vout voltage is 12V, select at least 16V capacitor and to secure enough margin, 25V voltage rating capacitor is recommended.

The high capacitance polymer capacitor or tantalum capacitor can be used for input and output, but capacitor voltage rating must be higher than the highest operating voltage with enough margin. The high frequency characteristics of these capacitors are not as good as ceramic capacitor, so at least 10μF ceramic capacitor should be placed in parallel to reduce high frequency ripple.

9.2 Inductor Selection

1μH to 4.7 μH inductor is recommended for loop stability. The peak inductor current in discharging mode can be calculated as:

$$IL\_peak = IBAT + \frac{VBAT\cdot(VBUS-VBAT\cdot\eta)}{2\cdot fsw\cdot L\cdot VBUS} \quad (VBUS \geq VBAT)$$

$$IL\_peak = IBUS + \frac{VBUS\cdot(VBAT-VBUS)}{2\cdot fsw\cdot L\cdot VBAT\cdot\eta} \quad (VBUS < VBAT)$$

where IBAT is the battery current at VBAT side, and can be calculated as

$$IBAT = \frac{VBUS\cdot IBUS}{\eta\cdot VBAT}$$

η is the power conversion efficiency. User can use 90% for calculation.

fsw is the switching frequency

L is the inductor value

The peak inductor current in charging mode can be calculated as

$$IL\_peak = IBAT + \frac{VBAT\cdot(VBUS-VBAT)}{2\cdot fsw\cdot L\cdot VBUS\cdot\eta} \quad (VBUS > VBAT)$$

$$IL\_peak = IBUS + \frac{VBUS\cdot(VBAT-VBUS\cdot\eta)}{2\cdot fsw\cdot L\cdot VBAT} \quad (VBUS \leq VBAT)$$

where IBAT is the battery charging current at VBAT side, and can be calculated as

$$IBAT = \frac{VBUS\cdot IBUS\cdot\eta}{VBAT}$$

η is the power conversion efficiency. User can use 90% for calculation.

fsw is the switching frequency

L is the inductor value

When selecting inductor, the inductor saturation current must be higher than the peak inductor current with enough margin (20% margin is recommended). The rating current of the inductor must be higher than the battery current.

The inductor DC resistance value (DCR) affects the conduction loss of switching regulator, so low DCR inductor is recommended especially for high power application. The conductor loss of inductor can be calculated roughly as

$$PL\_DC = IL^2\cdot DCR$$

IL is the average value of inductor current, and it equals to IBAT or IBUS.

Besides DC power loss, there are also inductor AC winding loss and inductor core loss, which are related to inductor peak current. Normally, higher peak current causes higher AC loss and core loss. The user can consult with the inductor vendor to select the inductors which have small ESR at high frequency and small core loss.

9.3 Current Sense Resistor

The RSNS1 and RSNS2 are current sense resistors. 10 mΩ should be used for RSNS1 to sense IBUS current, 5 mΩ or 10 mΩ used for RSNS2 to sense IBAT current (10 mΩ supports higher battery current limit accuracy, and 5 mΩ supports higher efficiency). Resistor of 1% or higher accuracy and low temperature coefficient is recommended.

Note: If the user wants to use other resistor values, please contact factory for support.

The resistor power rating and temperature coefficient should be considered. The power dissipation is roughly calculated as $P=I^2R$, and I is the highest current flowing through the resistor. The resistor power rating should be higher than the calculated value.

Normally the resistor value is varied if the temperature increased and the variation is decided by temperature coefficient. If high accuracy of current limit is required, select lower temperature coefficient resistor as much as possible.

9.4 MOSFET Selection

The IC integrates two power MOSFETs, and the user should add two external power MOSFETs at VBAT side.

The V_{DS} of MOSFET should be higher than the highest operating voltage with enough margin (recommend more than 10V higher). For example, if the highest operating voltage is 20V, at least 30V rated V_{DS} MOSFET should be selected; If the highest operating voltage is 24V, 40V V_{DS} voltage rating should be selected.

The V_{GS} voltage rating of MOSFET should be selected higher than 8V. Considering PCB parasitic parameters during operation, MOSFET V_{GS} voltage might be higher than V_{DRV} voltage due to transient overshoot, so 10V V_{GS} is recommended to secure sufficient margin.

The MOSFET current I_D should be higher than the highest battery current with enough margin.

To ensure the sufficient current capability in relatively high

temperature circumstance, the current rate at T_A=70˚C or T_C = 100˚C should be considered. In addition, the power dissipation value P_D should also be considered and higher P_D is better in applications. Make sure that MOSFET power consumption must not exceed P_D value.

The MOSFET $R_{DS(ON)}$ and input capacitor C_{ISS} impact power efficiency directly. Typically, lower $R_{DS(ON)}$ MOSFET has higher C_{ISS}. The $R_{DS(ON)}$ is related to conduction loss. Higher R_{DSON} results in higher conduction loss, thus lower efficiency and higher thermal dissipation; the C_{ISS} is related to MOSFET switch on/off time, and longer on/off time results in higher switching loss and lower efficiency. The proper MOSEFT should be selected based on tradeoff between the $R_{DS(ON)}$ and C_{ISS}.

If high C_{ISS} MOSFET is selected, the switching on and off time become longer, then the dead time should be adjusted to avoid simultaneous turn on for both high side and low side MOSFETs.

9.5 Driver Resistor and SW Snubber Circuit

To adjust MOSFET switching time and switching overshoot for EMI debugging, it is recommended to add series resistor (0603 size) for gate driving signal (HD1 to MOS gate, LD1 to MOS gate, LD2 to MOS gate, and HD2 to MOS gate), and RC snubber (0603 size) circuit at SWx, as shown below.

The driver resistor should be placed near MOS. At first, use 0Ω resistors; if switching overshoot is big, increase the resistor value to slow down the switching speed. It is suggested to keep the resistor value < 10 Ω. While the switching speed gets slower, the default dead time may not be enough to avoid overshoot of the power MOSFETs. So if higher than 10Ω is needed, user should increase the dead time if necessary.

The RC snubber circuit at SWx node is also helpful in absorbing the high frequency spike at SWx node, so to improve EMC performance. User can leave RC components as NC at the beginning, and adjust the value to improve the EMC performance if necessary. Normally user can try 2.2Ω and 1nF for the snubber. If EMC should be improved further, reduce the resistor value (like 1 Ω or even lower) and increase the capacitor value (like 2.2nF or even higher).

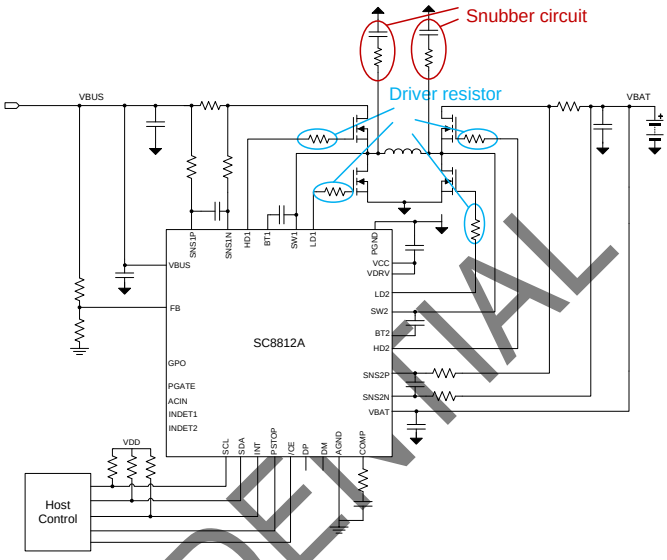


Figure 15 Driver resistor and snubber circuit

9.6 Layout Guide

1. The 1uF capacitors connected at VBUS/VBAT/VCC/VDRV pins should be placed near the IC, and their ground connection to the ground pins should be as short as possible.

a. component(s) on schematic:

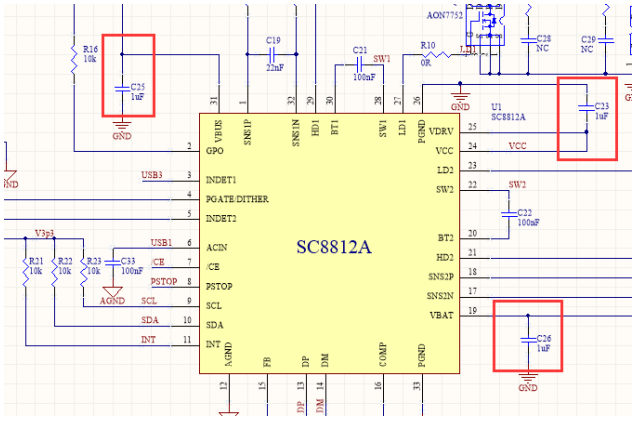


Figure 16 Schematic

b. **Layout example**: put the three capacitors near IC on the top layer. Connect the capacitors to each pin on the same layer, and connect the capacitors to ground pour through vias.

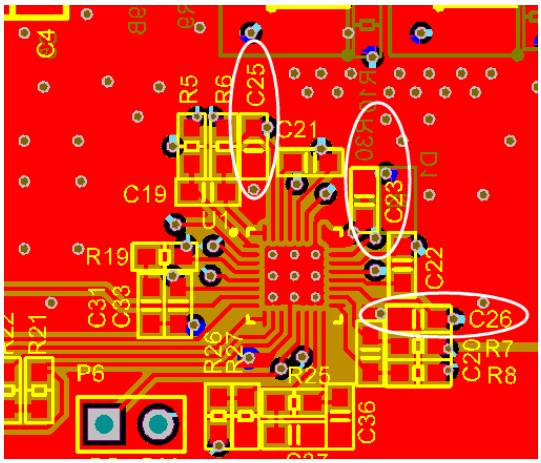


Figure 17 Top layer (flip view)

2. Put IBUS current sense resistor, MOSFETs and bulk capacitor at VBUS side as close as possible. And the low side MOSFET and bulk capacitors should be very close to PGND pins. Between current sense resistor and high side MOS, add a 100nF 0402 capacitor to PGND. It is helpful to suppress high frequency noise. Put it very close to MOS and PGND pins.

   a. component(s) on schematic

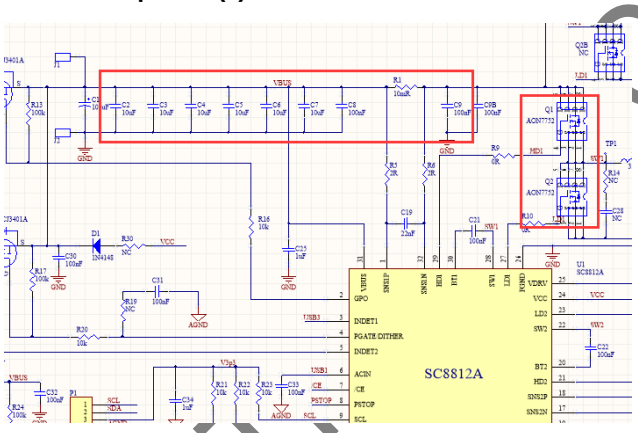


Figure 18 Schematic

   b. **Layout example**: put all these components on the top layer as a group, and the VBUS and PGND power paths should be as wide as possible. The low side MOS, 100nF capacitor and the bulk capacitors connected to PGND pins through ground pour on both top layer and bottom layer.

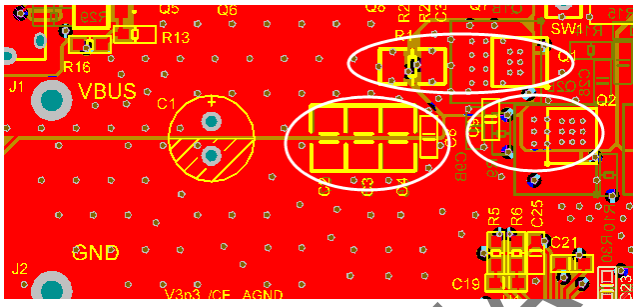


Figure 19 Top layer (flip view)

3. Put IBAT current sense resistor, MOSFETs and bulk capacitor at VBAT side as close as possible. And the low side MOSFET and bulk capacitors should be very close to PGND pins. Between current sense resistor and high side MOS, add a 100nF 0402 capacitor to PGND. It is helpful to suppress high frequency noise. Put it very close to MOS and PGND pins.

   a. component(s) on schematic

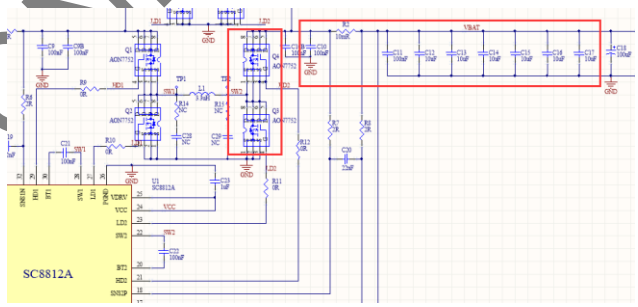


Figure 20 Schematic

   b. **Layout example**: put all these components on the top layer as a group, and the VBAT and PGND power paths should be as wide as possible. The low side MOS, 100nF capacitor and the bulk capacitors connected to PGND pins through ground pour on both top layer and bottom layer.

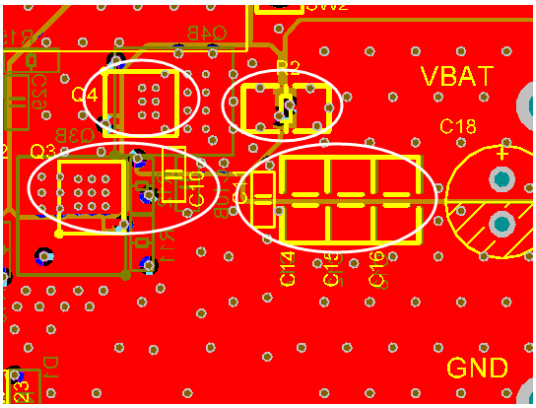


Figure 21 Top layer view

4. The driver signals (LD1 / HD1 / SW1 / LD2 / HD2 / SW2) as shown below should be routed with wide traces (≥ 15 mil). The driver resistors should be placed near MOS. The HDx and SWx should be routed in parallel, close to each other; the LDx should be routed in parallel with PGND traces (≥ 15 mil) or close to PGND pour. There should be wide space filled with PGND between LDx and HDx and also wide space from LDx to SWx to avoid interference.

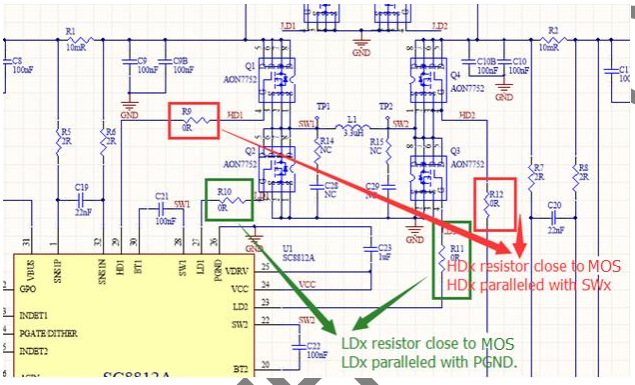


Figure 22 Schematic

5. The current sense traces should be connected to the current sense resistor's pads in Kelvin sense way as below, and routed in parallel (differential routing), and add filter for each current sense near the IC.

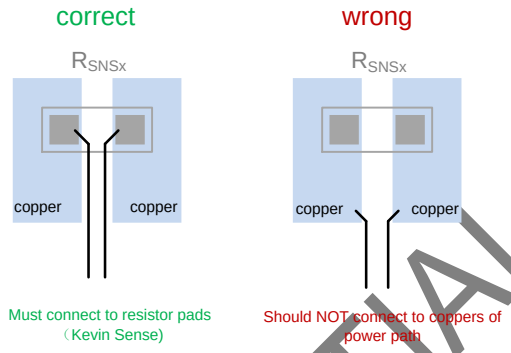


Figure 23 Current sense

a. component(s) on schematic

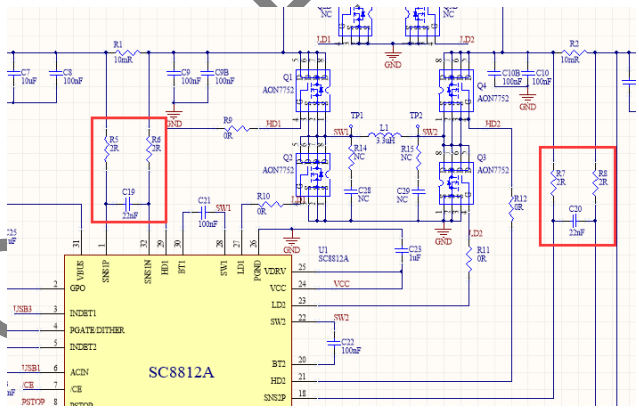


Figure 24 Schematic

b. **Layout example**: The current sense resistor R1 and R2 should be placed near the power MOSFETs, so it might be far from the IC. The sense filter should be placed near the IC. The traces can be routed on other layer (3rd layer in this example), but should route the traces in parallel (differential way), far away from switching signals and isolated them with PGND pour.

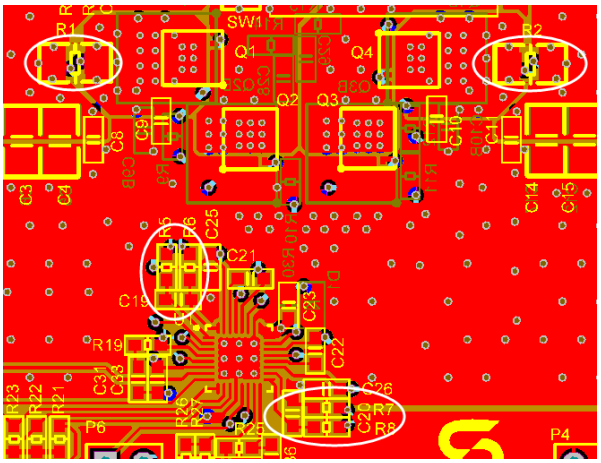


Figure 25 Top layer view

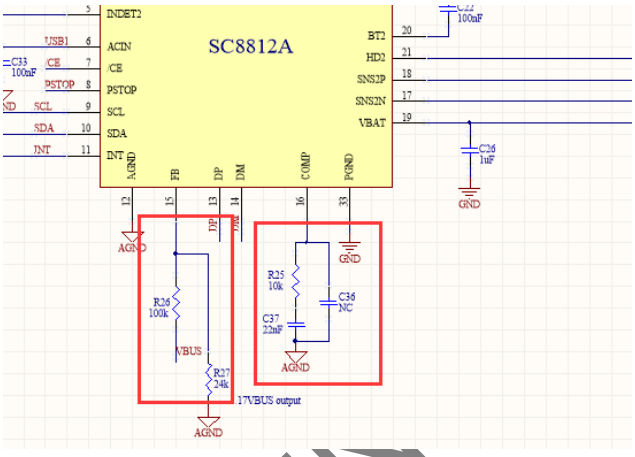


Figure 27 Schematic

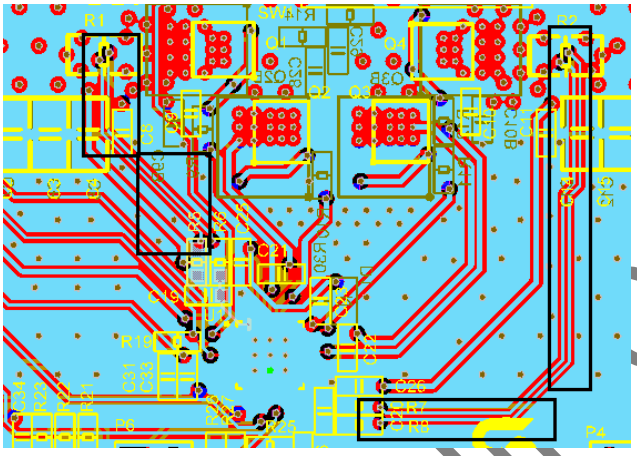


Figure 26 Middle-2 layer view

6. The components for analog signals (e.g. FB resistor divider, COMP pin components, etc) should be placed near IC, and connect to AGND (analog ground) pin. Then connect the AGND pin and PGNDs at the PGND pad under IC. Place vias at PGND pad for better thermal dissipation.
   a. component(s) on schematic

b. **Layout example**: analog components are placed near the IC, and the AGND are connected with PGND at PGND pad.

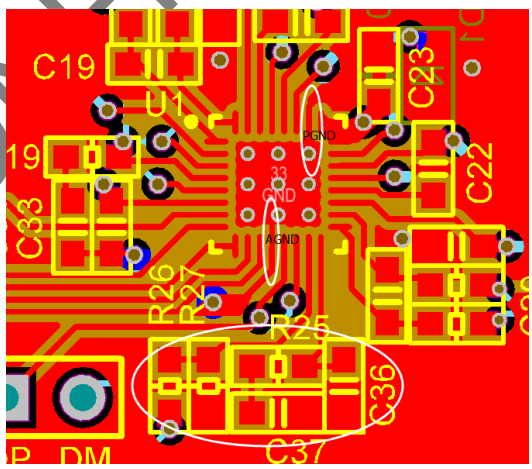


Figure 28 Top layer view

10 Register Map

7-bit address: 0x74; 8-bit address: 0xE8 for write command; 0xE9 for read command.

Addr	Register	Type	Default value @POR	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00H	VBAT_SET	R/W	0000 0001	IRCOMP		Reserved	CSEL		VCELL_SET		
01H	VBUSREF_I_SET	R/W	0011 0001	VBUSREF_I_SET							
02H	VBUSREF_I_SET2	R/W	11xx xxxx	VBUSREF_I_SET _2		Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
03H	VBUSREF_E_SET	R/W	0111 1100	VBUSREF_E_SET							
04H	VBUSREF_E_SET2	R/W	11xx xxxx	VBUSREF_E_SET _2		Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
05H	IBUS_LIM_SET	R/W	1111 1111	IBUS_LIM setting							
06H	IBAT_LIM_SET	R/W	1111 1111	IBAT_LIM setting							
07H	VINREG_SET	R/W	0010 1100	VINREG voltage setting							
08H	RATIO	R/W	0011 1000	Reserved		Reserved	IBAT_RATIO	IBUS_RATIO		VBAT_MON_ RATIO	VBUS_RATIO
09H	CTRL0_SET	R/W	0000 0100	EN_OTG	Reserved	Reserved	VINREG_RATIO	FREQ_SET		DT_SET	
0AH	CTRL1_SET	R/W	0000 0001	ICHAR_SEL	DIS_TRICKLE	DIS_TERM	FB_SEL	TRICKLE_SET	DIS_OVP	Reserved	Reserved
0BH	CTRL2_SET	R/W	0000 0001	Reserved		SoftStart_SET		FACTORY	EN_DITHER	SLEW_SET	
0CH	CTRL3_SET	R/W	0000 0010	EN_PGATE	GPO_CTRL	AD_START	ILIM_BW_SEL	LOOP_SET	DIS_ShortFoldBack	EOC_SET	EN_PFM
0DH	VBUS_FB_VALUE	R	0000 0000	VBUS_FB_value							
0EH	VBUS_FB_VALUE2	R	0000 0000	VBUS_FB_value2		Reserved					
0FH	VBAT_FB_VALUE	R	0000 0000	VBAT_FB_value							
10H	VBAT_FB_VALUE2	R	0000 0000	VBAT_FB_value2		Reserved					
11H	IBUS_VALUE	R	0000 0000	IBUS_value							
12H	IBUS_VALUE2	R	0000 0000	IBUS_value2		Reserved					
13H	IBAT_VALUE	R	0000 0000	IBAT_value							
14H	IBAT_VALUE2	R	0000 0000	IBAT_value2		Reserved					
15H	Reserved	R	0000 0000	Reserved							
16H	Reserved	R	0000 0000	Reserved							
17H	STATUS	R	0000 0000	DM_L	AC_OK	INDET2	INDET1	VBUS_SHORT	OTP	EOC	Reserved
18H	Reserved	R	0000 0000	Reserved							
19H	MASK	R/W	1000 0000	DM_L_Mask	AC_OK_Mask	INDET2_Mask	INDET1_Mask	VBUS_SHORT_ Mask	OTP_Mask	EOC_Mask	Reserved
1AH	DP/DM_CTRL	R/W	0000 0000	DP_CTRL		VDP_SET		DM_CTRL		VDM_SET	
1BH	DP/DM_READ	R/W	xxx0 0000	Reserved			SHORT_CTRL	VDP_RD		VDM_RD	

Table 1 0x00 VBAT_SET Register

Bit	Mode	Bit Name	Default value @POR	Description	Notes
7-6	R/W	IRCOMP	00	Battery IR compensation setting: 00: 0 mΩ (default) 01: 20 mΩ 10: 40 mΩ 11: 80 mΩ	
5	R/W	Reserved	0	**Internal use. Don't overwrite this bit.**	
4-3	R/W	CSEL	00	Battery cell selection, only valid for internal VBAT voltage setting 00: 1S battery (default) 01: 2S battery 10: 3S battery 11: 4S battery	
2-0	R/W	VCELL_SET	001	Battery voltage setting per cell, only valid for internal VBAT voltage setting 000: 4.1V 001: 4.2V (default) 010: 4.25V 011: 4.3V 100: 4.35V 101: 4.4V 110: 4.45V 111: 4.5V	

Table 2 0x01 VBUSREF_I_SET Register

Bit	Mode	Bit Name	Default value @POR	Description	Notes
7-0	R/W	VBUSREF_I_SET	0011 0001	Reference voltage programming for internal VBUS voltage setting. When FB_SEL = 0 (internal VBUS setting), set the highest 8-bit of the reference voltage for VBUS (total 10-bit programming). The internal reference voltage is calculated as VBUSREF_I = (4 x VBUSREF_I_SET + VBUSREF_I_SET2 + 1) x 2 mV The VBUS output voltage is calculated as VBUS = VBUSREF_I x VBUS_RATIO VBUSREF_I_SET range: 0 ~ 255 0000 0000: 0 0000 0001: 1 0000 0010: 2 …. 0011 0001: 49 (default)	

				…. 1111 1111: 255 The default reference voltage is (4 x 49 +3+1) x 2 mV = 400 mV; the default VBUS output voltage with FB_SEL = 0 is 400mV x 12.5 = 5V	

Table 3 0x02 VBUSREF_I_SET_2 Register

Bit	Mode	Bit Name	Default value @POR	Description	Notes
7-6	R/W	VBUSREF_I_SET2	11	Reference voltage programming for internal VBUS voltage setting. When FB_SEL = 0 (internal VBUS setting), set the lowest 2-bit of the reference voltage for VBUS (total 10-bit programming). The internal reference voltage is calculated as VBUSREF_I = (4 x VBUSREF_I_SET + VBUSREF_I_SET2 + 1) x 2 mV The VBUS output voltage is calculated as VBUS = VBUSREF_I x VBUS_RATIO VBUSREF_I_SET2 range: 0 ~ 3 00: 0 01: 1 10: 2 11: 3 (default)	
5-0		Reserved	xx xxxx		

Table 4 0x03 VBUSREF_E_SET Register

Bit	Mode	Bit Name	Default value @POR	Description	Notes
7-0	R/W	VBUSREF_E_SET	0111 1100	Reference voltage programming for external VBUS voltage setting. When FB_SEL = 1 (external VBUS setting), set the highest 8-bit of the reference voltage for VBUS (total 10-bit programming). The external reference voltage is calculated as VBUSREF_E = (4 x VBUSREF_E_SET+VBUSREF_E_SET2+1) x 2mV The VBUS output voltage is calculated as $VBUS = VBUSREF\_E \times (1+\frac{RUP}{RDOWM})$ VBUSREF_E_SET range: 0 ~ 255 0000 0000: 0 0000 0001: 1 0000 0010: 2 …. 0111 1100: 124 (default) ….	

				1111 1111: 255 The default reference voltage is (4 x 124 +3 +1) x 2 mV = 1 V	

Table 5 0x04 VBUSREF_E_SET_2 Register

Bit	Mode	Bit Name	Default value @POR	Description	Notes
7-6	R/W	VBUSREF_E_SET2	11	Reference voltage programming for external VBUS voltage setting. When FB_SEL = 1 (external VBUS setting), set the lowest 2-bit of the reference voltage for VBUS (total 10-bit programming). The external reference voltage is calculated as VBUSREF_E = (4 x VBUSREF_E_SET+VBUSREF_E_SET2+1) x 2mV The VBUS output voltage is calculated as $VBUS = VBUSREF\_E \times (1+\frac{RUP}{RDOWM})$ VBUSREF_E_SET2 range: 0 ~ 3 00: 0 01: 1 10: 2 11: 3 (default)	
5-0		Reserved	xx xxxx		

Table 6 0x05 IBUS_LIM_SET Register

Bit	Mode	Bit Name	Default value @POR	Description	Notes
7-0	R/W	IBUS_LIM_SET	1111 1111	Set IBUS current limit, which is valid for both charging and discharging modes. $IBUS\_LIM\ (A) = \frac{(IBUS\_LIM\_SET+1)}{256} \times IBUS\_RATIO \times \frac{10\ m\Omega}{RS1}$ RS1 is the current sense resistor at VBUS side. IBUS_LIM_SET range: 0 ~ 255 0000 0000: 0 0000 0001: 1 0000 0010: 2 … 1111 1111: 255 (default) E.g., if RS1 = 10 mΩ, the default IBUS current limit is (255+1)/256 x 3 x 10 mΩ / 10 mΩ = 3 A	**IBUS_LIM_SET must be >=300mA**

Table 7 0x06 IBAT_LIM_SET Register

Bit	Mode	Bit Name	Default value @POR	Description	Notes
7-0	R/W	IBAT_LIM_SET	1111 1111	Set IBAT current limit, which is valid for both charging and discharging modes. $IBAT\_LIM\ (A) = \frac{IBAT\_LIM\_SET+1}{256} \times IBAT\_RATIO \times \frac{10\ m\Omega}{RS2}$ RS2 is the current sense resistor at VBAT side. IBAT_LIM_SET range: 0 ~ 255 0000 0000: 0 0000 0001: 1 0000 0010: 2 … 1111 1111: 255 (default) E.g., if RS2 = 10 mΩ, the default IBAT current limit is (255+1)/256 x 12 x 10 mΩ / 10 mΩ = 12 A	**IBAT_LIM_SET must be >=300mA**

Table 8 0x07 VINREG_SET Register

Bit	Mode	Bit Name	Default value @POR	Description	Notes
7-0	R/W	VINREG_SET	0010 1100	Set VINREG reference voltage for charging mode. VINREG = (VINREG_SET+1) × VINREG_RATIO (mV) VINREG_SET range: 0 ~ 255 0000 0000: 0 0000 0001: 1 … 0010 1100: 44 (default) … 1111 1111: 255 If VINREG_RATIO = 1 (40x), the default VINREG voltage is 1.8V, and the maximum VINREG voltage which can be set is 10.24V; If VINREG_RATIO = 0 (100x), the default VINREG voltage is 4.5V, and the maximum VINREG voltage which can be set is 25.6V.	

Table 9 0x08 RATIO Register

Bit	Mode	Bit Name	Default value @POR	Description	Notes
7-6	R/W	Reserved	00	**Internal use. Don't overwrite this bit.**	
5	R/W	Reserved	1	**Internal use. Don't overwrite this bit.**	
4	R/W	IBAT_RATIO	1	IBAT_LIM setting ratio	

				0: 6x 1: 12x (default)	
3-2	R/W	IBUS_RATIO	10	IBUS_LIM setting ratio 00: not allowed 01: 6x 10: 3x (default) 11: not allowed	
1	R/W	VBAT_MON_RATIO	0	Ratio setting for VBAT voltage monitor 0: 12.5x (default) 1: 5x The battery voltage is monitored through ADC and can be calculated as below: VBAT = (4 x VBAT_FB_VALUE + VBAT_FB_VALUE2 + 1) x VBAT_MON_RATIO x 2 mV VBAT_FB_VALUE and VBAT_FB_VALUE2 are ADC register values. **For 1S and 2S battery applications (VBAT < 9V), set this bit to 1.**	
0	R/W	VBUS_RATIO	0	Set the ratio for VBUS voltage setting and VBUS voltage monitor. 0: 12.5x (default) 1: 5x	

Table 10 0x09 CTRL0_SET Register

Bit	Mode	Bit Name	Default value @POR	Description	Notes
7	R/W	EN_OTG	0	Enable OTG operation 0: set the charger to work in charging mode (default) 1: set the charger to work in discharging mode	
6	R/W	Reserved	0	**Internal use. Don't overwrite this bit.**	
5	R/W	Reserved	0	**Internal use. Don't overwrite this bit.**	
4	R/W	VINREG_RATIO	0	VINREG setting ratio 0: 100x (default) 1: 40x **Choose 40x ratio when VINREG target value < 10V.**	
3-2	R/W	FREQ_SET	01	Switching frequency setting 00: 150kHz 01: 300kHz (default) 10: Reserved 11: 450kHz	
1-0	R/W	DT_SET	00	Switching dead time setting 00: 20ns (default)	

				01: 40ns 10: 60ns 11: 80ns	

Table 11 0x0A CTRL1_SET Register

Bit	Mode	Symbol	Default value @POR	Description	Notes
7	R/W	ICHAR_SEL	0	Charging current selection 0: IBUS as charging current, the trickle charging current and termination current will be based on IBUS (default) 1: IBAT as charging current, the trickle charging current and termination current will be based on IBAT	
6	R/W	DIS_TRICKLE	0	Trickle charge control 0: enable trickle charge phase (default) 1: disable trickle charge phase	
5	R/W	DIS_TERM	0	Charging termination control 0: enable auto-termination (default) 1: disable auto-termination	
4	R/W	FB_SEL	0	VBUS voltage setting control, only for discharging mode 0: internal VBUS setting, VBUS output voltage is set by VBUS_RATIO bit and VBUSREF_I_SET bits (default) 1: external VBUS setting, VBUS output voltage is set by resistor divider at FB pin	
3	R/W	Trickle _SET	0	Trickle charge phase threshold setting 0: 70% of VBAT voltage setting (default) 1: 60% of VBAT voltage setting	
2	R/W	DIS_OVP	0	OVP protection setting for discharging mode 0: enable OVP protection (default) 1: disable OVP protection	
1	R/W	Reserved	0	**Internal use. Don't overwrite this bit.**	
0	R/W	Reserved	1	**Internal use. Don't overwrite this bit.**	

Table 12 0x0B CTRL2_SET Register

Bit	Mode	Symbol	Default value @POR	Description	Notes
7-6	R/W	Reserved	00	**Internal use. Don't overwrite this bit.**	
5-4	R/W	SoftStart_SET	00	Soft start slew rate setting 00: 0.0625mV/μs (default) 01: 0.125mV/μs	

				10: 0.25mV/μs 11: 0.5mV/μs	
3	R/W	FACTORY	0	**Factory setting bit. MCU shall write this bit to 1 after power up.**	
2	R/W	EN_DITHER	0	Enable switching frequency dithering function at PGATE pin: 0: disable frequency dithering function, PGATE pin used as PMOS gate control (default) 1: enable frequency dithering function, PGATE pin used to set the frequency dithering	
1-0	R/W	SLEW_SET	01	Slew rate setting for VBUS dynamic change in discharging mode 00: 1mV/μs 01: 2mV/μs (default) 10: 4mV/μs 11: 8mV/μs	

Table 13 0x0C CTRL3_SET Register

Bit	Mode	Symbol	Default value @POR	Description	Notes
7	R/W	EN_PGATE	0	PGATE control 0: PGATE outputs logic high to turn off PMOS (default) 1: PGATE outputs logic low to turn on PMOS	
6	R/W	GPO_CTRL	0	GPO output control 0: Open drain output (default) 1: Logic low output	
5	R/W	AD_START	0	ADC control 0: stop ADC conversion (default) 1: start ADC conversion, MCU can read the voltage/current values from ADC registers	
4	R/W	ILIM_BW_SEL	0	ILIM loop bandwidth setting: 0: 5kHz (default) 1: 1.25kHz	
3	R/W	LOOP_SET	0	Loop response control 0: Normal loop response (default) 1: Improve the loop response	
2	R/W	DIS_ShortFold Back	0	IBUS and IBAT current foldback control for VBUS short circuit condition, only valid in discharging mode 0: IBUS and IBAT current limit value are fold-back to 22% and 10% of setting value respectively (default) 1: disable fold-back.	
1	R/W	EOC_SET	1	Current threshold setting for End Of Charging (EOC) detection 0: 1/25 of charging current 1: 1/10 of charging current (default)	

				1/25 option is not recommended for ≤ 2A ILIMx setting.	
0	R/W	EN_PFM	0	PFM control under light load condition, only for discharging mode 0: disable PFM mode (PWM mode enabled) (default) 1: enable PFM mode	

Table 14 0x0D VBUS_FB_VALUE Register

Bit	Mode	Symbol	Default value @POR	Description	Notes
7-0	R	VBUS_FB_VALUE	0000 0000	The highest 8-bit of the ADC reading of VBUS voltage (total 10-bit). VBUS voltage is calculated as VBUS = (4 x VBUS_FB_VALUE + VBUS_FB_VALUE2 + 1) x VBUS_RATIO x 2 mV VBUS_FB_VALUE range: 0 ~ 255 0000 0000: 0 0000 0001: 1 0000 0010: 2 …. 1111 1111: 255	

Table 15 0x0E VBUS_FB_VALUE_2 Register

Bit	Mode	Symbol	Default value @POR	Description	Notes
7-6	R	VBUS_FB_VALUE2	00	The lowest 2-bit of the ADC reading of VBUS voltage (total 10-bit). VBUS voltage is calculated as VBUS voltage is calculated as VBUS = (4 x VBUS_FB_VALUE + VBUS_FB_VALUE2 + 1) x VBUS_RATIO x 2 mV VBUS_FB_VALUE2 range: 0 ~ 3 00: 0 01: 1 10: 2 11: 3	
5-0		Reserved	00 0000		

Table 16 0x0F VBAT_FB_VALUE Register

Bit	Mode	Symbol	Default value @POR	Description	Notes

7-0	R	VBAT_FB_VALUE	0000 0000	The highest 8-bit of the ADC reading of VBAT voltage (total 10-bit). VBAT voltage is calculated as VBAT = (4 x VBAT_FB_VALUE + VBAT_FB_VALUE2 + 1) x VBAT_MON_RATIO x 2 mV VBAT_FB_VALUE range: 0 ~ 255 0000 0000: 0 0000 0001: 1 0000 0010: 2 …. 1111 1111: 255	

Table 17 0x10 VBAT_FB_VALUE_2 Register

Bit	Mode	Symbol	Default value @POR	Description	Notes
7-6	R	VBAT_FB_VALUE_2	00	The lowest 2-bit of the ADC reading of VBAT voltage (total 10-bit). VBAT voltage is calculated as VBAT = (4 x VBAT_FB_VALUE + VBAT_FB_VALUE2 + 1) x VBAT_MON_RATIO x 2 mV VBAT_FB_VALUE_2 range: 0 ~ 3 00: 0 01: 1 10: 2 11: 3	
5-0		Reserved	00 0000		

Table 18 0x11 IBUS_VALUE Register

Bit	Mode	Symbol	Default value @POR	Description	Notes
7-0	R	IBUS_VALUE	0000 0000	The highest 8-bit of the ADC reading of IBUS current (total 10-bit). IBUS current is calculated as $\text{IBUS (A)} = \frac{(4 \times \text{IBUS\_VALUE} + \text{IBUS\_VALUE2} + 1) \times 2}{1200} \times \text{IBUS\_RATIO} \times \frac{10\ \text{m}\Omega}{\text{RS1}}$ IBUS_VALUE range: 0 ~ 255 0000 0000: 0 0000 0001: 1 0000 0010: 2 …. 1111 1111: 255	

Table 19 0x12 IBUS_VALUE_2 Register

Bit	Mode	Symbol	Default value @POR	Description	Notes
7-6	R	IBUS_VALUE 2	00	The lowest 2-bit of the ADC reading of IBUS current (total 10-bit). IBUS current is calculated as $IBUS\ (A) = \frac{(4 \times IBUS\_VALUE + IBUS\_VALUE2 + 1)\times 2}{1200} \times IBUS\_RATIO \times \frac{10\ m\Omega}{RS1}$ IBUS_VALUE2 range: 0 ~ 3 00: 0 01: 1 10: 2 11: 3	
5-0		Reserved	00 0000		

Table 20 0x13 IBAT_VALUE Register

Bit	Mode	Symbol	Default value @POR	Description	Notes
7-0	R	IBAT_VALUE	0000 0000	The highest 8-bit of the ADC reading of IBAT current (total 10-bit). IBAT current is calculated as $IBAT\ (A) = \frac{(4 \times IBAT\_VALUE + IBAT\_VALUE2 + 1)\times 2}{1200} \times IBAT\_RATIO \times \frac{10\ m\Omega}{RS2}$ IBAT_VALUE range: 0 ~ 255 0000 0000: 0 0000 0001: 1 0000 0010: 2 …. 1111 1111: 255	

Table 21 0x14 IBAT_VALUE_2 Register

Bit	Mode	Symbol	Default value @POR	Description	Notes
7-6	R	IBAT_VALUE 2	00	The lowest 2-bit of the ADC reading of IBAT current (total 10-bit). IBAT current is calculated as $IBAT\ (A) = \frac{(4 \times IBAT\_VALUE + IBAT\_VALUE2 + 1)\times 2}{1200} \times IBAT\_RATIO \times \frac{10\ m\Omega}{RS2}$ IBAT_VALUE2 range: 0 ~ 3	

				00: 0 01: 1 10: 2 11: 3	
5-0		Reserved	00 0000		

Table 22 0x17 STATUS Register

Bit	Mode	Symbol	Default value @POR	Description	Notes
7	R	DM_L	0	1: DM voltage is detected lower than 0.325V	
6	R	AC_OK	0	1: AC adapter is inserted	
5	R	INDET2	0	1: USB-A load insert is detected at INDET pin	
4	R	INDET1	0	1: USB-A load insert is detected at INDET1 pin	
3	R	VBUS_SHORT	0	1: VBUS short circuit fault happens in discharging mode	
2	R	OTP	0	1: OTP fault happens	
1	R	EOC	0	1: EOC conditions are satisfied	
0	R	Reserved	0	Reserved	

Table 23 0x19 MASK Register

Bit	Mode	Symbol	Default value @POR	Description	Notes
7	R/W	DM_L_Mask	1	1: Interrupt is disabled	
6	R/W	AC_OK_Mask	0	1: Interrupt is disabled	
5	R/W	INDET2_Mask	0	1: Interrupt is disabled	
4	R/W	INDET1_Mask	0	1: Interrupt is disabled	
3	R/W	VBUS_SHORT_ Mask	0	1: Interrupt is disabled	
2	R/W	OTP_Mask	0	1: Interrupt is disabled	
1	R/W	EOC_Mask	0	1: Interrupt is disabled	
0	R/W	Reserved	0	**Internal use. Don't overwrite this bit.**	

Table 24 0x1A DP/DM_CTRL Register

Bit	Mode	Symbol	Default value @POR	Description	Notes
7-6	R/W	DP_CTRL	00	00: float DP pin (default) 01: source: output a voltage at DP pin 10: sink: turn on sink current (100 μA) at DP pin 11: pull down: turn on the pull down resistor (19.53 kΩ) at DP pin	
5-4	R/W	VDP_SET	00	Set the output voltage at DP pin 00: 0.6V (default) 01: 1.2V with 100 kΩ output impedance at DP pin 10: 2.75V with 30 kΩ output impedance at DP pin 11: 2.75V	
3-2	R/W	DM_CTRL	00	00: float DM pin (default) 01: source: output a voltage at DM pin 10: sink: turn on sink current (100 μA) at DM pin 11: pull down: turn on the pull down resistor (19.53 kΩ) at DM pin	
1-0	R/W	VDM_SET	00	Set the output voltage at DM pin 00: 0.6V (default) 01: 1.2V with 100 kΩ output impedance at DP pin 10: 2.75V with 30 kΩ output impedance at DP pin 11: 2.75V	

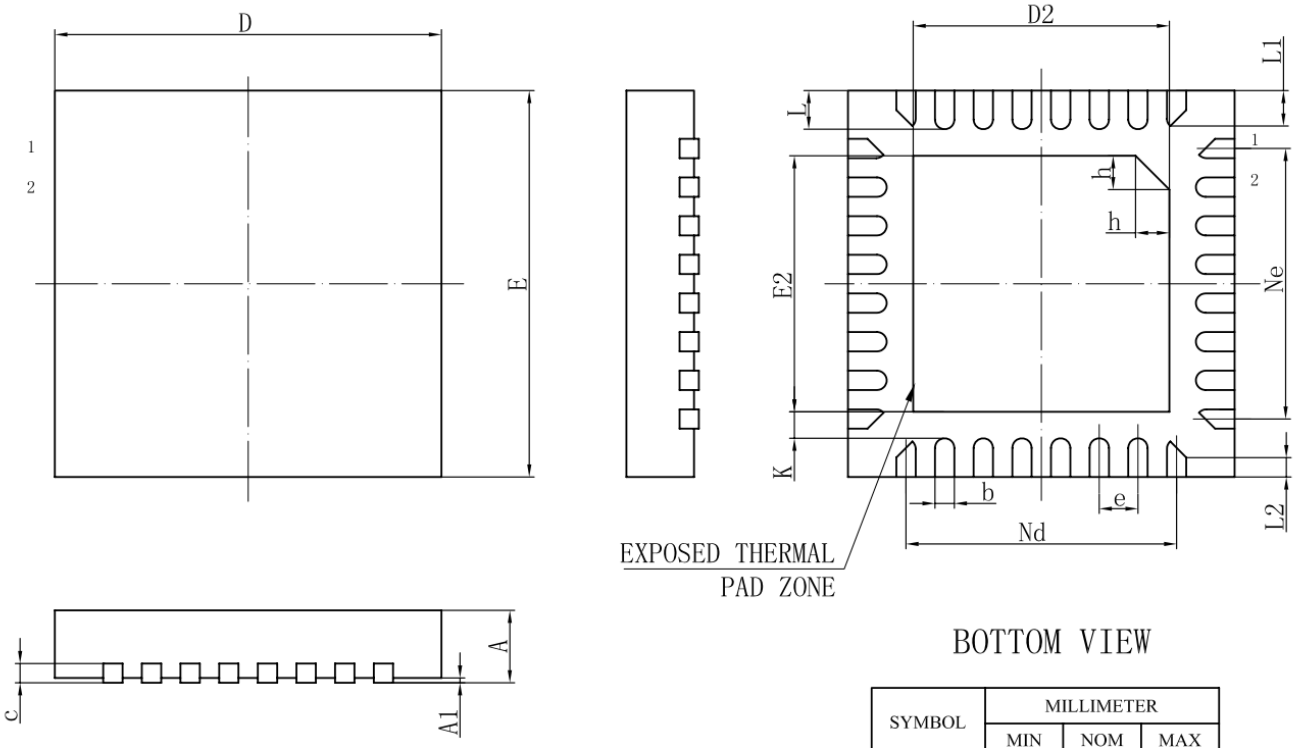
Table 25 0x1B DP/DM_READ Register

Bit	Mode	Symbol	Default value @POR	Description	Notes
7-5		Reserved	xxx		
4	R/W	SHORT_CTRL	0	Short DP pin and DM pin through 20 Ω resistor 0: no, disconnect (default) 1: yes, short	
3-2	R	VDP_RD	00	DP pin voltage reading 00: < 0.325V 01: 0.325V ~0.84V 10: 0.84V ~ 2.05V 11: >2.05V	
1-0	R	VDM_RD	00	DM pin voltage reading 00: < 0.325V 01: 0.325V ~0.84V 10: 0.84V ~ 2.05V	

				11: >2.05V	

MECHANICAL DATA

QFN32L(0404x0.75-0.40)



BOTTOM VIEW

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.25
D	3.90	4.00	4.10
D2	2.60	2.65	2.70
e	0.40BSC		
Nd	2.80BSC		
E	3.90	4.00	4.10
E2	2.60	2.65	2.70
Ne	2.80BSC		
K	0.20	-	-
L	0.35	0.40	0.45
L1	0.30	0.35	0.40
L2	0.15	0.20	0.25
h	0.30	0.35	0.40
L/F载体尺寸 (Mil)	112*112		