



PRODUCT DATA SHEET

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Datasheet



Resources



Samples

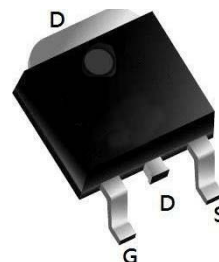
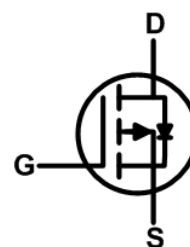
Please note: Please check the JINGAO Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.jg-semi.cn. Please email any questions regarding the system integration to JINGAO_questions@jgsemi.com.

Features

- Split Gate Trench MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$

Applications

- DC-DC Converters
- Power management functions
- Synchronous-rectification applications


TO252-3L


Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$, unless otherwise noted!)

Symbol	Parameter		Value	Units
VDSS	Drain-to-Source Voltage		-60	V
ID	Continuous Drain Current	TC = 25 °C	-60	A
	Continuous Drain Current	TC = 100 °C	-35	A
IDMa1	Pulsed Drain Current		-220	A
VGS	Gate-to-Source Voltage		±20	V
PD	Power Dissipation		100	W
EAS a2	Single pulse avalanche energy		337	mJ
TJ, TSTG	Operating Junction and Storage Temperature Range		150, -55 to 150	°C
TL	Maximum Temperature for Soldering		260	°C

Thermal Characteristics

Symbol	Parameter	Value	Units
RθJC	Thermal Resistance, Junction-to-Case	1.25	°C/W
RθJA	Thermal Resistance, Junction-to-Ambient	60	°C/W

T_J= 25°C unless otherwise specified)

Static Characteristics						
Symbol	Parameter	Test Conditions	Value			Units
			Min.	Typ.	Max.	
VDSS	Drain to Source Breakdown Voltage	V _{GS} =0V, I _D =-250μA	-60	--	--	V
IDSS	Drain to Source Leakage Current	V _{DS} = -60V, V _{GS} = 0V	--	--	1	μA
IGSS(F)	Gate to Source Forward Leakage	V _{GS} =-20V	--	--	100	nA
IGSS(R)	Gate to Source Reverse Leakage	V _{GS} =+20V	--	--	-100	nA
VGS(TH)	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =-250μA	-1.3	-1.8	-2.3	V
RDS(ON) 1	Drain-to-Source Resistance	On- V _{GS} =-10V, I _D =-20A	--	12	16	mΩ
RDS(ON) 2	Drain-to-Source Resistance	On- V _{GS} =-4.5V, I _D =-10A	--	18	20	mΩ

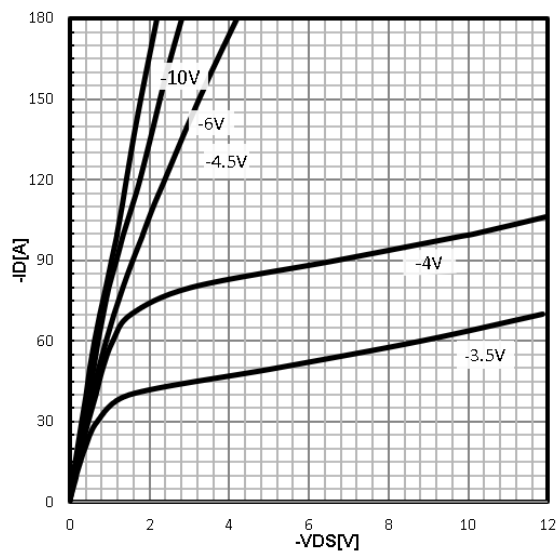
Dynamic Characteristics⁵						
Symbol	Parameter	Test Conditions	Value			Units
			Min.	Typ.	Max.	
Ciss	Input Capacitance	V _{GS} =0V V _{DS} =-30V f=1.0MHz	--	2630	--	pF
Coss	Output Capacitance		--	484	--	
Crss	Reverse Transfer Capacitance		--	9.4	--	
Rg	Gate resistance	V _{GS} =0V, V _{DS} Open	--	12.5	--	Ω

Switching Characteristics⁵						
Symbol	Parameter	Test Conditions	Value			Units
			Min.	Typ.	Max.	
td(ON)	Turn-on Delay Time	I _D =-10A, R _L =3.0Ω V _{DS} = -30V V _{GS} = -10V R _G = 3Ω	--	20	--	ns
tr	Rise Time		--	25	--	
td(OFF)	Turn-Off Delay Time		--	60	--	
Nottef :	Fall Time		--	30	--	
Qg	Total Gate Charge	V _{GS} =-10V	--	38	--	nC
Qgs	Gate Source Charge	V _{DS} =-30V	--	6.9	--	
Qgd	Gate Drain Charge	I _D =-10A	--	4.98	--	

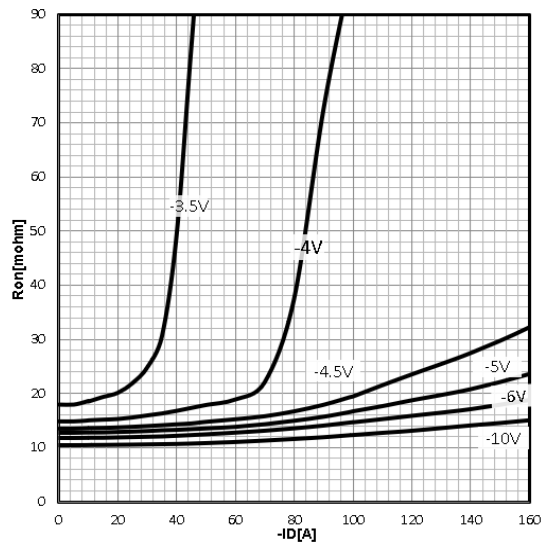
Drain- Source Body Diode Characteristics						
Symbol	Parameter	Test Conditions	Value			Units
			Min.	Typ.	Max.	
I _S	Diode Forward Current	T _C =25 °C	--	--	-60	A
V _{SD}	Diode Forward Voltage	I _S =-5.0A, V _{GS} =0V	--	--	-1.2	V
t _{rr}	Reverse Recovery time	I _S =-10A, V _{DD} =-30V dI/dt=100A/μs	--	50	--	ns
Q _{rr}	Reverse Recovery Charge		--	80	--	nC

Characteristics Curve:

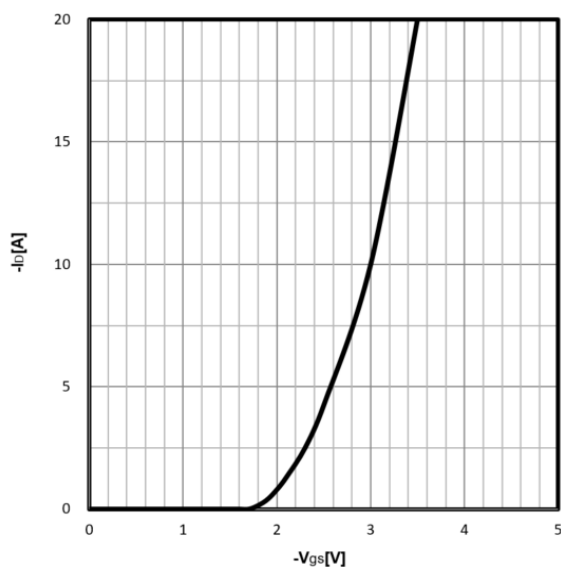
Typ. output characteristics
 $-I_D = f(-V_{DS})$



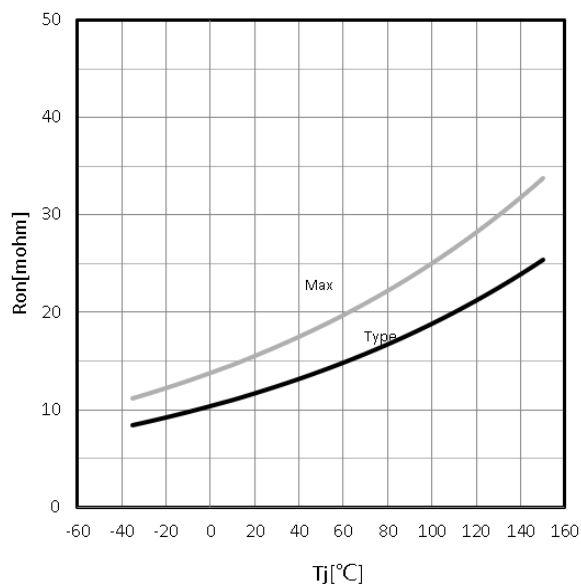
Typ. drain-source on resistance
 $R_{DS(on)} = f(-I_D)$



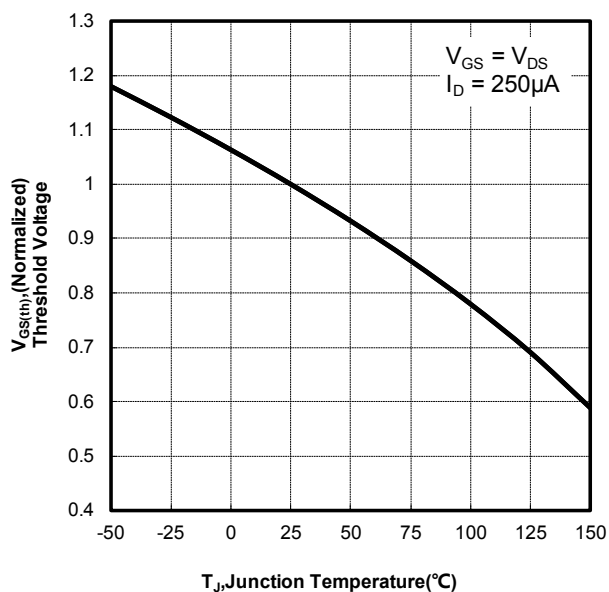
Typ. transfer characteristics
 $-I_D = f(-V_{GS})$



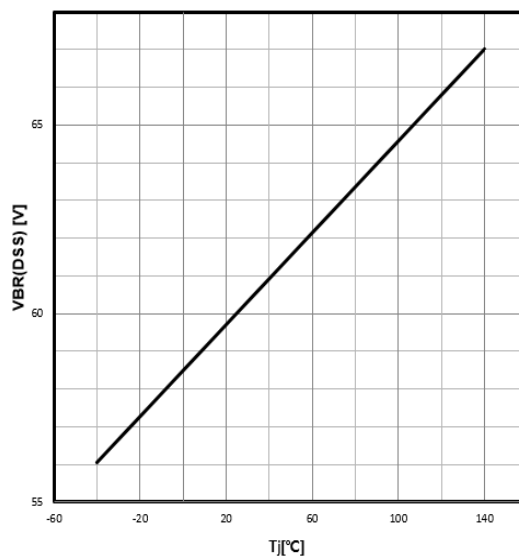
Drain-source on-state resistance
 $R_{DS(on)} = f(T_j); I_D = -20A; V_{GS} = -10V$



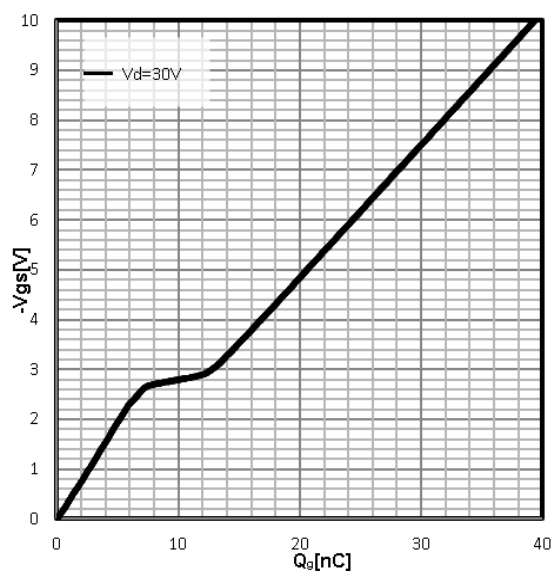
Gate Threshold Voltage
 $-V_{TH}=f(T_j)$; $I_D=-250\mu A$



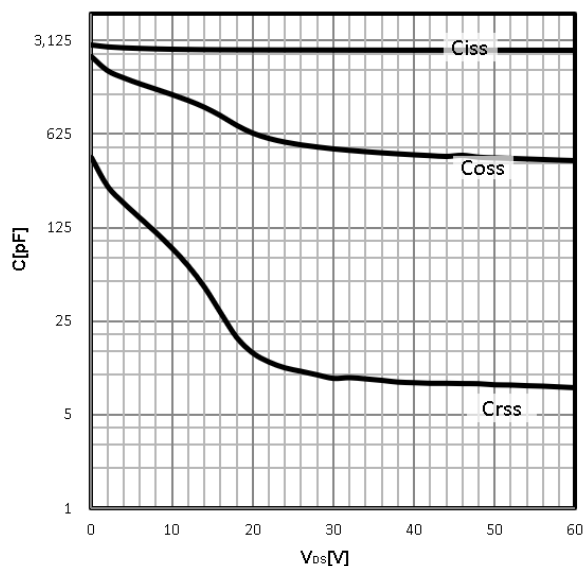
Drain-source breakdown voltage
 $-V_{BR(DSS)}=f(T_j)$; $I_D=-250\mu A$



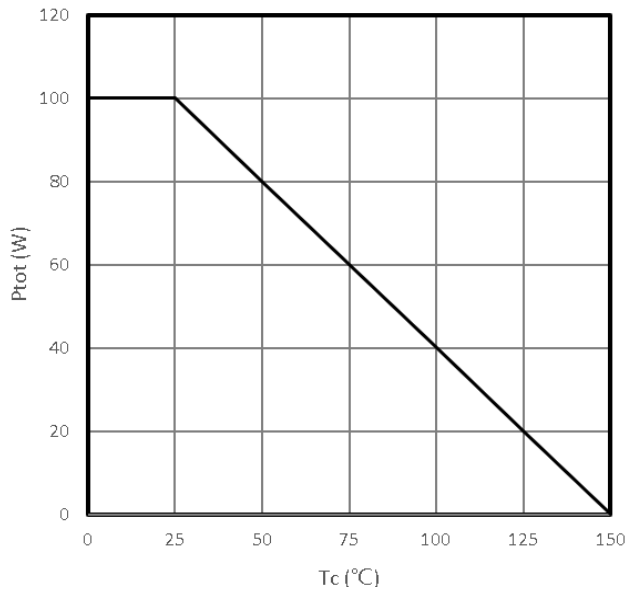
Typ. gate charge
 $V_{GS}=f(Q_{gate})$; $I_D=-10A$



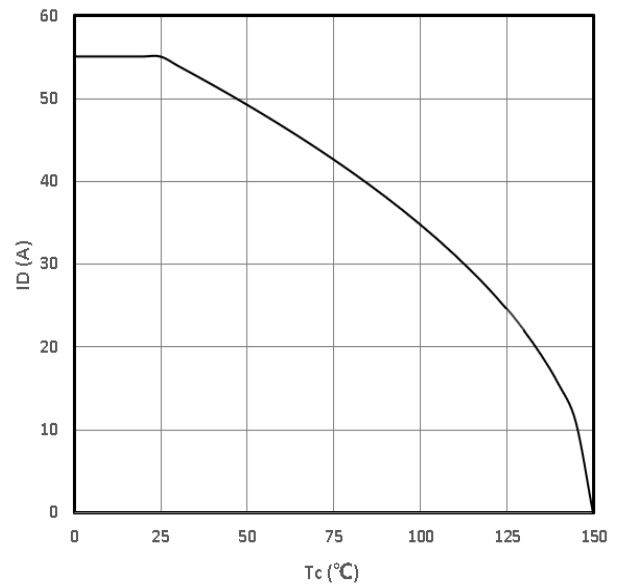
Typ. Capacitances
 $C=f(-V_{DS})$; $V_{GS}=0V$; $f=1MHz$



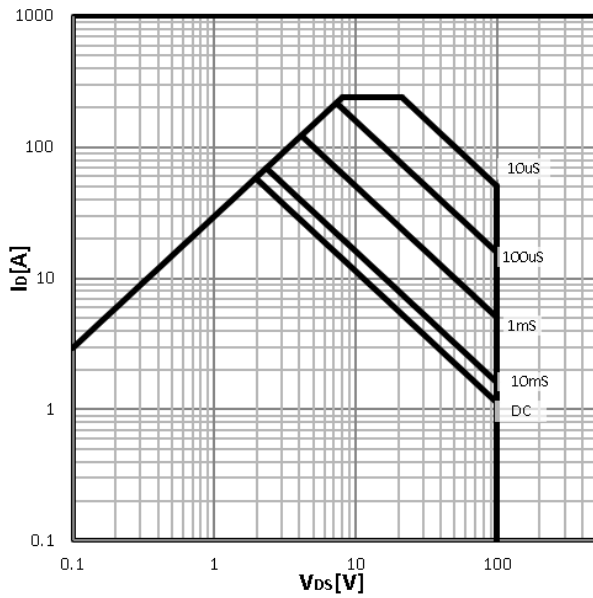
Power Dissipation
 $P_{tot}=f(T_C)$



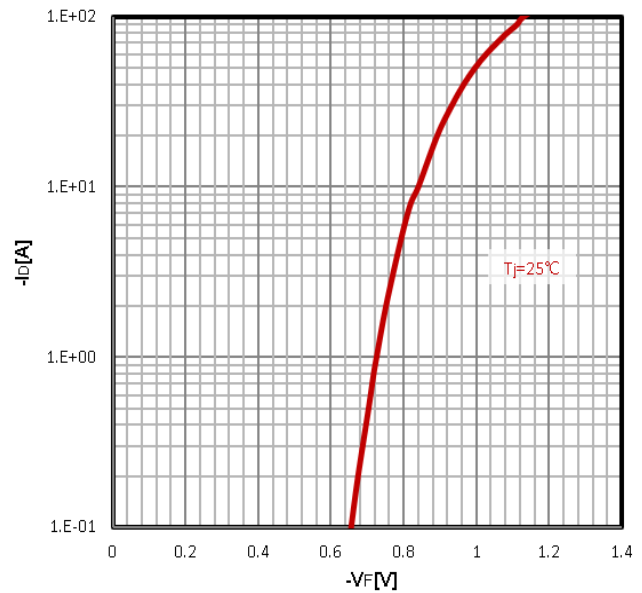
Maximum Drain Current
 $-I_D=f(T_C)$



Safe operating area
 $-I_D=f(-V_{DS})$

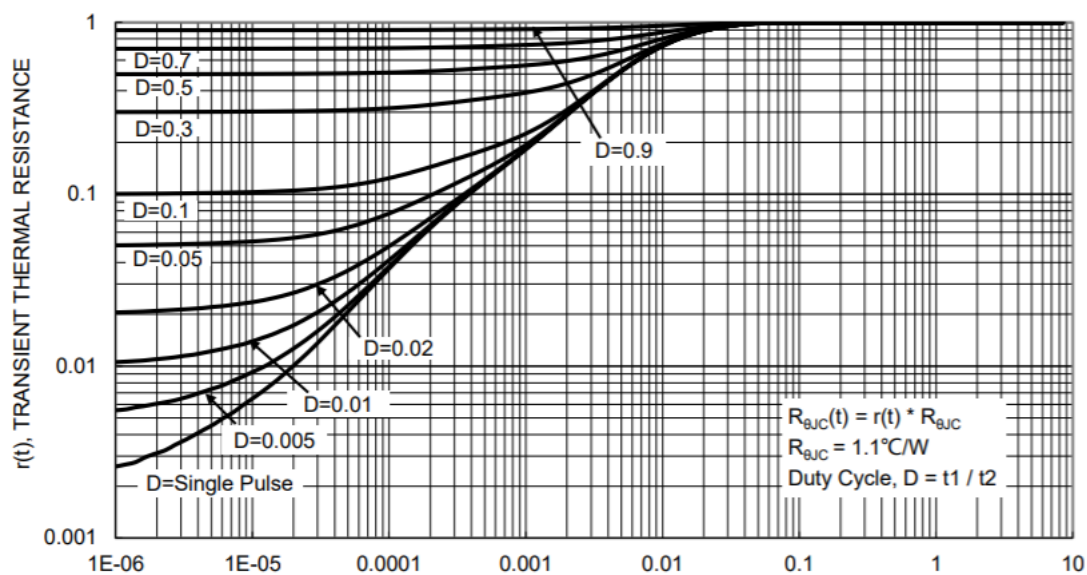


Body Diode Forward Voltage Variation
 $-I_F=f(-V_{DS})$



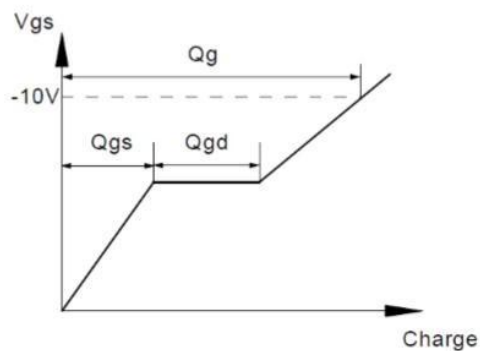
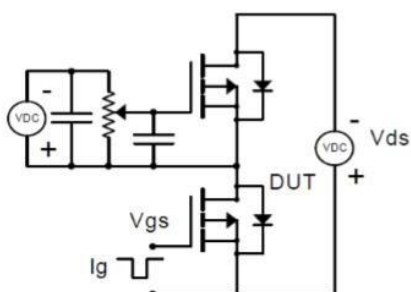
Max. transient thermal impedance

$$Z_{thJC}=f(t_p)$$

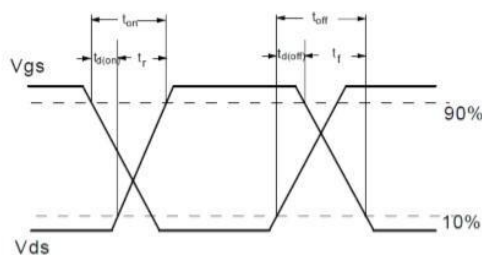
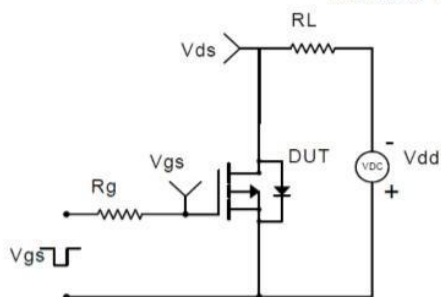


Test Circuit and Waveform:

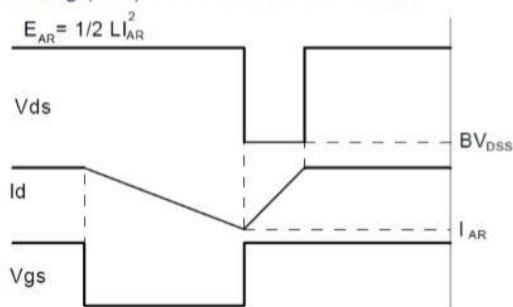
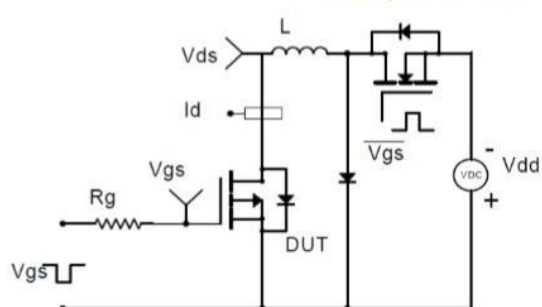
Gate Charge Test Circuit & Waveform



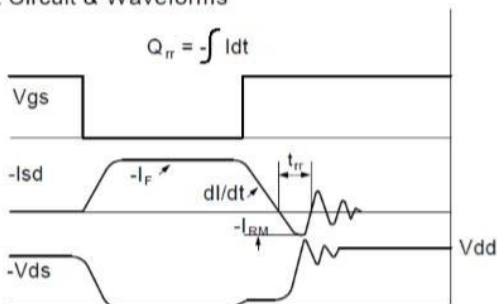
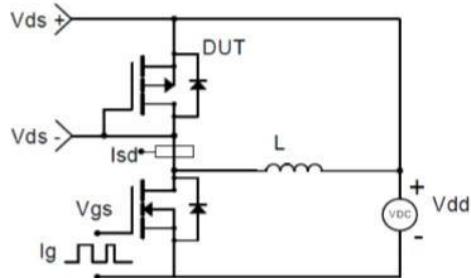
Resistive Switching Test Circuit & Waveforms



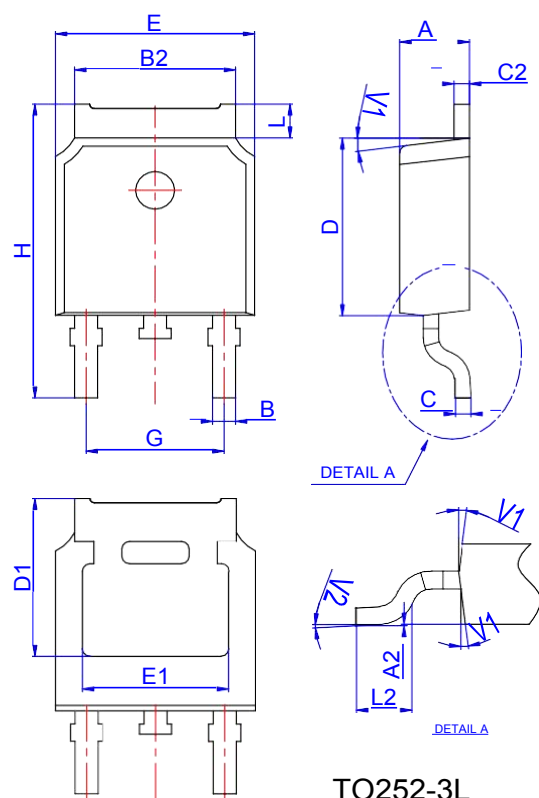
Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



Package Mechanical Data TO252-3L



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.10		2.50	0.083		0.098
A2	0		0.10	0		0.004
B	0.66		0.86	0.026		0.034
B2	5.18		5.48	0.202		0.216
C	0.40		0.60	0.016		0.024
C2	0.44		0.58	0.017		0.023
D	5.90		6.30	0.232		0.248
D1	5.30REF			0.209REF		
E	6.40		6.80	0.252		0.268
E1	4.63			0.182		
G	4.47		4.67	0.176		0.184
H	9.50		10.70	0.374		0.421
L	1.09		1.21	0.043		0.048
L2	1.35		1.65	0.053		0.065
V1		7°			7°	
V2	0°		6°	0°		6°

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