IEEE 802.3af/at, PoE Powered Device, Interface Controller

Features

- Compatible with 802.3af/at Specifications
- Support 25W PoE Power Application
- 100V, 0.48Ω Integrated Pass Switch
- 180mA Inrush Current Limit
- Current Limit During Normal Operation Between 720mA and 920mA
- Current Limit and Foldback
- Intelligent Maintain Power Signature
- Open Drain Type-2 PSE Indicator
- Self-Driving Power Good Indicator
- Over Temperature Protection (OTP)
- DFN3x3-10 Package

Application

- VoIP Telephones
- Security Camera Systems
- Remote Internet Power
- Safety Backup Power

Description

The PD provide a complete interface for a powered device (PD) to comply with the IEEE® 802.3af/at standard in a power-over-Ethernet system. The PD with a detection signature, classification signature, and an integrated isolation power switch with inrush current control. During the inrush period, the PD limit the current to less than 180mA before switching to the higher current limit (720mA to 920mA) when the isolation power MOSFET is fully enhanced. The devices feature an input UVLO with wide hysteresis and long deglitch time to compensate for twisted-pair cable resistive drop and to assure glitch-free transition during power-on/-off conditions. The PD can withstand up to 100V at the input. The PD support a 2-event classification method as specified in the IEEE 02.3at standard and provide a signal to indicate when probed by Type 2 power-sourcing equipment (PSE). A PG signal set to high indicates when the output is fully charged and pulls low when the output drops under the overload condition .The devices detect the presence of a wall adapter power-source connection and allow a smooth switchover from the PoE power source to the wall power adapter. The intelligent MPS function enables applications requiring very low power standby modes.

The TMI7303D is available in DFN3x3-10 package with exposed pad for low thermal resistance.

Typical Application

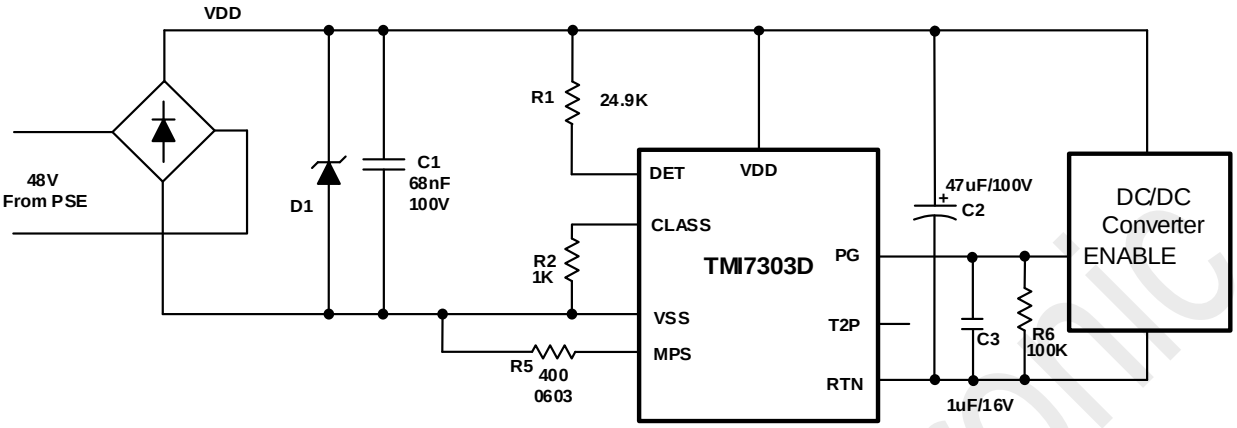


Figure 1. TMI7303D Typical Application Circuit

Absolute Maximum Ratings (Note 1)

Items	Min	Max	Unit
VDD, RTN, DET, T2P, to VSS	-0.3	100	V
CLASS, MPS to VSS	-0.3	5.5	V
PG to RTN	-0.3	5.5	V
T2P sink current	10		mA
Continuous Power Dissipation (T_A = +25°C) (Note2)	2.5		W
Junction Temperature	150		°C
Lead Temperature	260		°C
Storage Temperature	-65	150	°C

Recommended Operating Conditions (Note 3)

Items	Min	Max	Unit
Supply Voltage VDD	0	57	V
Maximum T2P Current		5	mA
Operating Junction Temp	-40	125	°C

Thermal Resistance

Items	Description	Value	Unit
θ_{JA}	Junction-to-ambient thermal resistance	50	°C/W
θ_{JC}	Junction-to-case(top) thermal resistance	12	°C/W

ESD Ratings

Items	Description	Value	Unit
$V_{(ESD-HBM)}$	Human Body Model (HBM) ANSI/ESDA/JEDEC JS-001-2017 Classification, Class: 2	±2000	V
$V_{(ESD-CDM)}$	Charged Device Mode (CDM) ANSI/ESDA/JEDEC JS-002-2018 Classification, Class: C3	±1000	V
$I_{LATCH-UP}$	JEDEC STANDARD NO.78E APRIL 2016 Temperature Classification, Class: I	±200	mA

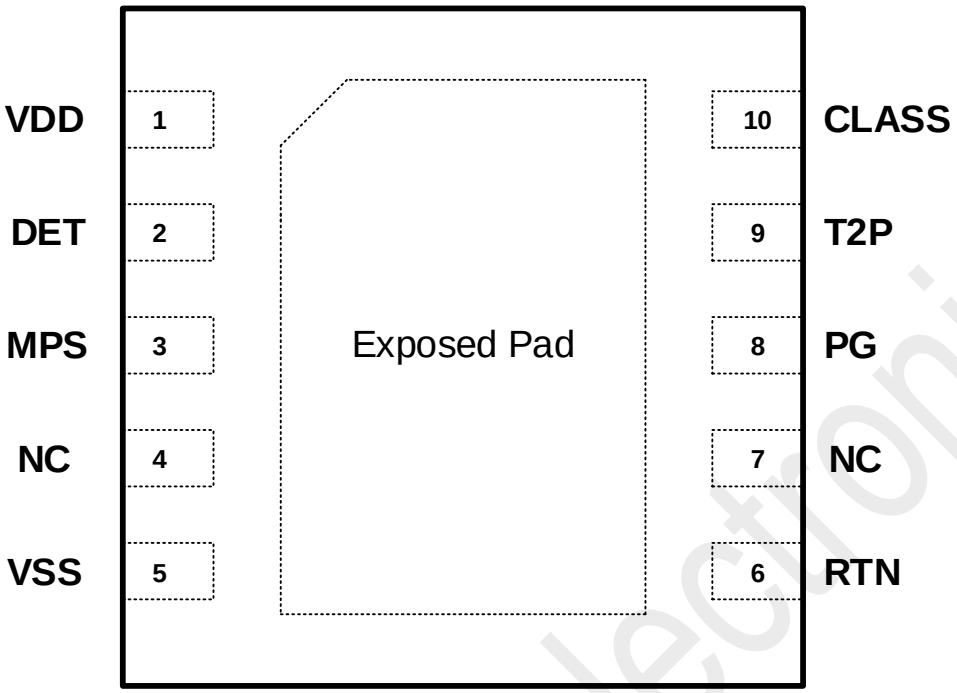
JEDEC specification JS-001

Note 1: Exceeding these ratings may damage the device.

Note 2: The maximum allowable power dissipation is a function of the maximum junction temperature $T_{J(MAX)}$, the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_{D(MAX)}=(T_{J\ (MAX)}-T_A)/\theta_{JA}$. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.

Note 3: The device is not guaranteed to function outside of its operating conditions.

Package



DFN3x3-10

Top Marking: T7303D/XXXXX (T7303D: Device Code, XXXXX: Inside Code)

Order Information

Part Number	Package	Top Marking	Quantity/ Reel
TMI7303D	DFN3x3-10	T7303D XXXXX	5000

TMI7303D devices are Pb-free and RoHS compliant.

Pin Functions

Pin	Name	Function
1	VDD	Positive Power Supply.
2	DET	Detection Resistor Input. Connect a signature resistor (RDET = 24.9kΩ) from DET to VDD.
3	MPS	Open drain output. work as MPS switch to generate current pulses by connecting a resistor between MPS and VSS. The high level of MPS pulse is 5V.
4	NC	Not connected internally.
5	VSS	Negative Power Supply Terminal from PoE input power rail.
6	RTN	Drain of Isolation MOSFET. RTN connects to the drain of the integrated isolation n-channel power MOSFET. Connect RTN to the downstream DC/DC converter ground as shown in the Typical Application Circuit.
7	NC	Not connected internally.
8	PG	PD supply power good indicator. This signal will enable the DCDC converter. It is pulled up by internal current source in output high condition, Connect PG to RTN through a resistor.
9	T2P	Type 2 PSE indicator, open-drain output. Pull low to VSS indicates the presence of a Type 2 PSE.
10	CLASS	Connect resistor from CLASS to VSS to program classification current.
11	Exposed Pad	Exposed Pad. Do not use exposed pad as an electrical connection to VSS. Exposed pad is internally connected to VSS through a resistive path and must be connected to VSS externally. To optimize power dissipation, solder the exposed pad to a large copper power plane.

Electrical Characteristics

V_{DD}-V_{SS}=48V, all voltages with respect to VSS, R_{DET}=24.9kΩ, R_{CLASS}=1000Ω, T_A=25ºC, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Detection						
Detection on	V_{DET_ON}	V_{VDD} Rising		1.4		V
Detection off	V_{DET_OFF}	V_{VDD} Rising		12		V
DET Leakage Current	V_{DET_LK}	V_{DET}=V_{VDD}=57V, Measure IDET		0.1	5	μA
Bias Current		V_{VDD}=10.1V, float DET pin, not in Mark event, Measure I_{SUPPLY}			12	μA
Detection Current	I_{DET}	V_{VDD} =2.5V, Measure I_{SUPPLY}	96	99	102	μA
		V_{VDD} =10.1V, Measure I_{SUPPLY}	395	410	425	μA
Classification						
Classification Stability Time				120		μs
VCLASS Output Voltage	V_{CLASS}	13V< V_{VDD} <21V, 1mA<I_{CLASS} <42mA	1.12	1.18	1.24	V
Classification Current	I_{CLASS}	13≤V_{VDD}≤21V, Guaranteed by V_{CLASS}				
		R_{CLASS}=1000Ω, 13≤V_{VDD}≤21V	1	1.2	2.8	mA
		R_{CLASS}=113Ω, 13≤V_{VDD}≤21V	10.3	10.5	11.3	
		R_{CLASS}=64.9Ω, 13≤V_{VDD}≤21V	17.7	18.2	19.5	
		R_{CLASS}=42.2Ω, 13≤V_{VDD}≤21V	27.1	28	29.5	
		R_{CLASS}=30Ω, 13≤V_{VDD}≤21V	36.4	39.4	43.6	
Classification Lower Threshold	V_{CL_ON}	Class Regulator Turns on, V_{VDD} Rising	11	12	13	V
Classification Upper Threshold	V_{CL_OFF}	Class Regulator Turns off, V_{VDD} Rising	21	22	23	V
Classification Hysteresis	V_{CL_HYS}	Low side Hysteresis		1		V
		High side Hysteresis		0.8		
Mark Event Rest Threshold	V_{MARK-L}		2.8	4	5.2	V
Max Mark Event Voltage	V_{MARK-H}		10.1	11	12	V
Mark Event Current	I_{MARK}		0.25		0.85	mA
IC Supply Current during Classification	I_{IN_CLASS}	V_{VDD} =17.5V, CLASS Floating		200	300	μA
PD UVLO						
VDD Turn on Threshold	$V_{VDD\_VSS\_R}$	V_{VDD} Rising	36	37.8	39.6	V
VDD Turn off Threshold	$V_{VDD\_VSS\_F}$	V_{VDD} Falling	30	31	32	V
VDD UVLO Hysteresis	$V_{VDD\_VSS\_HYS}$			7.6		V
IC Supply Current during Operation	I_{IN}			300	450	μA

Electrical Characteristics

V_{DD}-V_{SS}=48V, all voltages with respect to VSS, R_{DET}=24.9kΩ, R_{CLASS}=1000Ω, T_A=25ºC, unless otherwise noted.

Pass Device and Current Limit						
On Resistance	$R_{DS(ON)}$	I_{RTN}=600mA		0.48		Ω
Leakage Current	I_{RTN_LK}	V_{VDD}=V_{RTN}=57V		1	15	μA
Current Limit	I_{LIMIT}	V_{RTN}=1V	720	840	920	mA
Inrush Limit	I_{INRUSH}	V_{RTN}=2V		180		mA
Inrush Termination Current		I_{RTN} Falling Percentage of inrush current		88%		
Inrush to Operation Mode Delay	T_{DELAY}		80	96		ms
Current Fold-back Threshold		V_{RTN} Rising		12		V
MPS						
Intelligent MPS falling current threshold	I_{MPS_TH}	Startup has completed, I_{RTN} falling threshold to generate MPS pulses		22		mA
	I_{MPS_HYS}	Hysteresis on RTN current		3		mA
The high level of MPS pulse	V_{MPS}	I_{RTN}<I_{MSTH}	4	4.5	5	V
MPS pulsed mode duty cycle		MPS pulsed current ON time	75	80	85	ms
		MPS pulsed current OFF time	225	240	255	ms
		MPS pulsed current duty cycle	24.7%	25%	25.3%	
T2P						
T2P Output Low Voltage		I_{T2P}=2mA, respect to VSS		0.1	0.3	V
T2P Output High Leakage Current		V_{T2P}=48V			1	μA
PG						
Source Current Capability		PG is logic high, pull PG pin to 0V		30		μA
PG Pull Down Resistance		PG is logic low, pull up PG pin to 1V		1000		kΩ
PD Thermal Shutdown						
Thermal Shut down Temperature (Note 1)	T_{PD-SD}			150		ºC
Thermal Shut down Hysteresis (Note 1)	T_{PD-HYS}			20		ºC

Note 1: Guaranteed by design.

Block Diagram

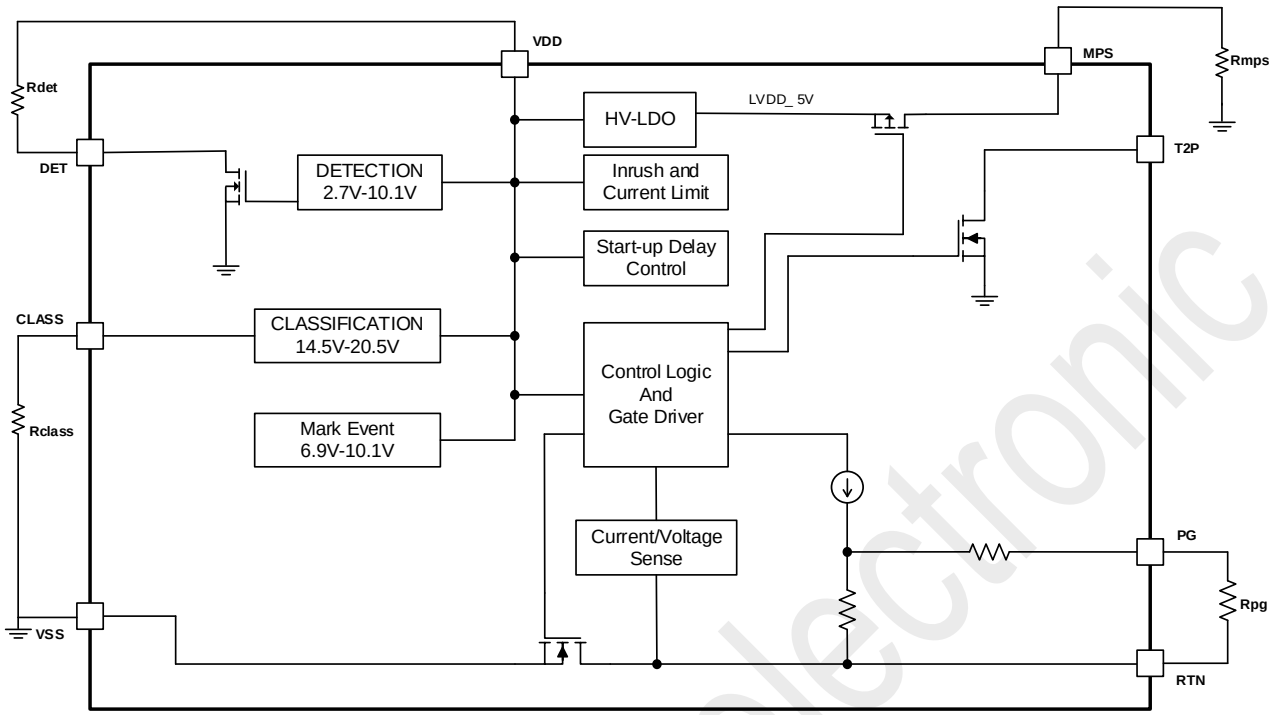


Figure 2 TMI7303D Block Diagram

Operation Description

Operation

Depending on the input voltage (VIN = VDD - VSS), the TMI7303D operate in four different modes: PD detection, PD classification, mark event, and PD power. The devices enter PD detection mode when the input voltage is between 1.4V and 10.1V. The device enters PD classification mode when the input voltage is between 12V and 20V. The device enters PD power mode once the input voltage exceeds VON. Figure 3 shows the function diagram of this device.

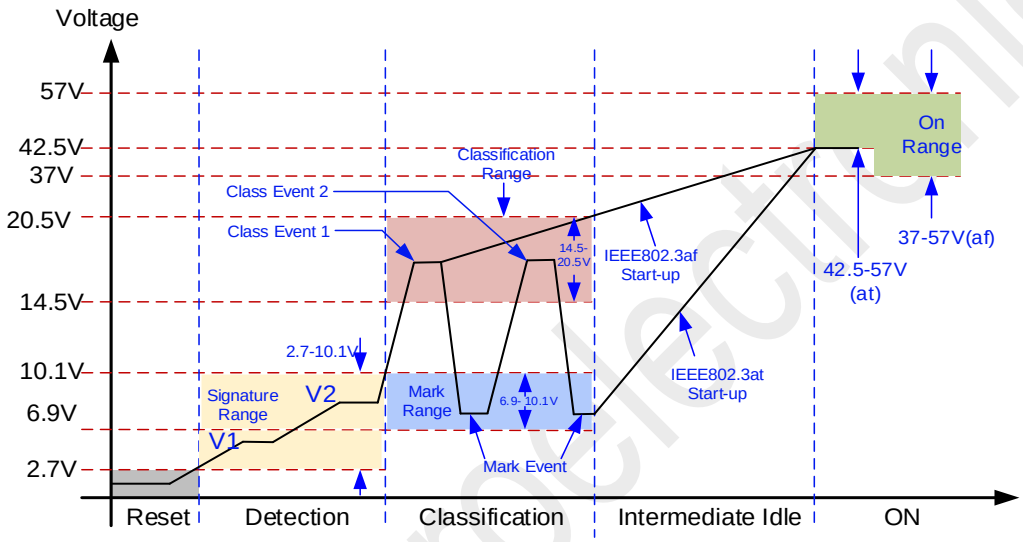


Figure 3 PD Interface Operation Description

Detection Mode(1.4V≤VDD≤10.1V)

In detection mode, the PSE applies two voltages on VDD in the range of 1.4V to 10.1V (1V step minimum) and then records the current measurements at the two points. The PSE then computes ΔV/ΔI to ensure the presence of the 24.9kΩ signature resistor. Connect the signature resistor (R_{DET}) from VDD to DET for proper signature detection. The TMI7303D pull DET low in detection mode. DET goes high impedance when the input voltage exceeds 12.5V. In detection mode, most of the TMI7303D internal circuitry is off and the offset current is less than 10μA.

If the voltage applied to the PD is reversed, install protection diodes at the input terminal to prevent internal damage to the TMI7303D (see the Typical Application Circuit). Since the PSE uses a slope technique (ΔV/ΔI) to calculate the signature resistance, the DC offset due to the protection diodes is ubtracted and does not affect the detection process.

Classification Mode(12.6V≤VDD≤20V)

In the classification mode, the PSE classifies the PD based on the power consumption required by the PD. This allows the PSE to efficiently manage power distribution. Class 0 to 4 is defined as shown in Table 1. An external resistor (R_{CLS}) connected from CLS to VSS sets the classification current. The PSE determines the class of a PD by applying a voltage at the PD input and measuring the current sourced out of the PSE. When the PSE applies a voltage between 12.1V and 20V, the TMI7303D exhibit a current characteristic with a value shown in Table 1. The PSE uses the classification current information to classify the power requirement of the PD. The classification current includes the current drawn by RCLS and the supply current of the TMI7303D so the total current drawn by the PD is within the IEEE 802.3af/at standard figures. The classification current is turned off whenever the device is in power mode.

Table 1. CLASS Resistor Selection

Class	Max. Input Power to PD(W)	Classification Current(mA)	R_{CLASS}(Ω)
0	12.95	1.2	1000
1	3.84	10.5	113
2	6.49	18.2	64.9
3	12.95	28	42.2
4	25.5	39.4	30

2-Event Classification and Detection

During 2-event classification, a Type 2 PSE probes PD for classification event, the PSE presents an input voltage between 12.6V and 20V, and the TMI7303D presents the programmed load I_{CLASS}. Then, the PSE drops the probing voltage below the mark event threshold of 10.1V and the devices present the mark current. This sequence is repeated one more time. When the TMI7303D is powered by a Type 2 PSE, the 2-event identification output T2P asserts low after the internal isolation n-channel MOSFET is fully turned on. T2P is turned off when VDD goes below the UVLO threshold (V_{OFF}) and turns on when VDD goes above the UVLO threshold (V_{ON}), unless VDD goes below V_{THR} to reset the latched output of the Type 2 PSE detection flag.

PD Interface UVLO and Current Limit

When PD is powered by PSE and VDD is higher than turn on threshold, the hot-swap switch will start pass a limited current I_{INRUSH} to charge the downstream DC/DC converter's input capacitor C_{BULK}. The startup charging current is around 180mA. Once the inrush current falls about 20% below the inrush current limit, the hot-swap current limit will change to 840mA. After the t_{DELAY} from UVLO starting, TMI7303D will assert PG signal and go from the startup mode to the running mode if inrush period elapse, the PG signal can enable down-stream DCDC converter internally.

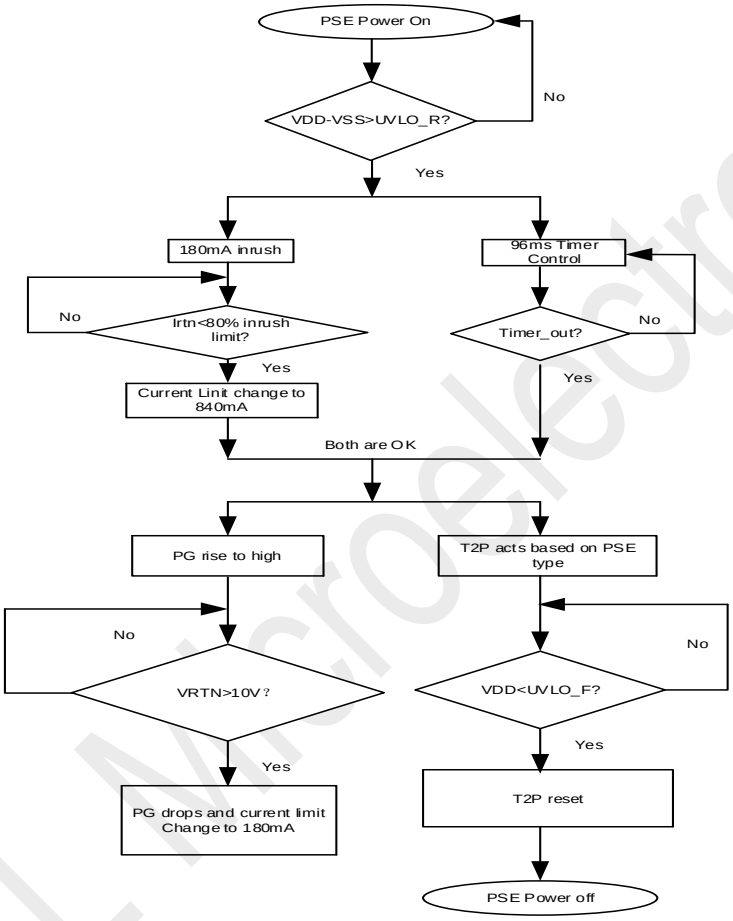


Figure 4 Startup Sequence

If VDD-VSS drops below falling UVLO, the hot-swap MOSFET and DC/DC converter both are disabled. If output current overloads on the internal pass MOSFET, current limit works and V_{RTN}-VSS rises. If V_{RTN} rises above 10V the current limit reverts to the inrush value, and PG is pulled down internally to disable DCDC regulator at the same time. Figure 4 shows the current limit, PG and T2P work logic during startup from PSE power supply.

Power Good Indicator (PG)

The PG signal is driven by internal current source. After T_{DELAY} from UVLO starting and the inrush current falls about 20% below the inrush current limit, the PG signal will be pulled high to indicate power condition and enable the downstream DCDC converter.

Maintain Power Signature (MPS)

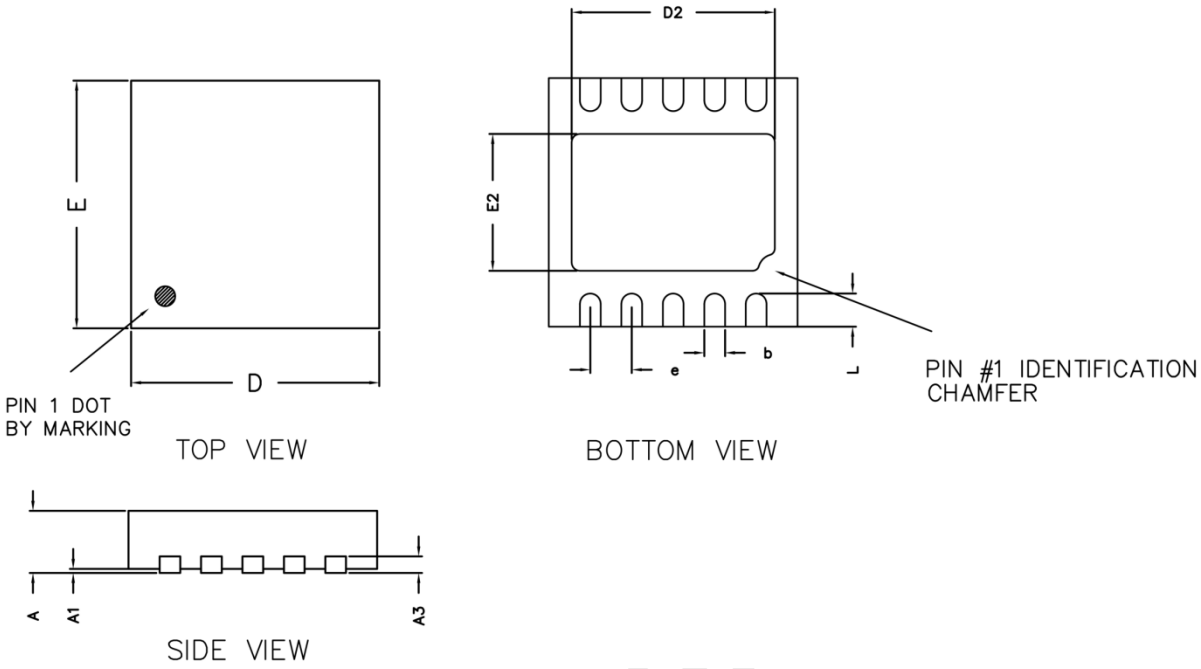
The MPS is an electrical signature presented by the PD to assure the PSE that it is still present after operating voltage is applied. For IEEE802.3af/at PD, a valid MPS consists of a minimum dc current of 10mA, or a 10mA pulsed current for at least 75ms every 325ms, and an AC impedance lower than 26.3kΩ in parallel with 0.05μF. If the current through the RTN-to-VSS path is below ~22mA, the TMI7303D automatically generates the MPS pulsed current through the MPS output pin, the current amplitude being adjustable with an external resistor. The high level MPS pulse is 5V.

Thermal Shutdown

The TMI7303D has a temperature protection circuit. When the junction temperature exceeds 150ºC the device shuts down. The device recovers with limited inrush current if the junction temperature drops below 130ºC.

Package Information

DFN3x3-10

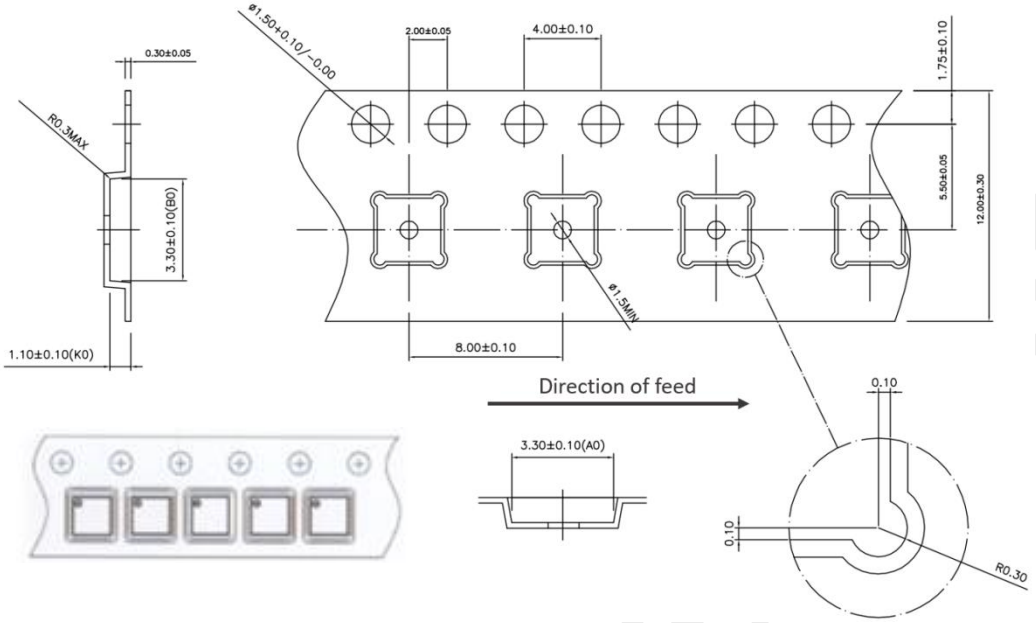


Unit: mm

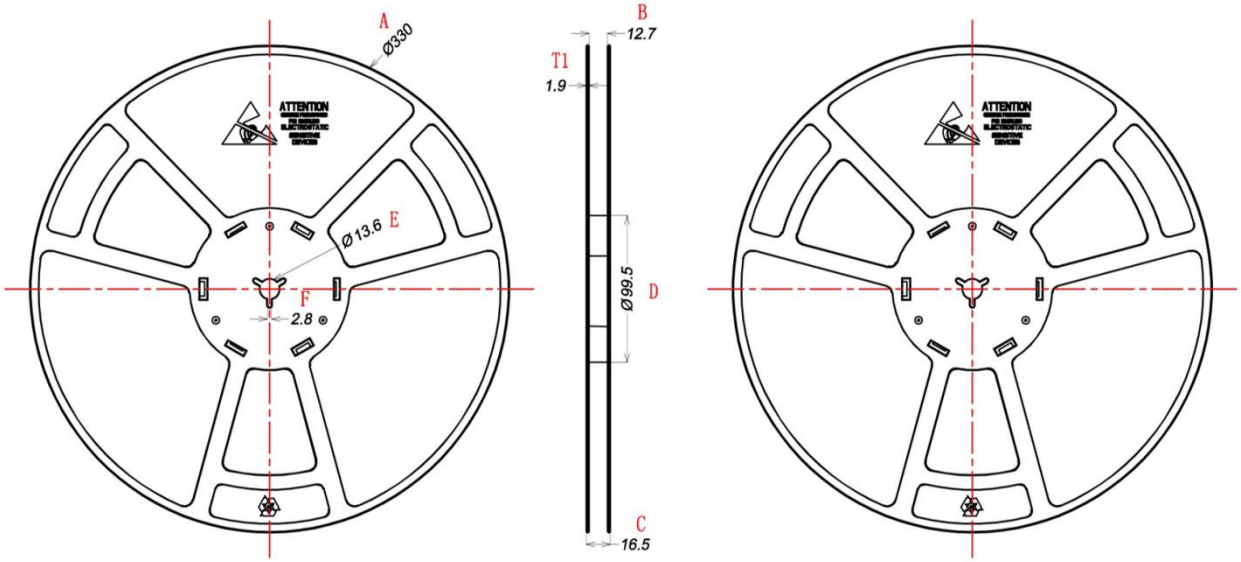
Symbol	Dimensions In Millimeters			Symbol	Dimensions In Millimeters		
	Min	Nom	Max		Min	Nom	Max
A	0.70	0.75	0.80	b	0.20	0.25	0.3
A1	0.00	-	0.05	L	0.30	0.40	0.50
A3	0.2 REF			D2	2.30	2.40	2.50
D	2.95	3.00	3.05	E2	1.50	1.65	1.75
E	2.95	3.00	3.05	e	0.50 BSC		

Tape And Reel Information

TAPE DIMENSIONS:



REEL DIMENSIONS:



Unit: mm

A	B	C	D	E	F	T1
Ø 330±1	12.7±0.5	16.5±0.3	Ø 99.5±0.5	Ø 13.6±0.2	2.8±0.2	1.9±0.2

Note:

1) All Dimensions are in Millimeter
2) Quantity of Units per Reel is 5000
3) MSL level is level 3.

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