

1. Product profile

1.1 General description

A 100 W LDMOS RF power push-pull transistor for broadcast transmitter and industrial applications. The transistor is suitable for the frequency range HF to 1400 MHz. The excellent ruggedness and broadband performance of this device makes it ideal for digital applications.

Table 1. Typical performance

RF performance at $T_h = 25\text{ °C}$ in a common source test circuit.

Mode of operation	f (MHz)	V _{DS} (V)	P _L (W)	P _{L(PEP)} (W)	G _p (dB)	η _D (%)	IMD (dBc)
CW, class-AB	1300	32	100	-	18	56	-
2-tone, class-AB	1300	32	-	100	18	45	-32

1.2 Features

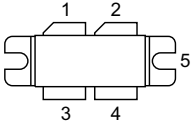
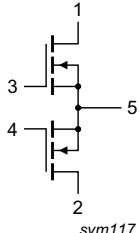
- CW performance at 1300 MHz, a drain-source voltage V_{DS} of 32 V and a quiescent drain current I_{Dq} = 0.9 A for total device:
 - ◆ Average output power = 100 W
 - ◆ Power gain = 18 dB
 - ◆ Drain efficiency = 56 %
- 2-tone performance at 1300 MHz, a drain-source voltage V_{DS} of 32 V and a quiescent drain current I_{Dq} = 0.9 A for total device:
 - ◆ Peak envelope load power = 100 W
 - ◆ Power gain = 18 dB
 - ◆ Drain efficiency = 45 %
 - ◆ Intermodulation distortion = -32 dBc
- Integrated ESD protection
- Excellent ruggedness
- High power gain
- High efficiency
- Excellent reliability
- Easy power control
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

1.3 Applications

- Communication transmitter applications in the HF to 1400 MHz frequency range
- Industrial applications in the HF to 1400 MHz frequency range

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	drain 1		
2	drain 2		
3	gate 1		
4	gate2		
5	source		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLF645	-	flanged balanced LDMOST ceramic package; 2 mounting holes; 4 leads	SOT540A

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
V_{GS}	gate-source voltage		-0.5	+11	V
I_D	drain current		-	32	A
T_{stg}	storage temperature		-65	+150	°C
T_j	junction temperature		-	200	°C

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	$T_{case} = 80\text{ °C}$; $P_L = 100\text{ W}$	[1]	0.67 K/W

[1] $R_{th(j-c)}$ is measured under RF conditions.

6. Characteristics

Table 6. Characteristics per section

$T_j = 25\text{ }^{\circ}\text{C}$ per section; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0\text{ V}; I_D = 0.9\text{ mA}$	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$V_{DS} = 32\text{ V}; I_D = 90\text{ mA}$	1.4	1.9	2.4	V
V_{GSq}	gate-source quiescent voltage	$V_{DS} = 32\text{ V}; I_{Dq} = 450\text{ mA}$	1.5	2.0	2.5	V
I_{DSS}	drain leakage current	$V_{GS} = 0\text{ V}; V_{DS} = 32\text{ V}$	-	-	1.4	μA
I_{DSX}	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75\text{ V};$ $V_{DS} = 10\text{ V}$	-	14	-	A
I_{GSS}	gate leakage current	$V_{GS} = \pm 10\text{ V}; V_{DS} = 0\text{ V}$	-	-	120	nA
g_{fs}	forward transconductance	$V_{DS} = 10\text{ V}; I_D = 4.5\text{ A}$	-	6.4	-	S
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75\text{ V};$ $I_D = 3.15\text{ A}$	-	220	-	$\text{m}\Omega$
C_{iss}	input capacitance	$V_{GS} = 0\text{ V}; V_{DS} = 32\text{ V};$ $f = 1\text{ MHz}$	-	69	-	pF
C_{oss}	output capacitance	$V_{GS} = 0\text{ V}; V_{DS} = 32\text{ V};$ $f = 1\text{ MHz}$	-	25	-	pF
C_{rs}	feedback capacitance	$V_{GS} = 0\text{ V}; V_{DS} = 32\text{ V};$ $f = 1\text{ MHz}$	-	1.2	-	pF

7. Application information

Table 7. RF performance in a common-source class-AB circuit

$T_h = 25\text{ }^{\circ}\text{C}; I_{Dq} = 0.9\text{ A}$ for total device.

Mode of operation	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)
CW, class-AB	1300	32	100	> 16.5	> 53

7.1 Ruggedness in class-AB operation

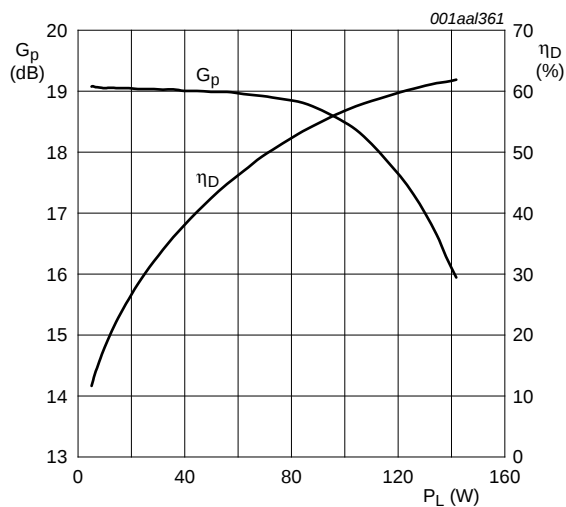
The BLF645 is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: $V_{DS} = 32\text{ V}; f = 1300\text{ MHz}$ at rated load power.

8. Test information

8.1 RF performance

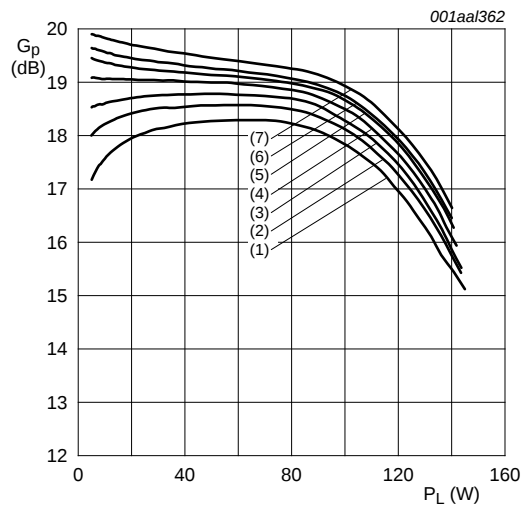
The following figures are measured in a class-AB production test circuit.

8.1.1 1-Tone CW



$V_{DS} = 32$ V; $I_{Dq} = 900$ mA (for total device);
 $f = 1300$ MHz.

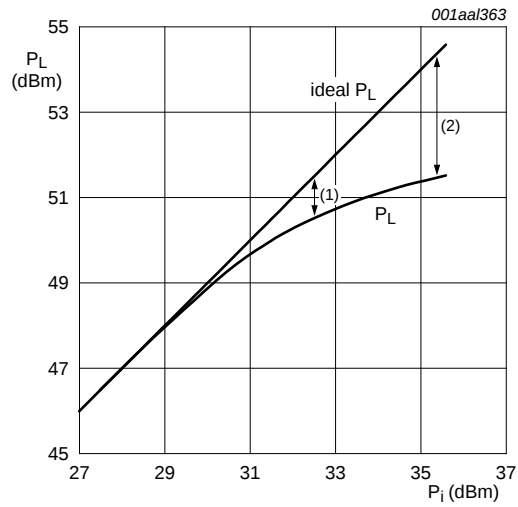
Fig 1. Power gain and drain efficiency as function of load power; typical values



$V_{DS} = 32$ V; $f = 1300$ MHz.

- (1) $I_{Dq} = 200$ mA (for total device).
- (2) $I_{Dq} = 400$ mA (for total device).
- (3) $I_{Dq} = 600$ mA (for total device).
- (4) $I_{Dq} = 900$ mA (for total device).
- (5) $I_{Dq} = 1200$ mA (for total device).
- (6) $I_{Dq} = 1400$ mA (for total device).
- (7) $I_{Dq} = 1800$ mA (for total device).

Fig 2. Power gain as a function of load power; typical values



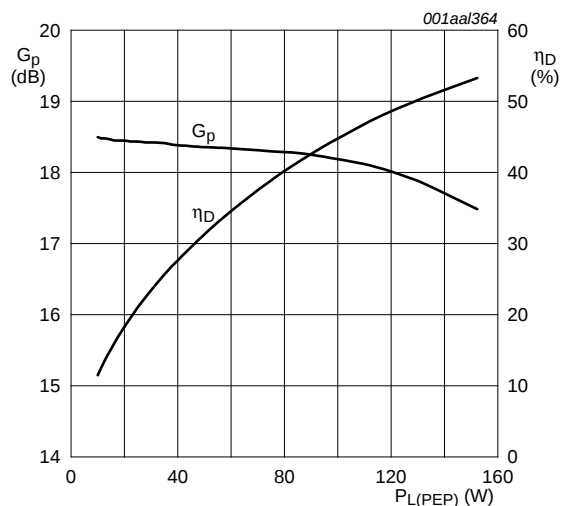
$V_{DS} = 32$ V; $I_{Dq} = 900$ mA (for total device); $f = 1300$ MHz.

(1) $P_{L(1dB)} = 50.5$ dBm (112 W).

(2) $P_{L(3dB)} = 51.5$ dBm (141 W).

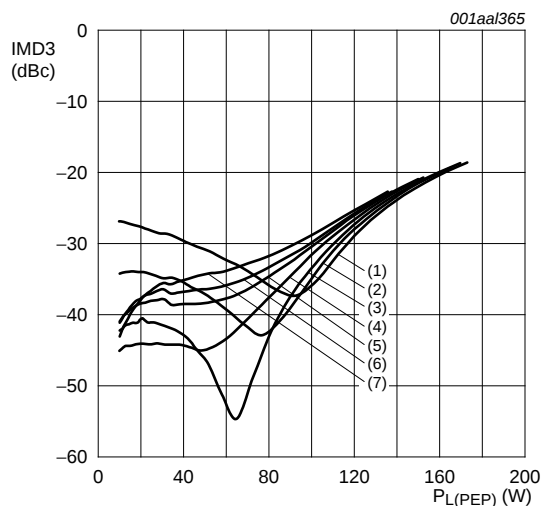
Fig 3. Load power as function of input power; typical values

8.1.2 2-Tone CW



$V_{DS} = 32$ V; $I_{Dq} = 900$ mA (for total device);
 $f = 1300$ MHz; carrier spacing = 100 kHz.

Fig 4. Power gain and drain efficiency as function of peak envelope load power; typical values

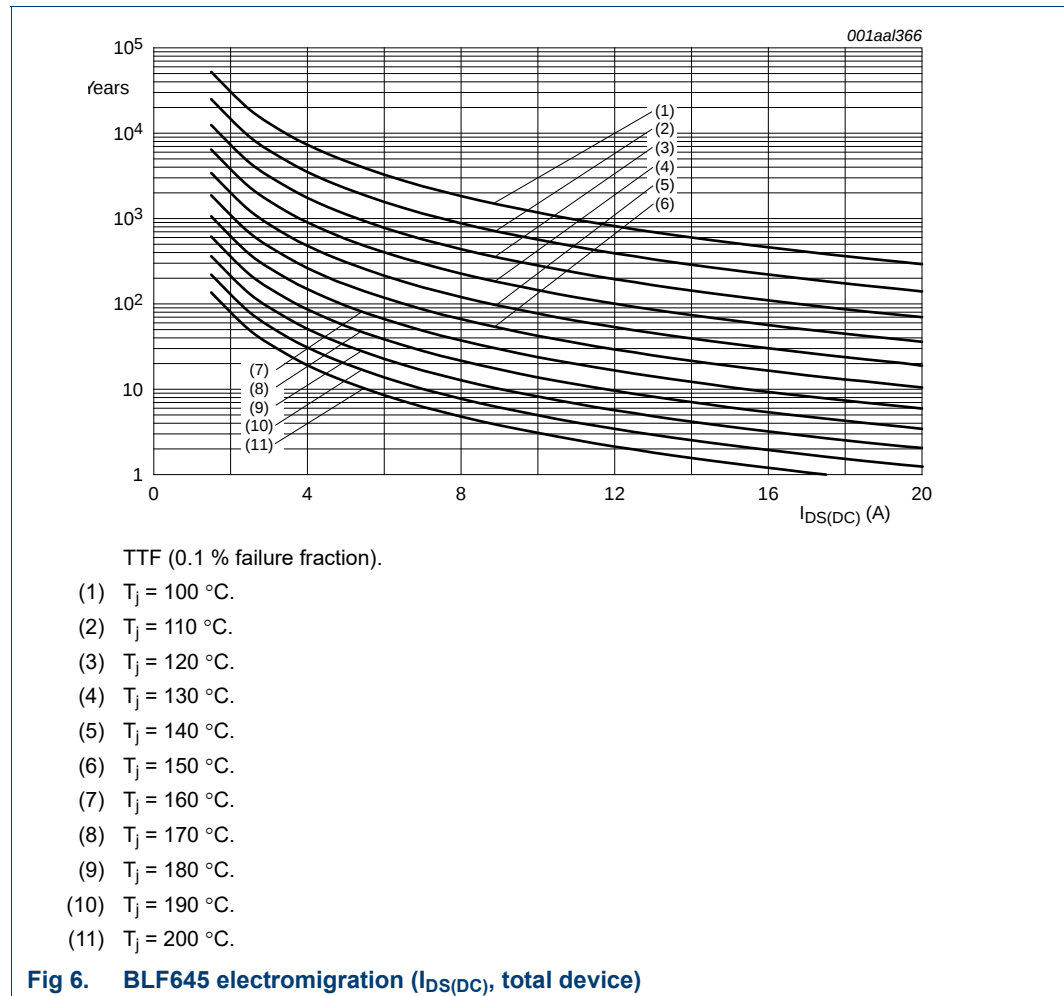


$V_{DS} = 32$ V; $f = 1300$ MHz; carrier spacing = 100 kHz.

- (1) $I_{Dq} = 200$ mA (for total device).
- (2) $I_{Dq} = 400$ mA (for total device).
- (3) $I_{Dq} = 600$ mA (for total device).
- (4) $I_{Dq} = 900$ mA (for total device).
- (5) $I_{Dq} = 1200$ mA (for total device).
- (6) $I_{Dq} = 1400$ mA (for total device).
- (7) $I_{Dq} = 1800$ mA (for total device).

Fig 5. Third order intermodulation distortion as a function of peak envelope load power; typical values

8.2 Reliability



8.3 Test circuit

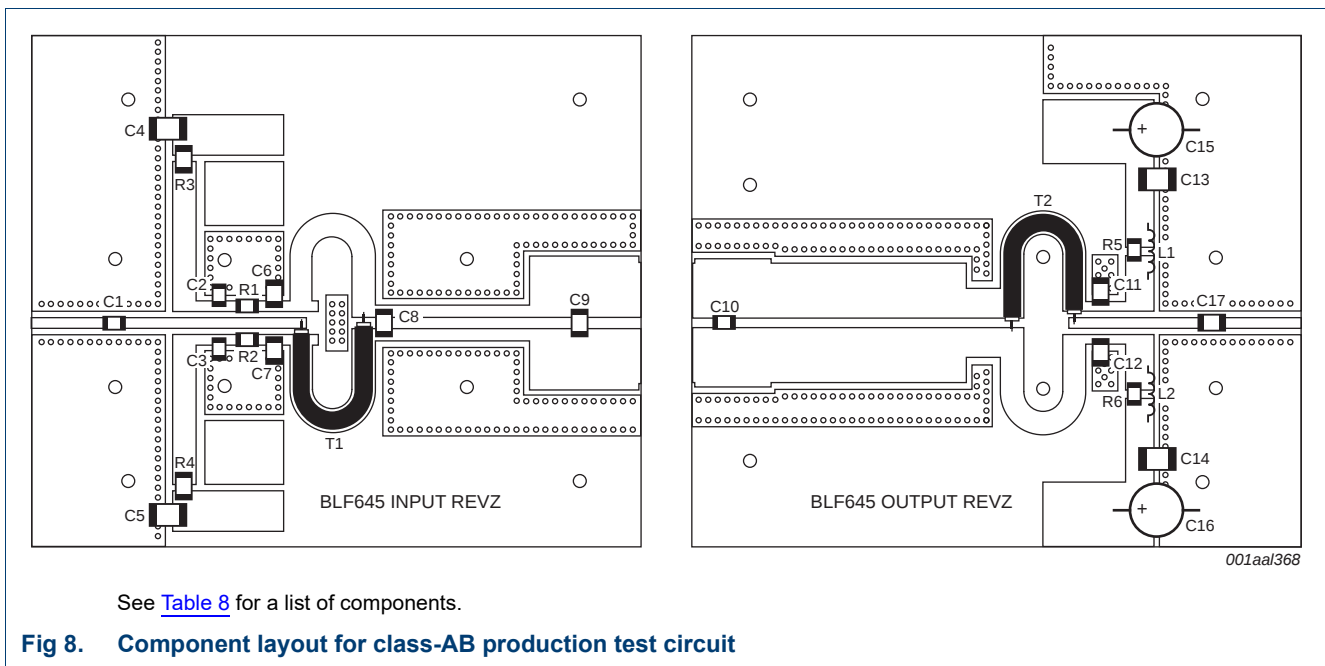
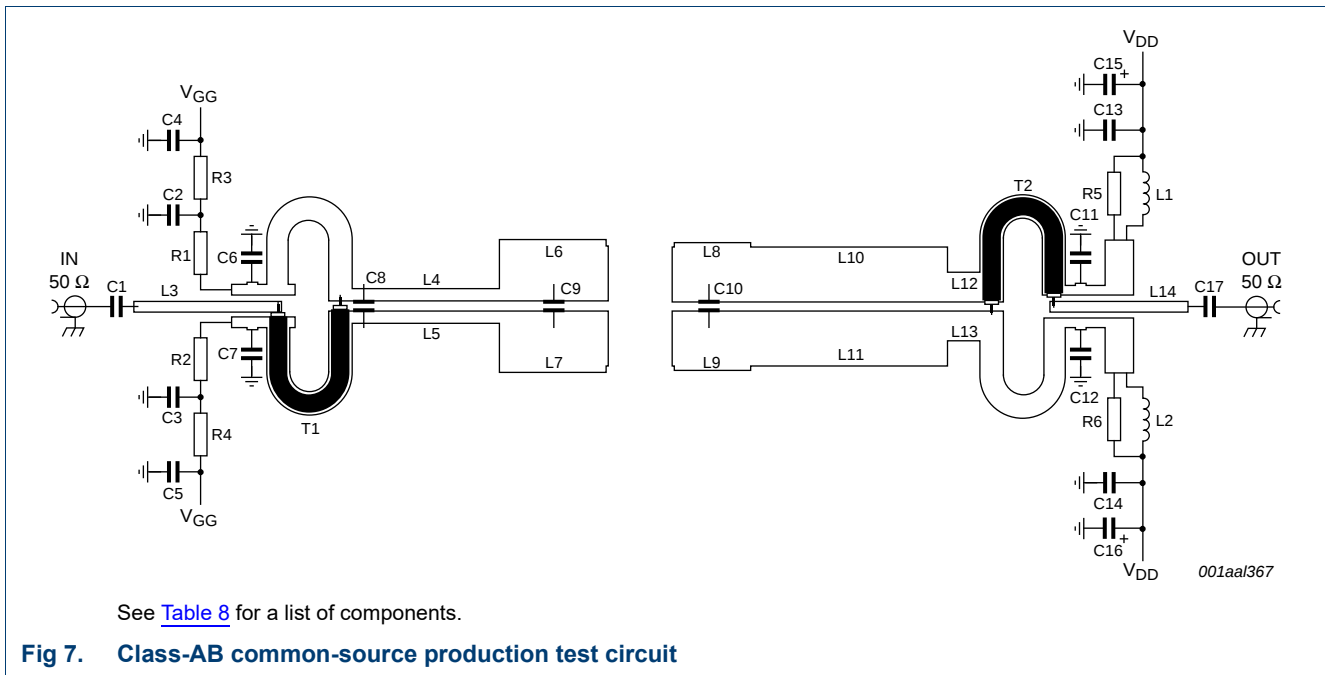


Table 8. List of components

For test circuit, see [Figure 7](#) and [Figure 8](#).

Component	Description	Value	Remarks
C1	multilayer ceramic chip capacitor	47 pF	[1]
C6, C7, C11, C12, C17	multilayer ceramic chip capacitor	27 pF	[2]
C2, C3	multilayer ceramic chip capacitor	100 nF	Murata X7R or equivalent
C4, C5, C13, C14	multilayer ceramic chip capacitor	4.7 μ F	TDK C4532X7R1E475MT020U or capacitor of same quality.
C8	multilayer ceramic chip capacitor	1.5 pF	[2]
C9	multilayer ceramic chip capacitor	3.3 pF	[2]
C10	multilayer ceramic chip capacitor	6.2 pF	[3]
C15, C16	electrolytic capacitor	220 μ F	TDK C4532X7R1E475MT020U or capacitor of same quality.
L1, L2	4 turns, 0.8 mm enameled copper wire	D = 3.5 mm; length = 4 mm	
L3	microstrip	-	[4] (W $\times$ L) 1.67 mm $\times$ 19.17 mm
L4, L5	microstrip	-	[4] (W $\times$ L) 1.9 mm $\times$ 23.7 mm
L6, L7	microstrip	-	[4] (W $\times$ L) 9.6 mm $\times$ 17.3 mm
L8, L9	microstrip	-	[4] (W $\times$ L) 9 mm 12 mm
L10, L11	microstrip	-	[4] (W $\times$ L) 8.5 mm $\times$ 31.0 mm
L12, L13	microstrip	-	[4] (W $\times$ L) 4.52 mm $\times$ 5.0 mm
L14	microstrip	-	[4] (W $\times$ L) 1.67 mm $\times$ 21.67 mm
R1, R2	SMD resistor	11 Ω	1206
R3, R4	SMD resistor	1 k Ω	1206
R5, R6	SMD resistor	12 Ω	1206
T1, T2	semi rigid coax	Z = 50 Ω ; length = 34 mm	

[1] American technical ceramics type 100A or capacitor of same quality.

[2] American technical ceramics type 100B or capacitor of same quality.

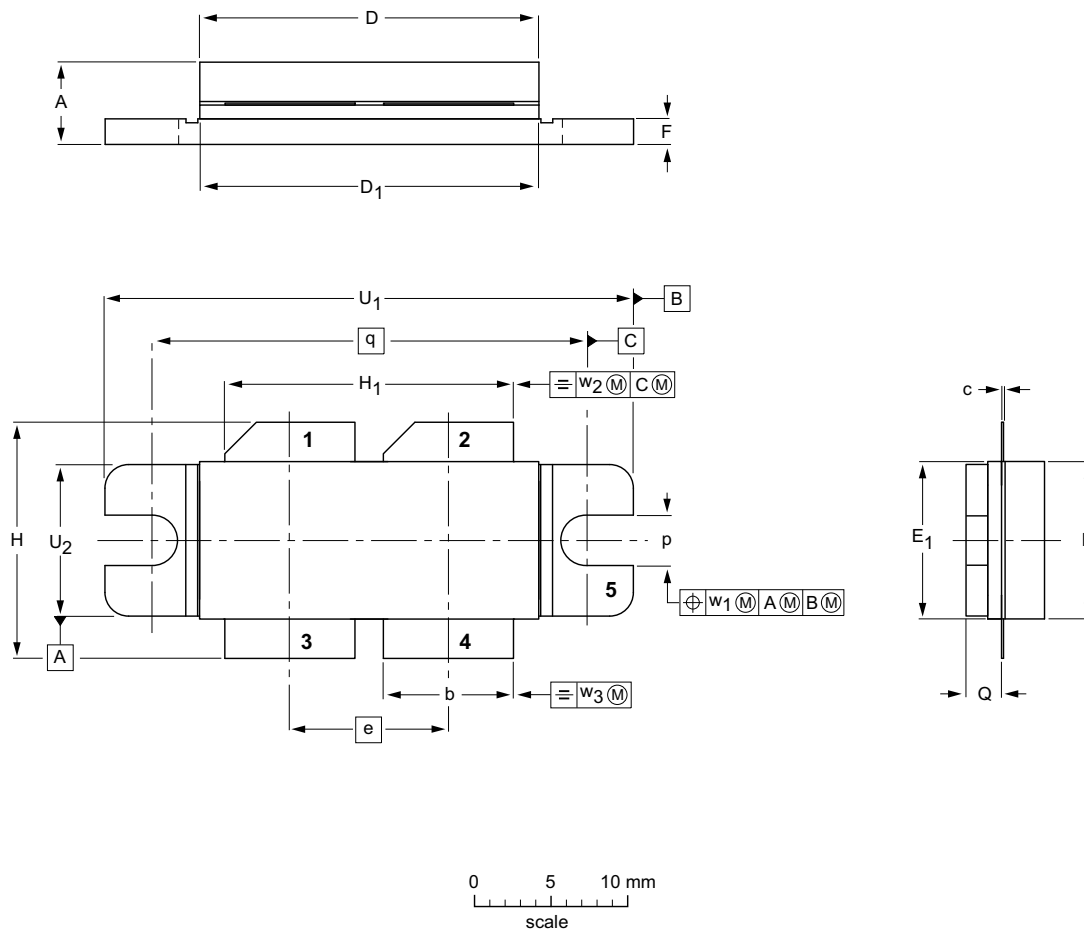
[3] American technical ceramics type 180R or capacitor of same quality.

[4] Printed-Circuit Board (PCB): Taconic RF35; $\epsilon_r = 3.5$ F/m; height = 0.79 mm; Cu (top/bottom metallization); thickness copper plating = 35 μ m.

9. Package outline

Flanged balanced ceramic package; 2 mounting holes; 4 leads

SOT540A



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D ₁	e	E	E ₁	F	H	H ₁	p	Q	q	U ₁	U ₂	w ₁	w ₂	w ₃
mm	5.77 5.00	8.51 8.26	0.15 0.10	22.05 21.64	22.05 21.64	10.21	10.26 10.06	10.31 10.01	1.78 1.52	15.75 14.73	18.72 18.47	3.38 3.12	2.72 2.46	27.94	34.16 33.91	9.91 9.65	0.25	0.51	0.25
inches	0.227 0.197	0.335 0.325	0.006 0.004	0.868 0.852	0.868 0.852	0.402	0.404 0.396	0.406 0.394	0.070 0.060	0.620 0.580	0.737 0.727	0.133 0.123	0.107 0.097	1.100	1.345 1.335	0.390 0.380	0.010	0.020	0.010

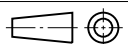
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT540A						-99-12-28- 12-05-02

Fig 9. Package outline SOT540A

10. Abbreviations

Table 9. Abbreviations

Acronym	Description
CW	Continuous Waveform
DC	Direct Current
D-MOS	Diffusion Metal-Oxide Semiconductor
ESD	ElectroStatic Discharge
HF	High Frequency
LDMOS	Laterally Diffused Metal Oxide Semiconductor
LDMOST	Laterally Diffused Metal-Oxide Semiconductor Transistor
RF	Radio Frequency
SMD	Surface-Mount Device
VSWR	Voltage Standing-Wave Ratio

11. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF645#2	20150901	Product data sheet	-	BLF645_1
Modifications:	- The format of this document has been redesigned to comply with the new identity guidelines of Ampleon. - Legal texts have been adapted to the new company name where appropriate.			
BLF645_1	20100127	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.ampleon.com>.

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