CSR1021 QFN

Production Information Data Sheet

CS-303917-DS Rev. 8

June 3, 2016

Qualcomm Technologies International, Ltd.

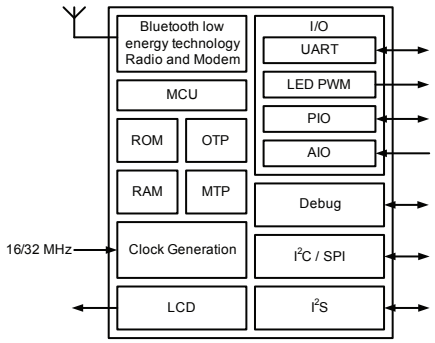
Device Description

- Bluetooth® low energy technology single-mode SoC with G.722 Audio Codec
- 16-bit RISC MCU, Up to 16 MB external SPI flash from system generated 2.5 to 3.3 V rail, 80 KB RAM, 192 KB ROM, 60 KB OTP
- 37 digital PIOs, 2 analogue AIOs, SPI, I²C, I²S, quadrature decoders, 3D shutter/LED PWM modules, key scanner, LCD glass drive, IR encoder, 10-bit Aux ADC
- Ultra low power Bluetooth low energy technology radio v4.2 specification compliant radio
- 60-lead 8 x 8 x 0.65 mm, 0.5 mm pitch QFN

Applications

- Bluetooth low energy technology:
  - HID: keyboards, mice, touchpads, advanced remote controls with voice activation
  - Sports and fitness sensors: heart rate, runner/cycle speed and cadence
  - Health sensors: blood pressure, thermometer and glucose meters
  - Mobile accessories: watches, proximity tags, alert tags and camera controls
  - Smart home: heating/lighting control
- CSRmesh™ connectivity: Internet of Things control

System Architecture



Ecosystem

Qualcomm Technologies International, Ltd. (formerly known as Cambridge Silicon Radio Limited) is a company registered in England and Wales with a registered office at: Churchill House, Cambridge Business Park, Cowley Road, Cambridge, CB4 0WZ, United Kingdom.
Registered Number: 3665875 | VAT number: GB787433096

General Description

CSR1021 QFN is Qualcomm Technologies International, Ltd. (QTIL) 's latest generation Bluetooth low energy technology single-mode platform device with ultra low power consumption. CSR1021 QFN enables customer applications of up to 60 KB to be stored on chip for optimal power consumption.

Qualcomm® µEnergy™ technology enables ultra low-power connectivity and basic data transfer for applications previously limited by the power consumption, size constraints and complexity of other wireless standards. The µEnergy platform provides everything required to create a Bluetooth low energy technology product with RF, baseband, MCU, qualified Bluetooth v4.2 specification stack and customer application running on a single IC.

QTIL is the industry leader for Bluetooth low energy technology. Bluetooth low energy technology enables connectivity and data transfer to leading smartphone, tablet and personal computing devices including iOS, Android, Windows Phone 8 and Blackberry OS10 devices.

CSRmesh places the smartphone at the centre of the Internet of Things allowing an almost unlimited number of Bluetooth low energy technology enabled devices to be simply networked together and controlled directly from a single smartphone, tablet or PC.

CSR1021 QFN supports profiles for health and fitness sensors, watches, keyboards, mice and advanced remote controls.

Device Details

Ultra Low Power Bluetooth low energy technology Radio

- Single pin RF connection (50 Ω impedance in TX and RX modes)
- Requires no external RF components[1]
- Operates from a single crystal
- Bluetooth v4.2 specification compliant

Bluetooth Transmitter

- 4 dBm RF transmit power
- TX power control
- No external power amplifier or TX/RX switch required

Bluetooth Receiver

- -90 dBm sensitivity
- -91.5 dBm RX Boost mode available: Enhances RX sensitivity at higher receive current cost
- Integrated channel filters
- Digital demodulator for improved sensitivity and co-channel rejection
- Fast AGC for enhanced dynamic range

Bluetooth Stack

QTIL's protocol stack runs on the integrated MCU:

- Support for Bluetooth v4.2 specification features:
  - Master and slave operation
  - Including encryption
- Software stack in firmware includes:
  - GAP
  - L2CAP
  - Security manager
  - Generic attribute protocol
  - Attribute profile
  - Bluetooth low energy technology profile support

Synthesiser

- Fully integrated synthesiser requires no external VCO varactor diode, resonator or loop filter

Baseband and Software

- Integrated MAC for all packet types enables packet handling without the need to involve the MCU

Audio

- Digital microphone input
- I²S port for PCM I/O
- G.722 Codec

Physical Interfaces

- 32 digital flexible PIOs
- 5 digital static PIOs
- 2 analogue AIOs
- UART
- SPI master interface
- Debug SPI interface for programming
- Serial memory flash controller
- I²C master controller
- 4 x quadrature decoders
- PWM 3D shutter control
- 5 x LED PWMs
- Keyboard scanner
- LCD glass drive
- 10-bit Aux ADC
- IR encoder

Auxiliary Features

- Battery monitor
- 6 power modes
- Power management features include software shutdown and hardware wake-up
- Wake-up power management from any PIO
- Integrated switch-mode power supply
- Linear regulator (internal use only)
- AES-128
- Watchdog timer

Memory

- 64 KB (Code) and 16 KB (Data) RAM
- 192 KB ROM
- 60 KB OTP
- 256 Byte MTP
- Up to 16 MB external SPI flash from system generated 2.5 to 3.3 V rail

Battery

- Battery input voltage 3.6 V to 0.9 V

Temperature Specification

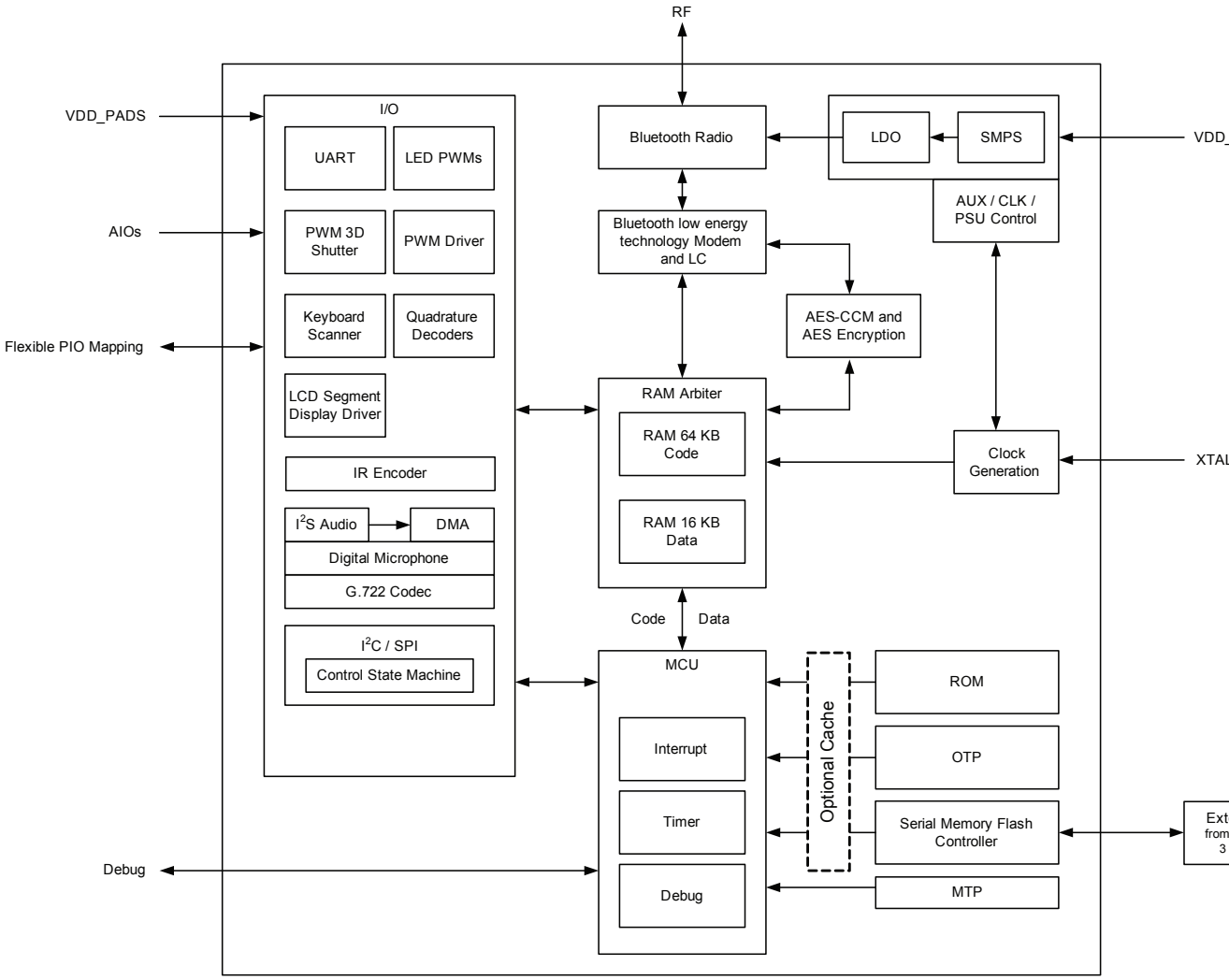
- Operating temperature -30 to 85 ºC

Package

- 60-lead 8 x 8 x 0.65 mm, 0.5 mm pitch QFN
- Single side routing pinout optimised

NOTE 1. Certain antennas with gain may require a simple filter.

CSR1021 QFN Functional Block Diagram



CSR1021 QFN Functional Block Diagram

Ordering Information

Device	Package			Order Number
	Type	Size	Shipment Method	
CSR1021 QFN	QFN 60-lead (Pb free)	8 x 8 x 0.65 mm 0.5 mm pitch	Tape and reel	CSR1021A05-IQQS-R

NOTE Minimum order quantity is 2 kcps.

Supply chain: QTIL's manufacturing policy is to multisource volume products. For further details, contact your local sales account manager or representative.

QTIL Contacts

General information	www.csr.com
Information on this product	sales@csr.com
Customer support for this product	www.csrsupport.com
Details of compliance and standards	product.compliance@csr.com
Help with this document	comments@csr.com

Document History

Revision	Date	Change Reason
1	16 OCT 13	Original publication of this document.
2	08 OCT 15	Updated information for Engineering Sample release.
3	09 OCT 15	Updated Peripheral Interfaces information.
4	11 MAR 16	Updated to Pre-production Information.
5	10 MAY 16	Updated to Production Information.
6	13 MAY 16	Revised RF information.
7	19 MAY 16	Updated Corporate Branding.
8	03 JUN 16	Updated Document References.

Contents

Tables

Figures

1 Status Information

QTIL Product Data Sheets progress according to the following formats: Advance Information, Engineering Sample, Pre-production Information and Production Information. The status of this document is Production Information.

Advance Information

Information for designers concerning QTIL product in development. All values specified are the target values of the design. Minimum and maximum values specified are only given as guidance to the final specification limits and must not be considered as the final values.

Engineering Sample

Information about initial devices. Devices are untested or partially tested prototypes, their status is described in an Engineering Sample Release Note. All values specified are the target values of the design. Minimum and maximum values specified are only given as guidance to the final specification limits and must not be considered as the final values.

All detailed specifications including pinouts and electrical specifications may be changed by QTIL without notice.

Pre-production Information

Pinout and mechanical dimension specifications finalised. All values specified are the target values of the design. Minimum and maximum values specified are only given as guidance to the final specification limits and must not be considered as the final values.

All electrical specifications may be changed by QTIL without notice.

Production Information

Final Data Sheet including the guaranteed minimum and maximum limits for the electrical specifications.

Production Data Sheets supersede all previous document versions.

1.1 Device Implementation

As the feature-set of the CSR1021 QFN is firmware build-specific, see the relevant software release note for the exact implementation of features on the CSR1021 QFN.

1.2 Life Support Policy and Use in Safety-critical Applications

QTIL's products are not authorised for use in life-support or safety-critical applications. Use in such applications is done at the sole discretion of the customer. QTIL will not warrant the use of its devices in such applications.

1.3 CSR Green Semiconductor Products and RoHS Compliance

CSR1021 QFN devices meet the requirements of Directive 2011/65/EU of the European Parliament and of the Council on the Restriction of Hazardous Substance (RoHS).

CSR1021 QFN devices are free from halogenated or antimony trioxide-based flame retardants and other hazardous chemicals. For more information, see QTIL's *Environmental Compliance Statement for CSR Green Semiconductor Products*.

2 Package Information

CSR1021 QFN is available in a 8 x 8 x 0.65 mm 60-lead QFN package.

2.1 CSR1021 QFN Pinout Diagram

The CSR1021 QFN IC has 60 pins, numbered sequentially in an anti-clockwise (counter-clockwise) direction, starting from lead 1.

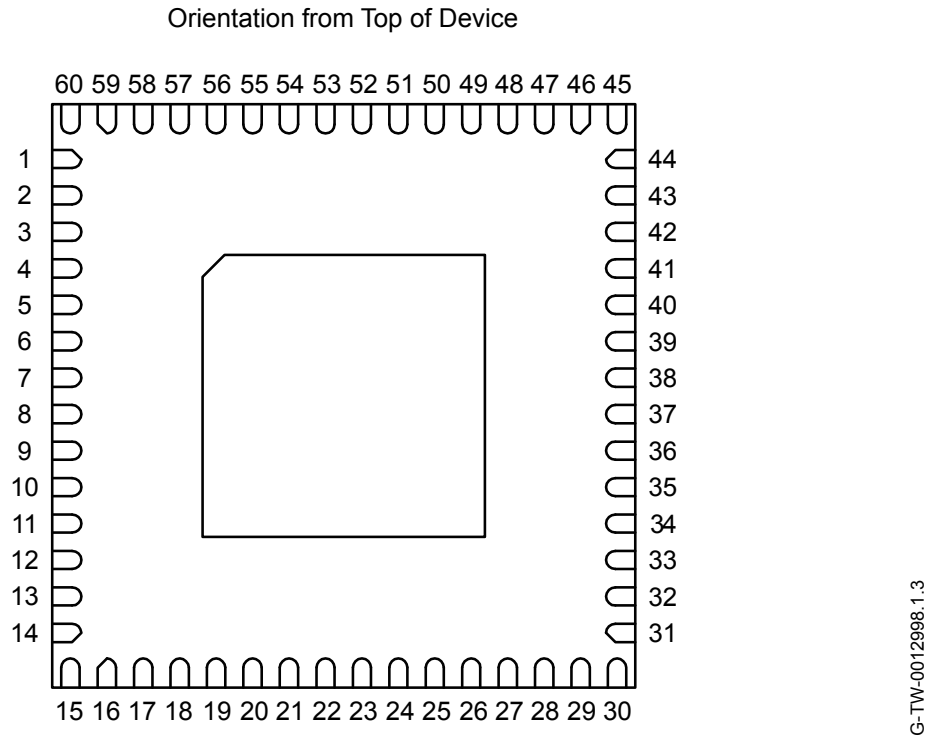


Figure 2-1 CSR1021 QFN Pinout Diagram

2.2 Device Terminal Functions

The leads on the CSR1021 QFN are grouped into a variety of terminal functions. The device terminal functions include:

- Radio
- Synthesiser and oscillator
- PIO port
- Test and debug
- Power supplies and control
- Unconnected terminals

2.2.1 Device Terminal Functions (Radio)

Table 2-1 CSR1021 QFN Device Terminal Functions (Radio)

Radio	Lead	Pad Type	Supply Domain	Description
RF	7	RF	VDD_RF	Antenna port for Bluetooth transmitter / receiver.

2.2.2 Device Terminal Functions (Synthesiser and Oscillator)

Table 2-2 CSR1021 QFN Device Terminal Functions (Synthesiser and Oscillator)

Synthesiser and Oscillator	Lead	Pad Type	Supply Domain	Description
XTAL_IN	10	Analogue	VDD_RF	Reference clock input.
XTAL_OUT	9	Analogue	VDD_RF	Drive for clock crystal.

2.2.3 Device Terminal Functions (PIO Port)

Table 2-3 CSR1021 QFN Device Terminal Functions (PIO Port)

PIO Port	Lead	Pad Type	Supply Domain	Description
PIO[36]	24	Digital: Bidirectional with programmable strength internal pull-up / pull-down	VDD_MEM	Static programmable I/O line 36.
PIO[35]	27	Digital: Bidirectional with programmable strength internal pull-up / pull-down	VDD_MEM	Static programmable I/O line 35.

Table 2-3 CSR1021 QFN Device Terminal Functions (PIO Port) (Continued)

PIO Port	Lead	Pad Type	Supply Domain	Description
PIO[34]	25	Digital: Bidirectional with programmable strength internal pull-up / pull-down	VDD_MEM	Static programmable I/O line 34.
PIO[33]	26	Digital: Bidirectional with programmable strength internal pull-up / pull-down	VDD_MEM	Static programmable I/O line 33.
PIO[32]	34	Digital: Bidirectional with programmable strength internal pull-up / pull-down	VDD_PADS	Static programmable I/O line 32.
PIO[31]	33	Digital: Bidirectional with programmable strength internal pull-up / pull-down and LCD glass driving capability	VDD_PADS	General programmable I/O line 31.
PIO[30]	38	Digital: Bidirectional with programmable strength internal pull-up / pull-down and LCD glass driving capability	VDD_PADS	General programmable I/O line 30.
PIO[29]	37	Digital: Bidirectional with programmable strength internal pull-up / pull-down and LCD glass driving capability	VDD_PADS	General programmable I/O line 29.
PIO[28]	36	Digital: Bidirectional with programmable strength internal pull-up / pull-down and LCD glass driving capability	VDD_PADS	General programmable I/O line 28.
PIO[27]	35	Digital: Bidirectional with programmable strength internal pull-up / pull-down and LCD glass driving capability	VDD_PADS	General programmable I/O line 27.
PIO[26]	59	Digital: Bidirectional with programmable strength internal pull-up / pull-down and LCD glass driving capability	VDD_PADS	General programmable I/O line 26.
PIO[25]	58	Digital: Bidirectional with programmable strength internal pull-up / pull-down and LCD glass driving capability	VDD_PADS	General programmable I/O line 25.
PIO[24]	57	Digital: Bidirectional with programmable strength internal pull-up / pull-down and LCD glass driving capability	VDD_PADS	General programmable I/O line 24.
PIO[23]	56	Digital: Bidirectional with programmable strength internal pull-up / pull-down and LCD glass driving capability	VDD_PADS	General programmable I/O line 23.
PIO[22]	55	Digital: Bidirectional with programmable strength internal pull-up / pull-down and LCD glass driving capability	VDD_PADS	General programmable I/O line 22.
PIO[21]	54	Digital: Bidirectional with programmable strength internal pull-up / pull-down and LCD glass driving capability	VDD_PADS	General programmable I/O line 21.

Table 2-3 CSR1021 QFN Device Terminal Functions (PIO Port) (Continued)

PIO Port	Lead	Pad Type	Supply Domain	Description
PIO[20]	53	Digital: Bidirectional with programmable strength internal pull-up / pull-down and LCD glass driving capability	VDD_PADS	General programmable I/O line 20.
PIO[19]	52	Digital: Bidirectional with programmable strength internal pull-up / pull-down and LCD glass driving capability	VDD_PADS	General programmable I/O line 19.
PIO[18]	50	Digital: Bidirectional with programmable strength internal pull-up / pull-down and LCD glass driving capability	VDD_PADS	General programmable I/O line 18.
PIO[17]	49	Digital: Bidirectional with programmable strength internal pull-up / pull-down and LCD glass driving capability	VDD_PADS	General programmable I/O line 17.
PIO[16]	32	Digital: Bidirectional with programmable strength internal pull-up / pull-down and LCD glass driving capability	VDD_PADS	General programmable I/O line 16.
PIO[15]	31	Digital: Bidirectional with programmable strength internal pull-up / pull-down and LCD glass driving capability	VDD_PADS	General programmable I/O line 15.
PIO[14]	30	Digital: Bidirectional with programmable strength internal pull-up / pull-down and LCD glass driving capability	VDD_PADS	General programmable I/O line 14.
PIO[13]	5	Digital: Bidirectional with programmable strength internal pull-up / pull-down and LCD glass driving capability	VDD_PADS	General programmable I/O line 13.
PIO[12]	4	Digital: Bidirectional with programmable strength internal pull-up / pull-down and LCD glass driving capability	VDD_PADS	General programmable I/O line 12.
PIO[11]	3	Digital: Bidirectional with programmable strength internal pull-up / pull-down and LCD glass driving capability	VDD_PADS	General programmable I/O line 11.
PIO[10]	2	Digital: Bidirectional with programmable strength internal pull-up / pull-down and LCD glass driving capability	VDD_PADS	General programmable I/O line 10.
PIO[9]	1	Digital: Bidirectional with programmable strength internal pull-up / pull-down and LCD glass driving capability	VDD_PADS	General programmable I/O line 9.
PIO[8]	60	Digital: Bidirectional with programmable strength internal pull-up / pull-down and LCD glass driving capability	VDD_PADS	General programmable I/O line 8.

Table 2-3 CSR1021 QFN Device Terminal Functions (PIO Port) (Continued)

PIO Port	Lead	Pad Type	Supply Domain	Description
PIO[7]	48	Digital: Bidirectional with programmable strength internal pull-up / pull-down and LCD glass driving capability	VDD_PADS	General programmable I/O line 7.
PIO[6]	47	Digital: Bidirectional with programmable strength internal pull-up / pull-down and LCD glass driving capability	VDD_PADS	General programmable I/O line 6.
PIO[5]	46	Digital: Bidirectional with programmable strength internal pull-up / pull-down and LCD glass driving capability	VDD_PADS	General programmable I/O line 5.
PIO[4]	45	Digital: Bidirectional with programmable strength internal pull-up / pull-down and LCD glass driving capability	VDD_PADS	General programmable I/O line 4.
PIO[3]	43	Digital: Bidirectional with programmable strength internal pull-up / pull-down and LCD glass driving capability	VDD_PADS	General programmable I/O line 3.
PIO[2]	42	Digital: Bidirectional with programmable strength internal pull-up / pull-down and LCD glass driving capability	VDD_PADS	General programmable I/O line 2.
PIO[1]	41	Digital: Bidirectional with programmable strength internal pull-up / pull-down and LCD glass driving capability	VDD_PADS	General programmable I/O line 1.
PIO[0]	40	Digital: Bidirectional with programmable strength internal pull-up / pull-down and LCD glass driving capability	VDD_PADS	General programmable I/O line 0.
AIO[1]	13	Unidirectional analogue	VDD_AUX	Analogue programmable input line.
AIO[0]	14	Unidirectional analogue	VDD_AUX	Analogue programmable input line.

2.2.4 Device Terminal Functions (Test and Debug)

Table 2-4 CSR1021 QFN Device Terminal Functions (Test and Debug)

Test and Debug	Lead	Pad Type	Supply Domain	Description
SPI_PIO#	39	Input with strong internal pull-down	VDD_PADS	Selects Debug SPI on PIO[3:0].

2.2.5 Device Terminal Functions (Power Supplies and Control)

Table 2-5 CSR1021 QFN Device Terminal Functions (Power Supplies and Control)

Power Supplies and Control	Lead	Description
VDD_BAT	16	Positive supply from the battery.
SMPS_LX1	17	Terminal 1 of the external 2.2 µH inductor connected to this pin.
SMPS_LX2	18	Terminal 2 of the external 2.2 µH inductor connected to this pin.
VDD_AUX	21	SMPS output for the auxiliary rail and AIO ports.
VDD_DIG	22	SMPS output for the digital rail.
VDD_MEM	23	SMPS output for the memory rail and PIO[36:33].
VDD_RAD	19	SMPS output for the radio rail.
VDD_RF_IN	20	SMPS output for the radio rail.
VDD_RF	11	Decoupled supply for radio and XTAL pads.
VSS_RF	8, 6	Ground connection for RF.
VDD_PADS	44, 28	Positive supply for digital I/O ports PIO[32:0] and SPI_PIO#.
VSS	51, 29, 15 and the exposed pad	Ground connections.

2.2.6 Device Terminal Functions (Unconnected Terminals)

Table 2-6 CSR1021 QFN Device Terminal Functions (Unconnected Terminals)

Unconnected Terminals	Lead	Description
NC	12	Leave unconnected.

NOTE Do not connect this pin doing so may have an adverse affect on the system.

This pin must be left floating.

Do not ground this pin (grounding this pin prevents the chip from functioning).

2.3 Package Dimensions

CSR1021 QFN is available in a 8 x 8 x 0.65 mm 60-lead QFN package.

Package Dimensions Diagram

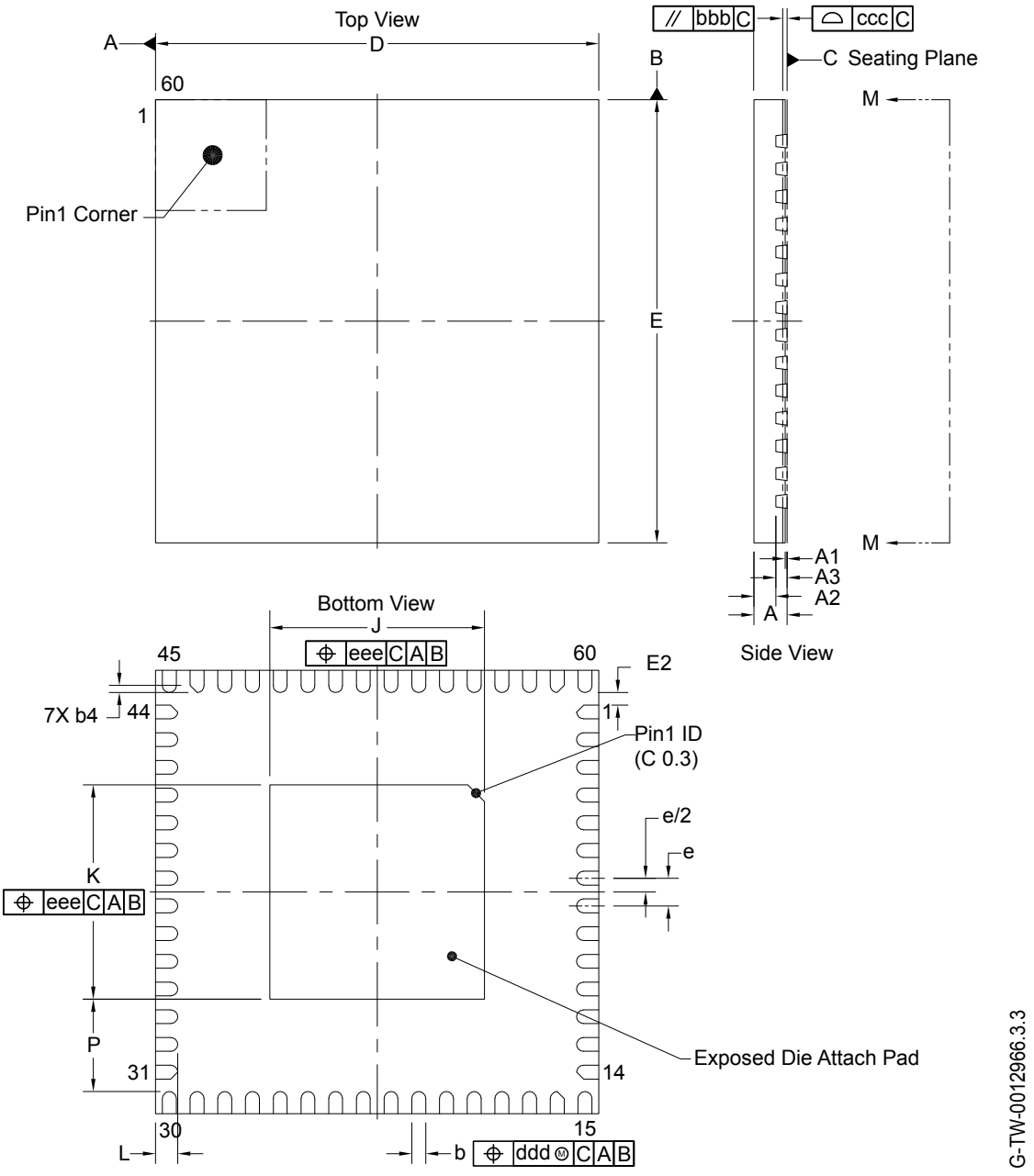


Figure 2-2 CSR1021 QFN Package Dimensions Diagram

Package Dimensions Table

Table 2-7 CSR1021 QFN Package Dimensions Table

Dimension	Min	Typ	Max	Dimension	Min	Typ	Max
A	0.55	0.6	0.65	e	-	0.5	-
A1	0	0.035	0.05	J	3.77	3.87	3.97
A2	-	0.4	-	K	3.77	3.87	3.97
A3	-	0.203	-	L	0.35	0.4	0.45
b	0.2	0.25	0.3	P	1.565	-	-
b4	-	C0.128	-	bbb	-	0.1	-
D	7.9	8	8.1	ccc	-	0.08	-
E	7.9	8	8.1	ddd	-	0.1	-
E2	-	0.225	-	eee	-	0.1	-
Notes	1. Dimensioning and tolerances conform to ASME Y14.5M. - 1994 2. Pin #1 identifier is placed on the top surface of the package. Exact shape and size of this feature is optional. 3. Coplanarity applies to leads, corner leads and die attach pad. 4. Lead 29 is not bevelled unlike similar corner leads 1, 14, 16, 31, 44, 46 and 59 which are bevelled. 5. Radius for all leads is 125 µm.						
Description	60-lead Quad Flat No-lead Package						
Size	8 x 8 x 0.65 mm			**JEDEC**	MO-220		
Pitch	0.5			**Units**	mm		

2.4 PCB Design and Assembly Considerations

This section lists recommendations to achieve maximum board-level reliability of the 8 x 8 x 0.65 mm QFN 60-lead package:

- NSMD lands (lands smaller than the solder mask aperture) are preferred, because of the greater accuracy of the metal definition process compared to the solder mask process. With solder mask defined pads, the overlap of the solder mask on the land creates a step in the solder at the land interface, which can cause stress concentration and act as a point for crack initiation.
- QTIL recommends that the PCB land pattern is in accordance with IPC standard IPC-7351.
- Solder paste must be used during the assembly process.

2.5 Typical Solder Reflow Profile

For information, see *Typical Solder Reflow Profile for Lead-free Devices Information Note*.

3 Bluetooth Modem

CSR1021 QFN's modem supports Bluetooth low energy technology and has 4 link controller blocks supporting up to 4 connections.

3.1 RF Port

CSR1021 QFN contains a single-ended 50 Ω RF TX / RX port pin. No external matching to 50 Ω is required.

3.2 RF Receiver

The receiver features a near-zero IF architecture enabling the channel filters to be integrated onto the die. Sufficient out-of-band blocking provided on die at the LNA input enables the receiver to be used in close proximity to GSM and W-CDMA cellular phone transmitters without being significantly desensitised:

- Receive sensitivity is typically -90 dBm
- Software selectable Boost mode can be enabled for additional sensitivity
- An ADC digitises the IF received signal
- An AGC supports the Bluetooth v4.2 specification's full range of input signal levels

3.2.1 RSSI

Front-end LNA gain is changed according to measured RSSI, keeping the first mixer input signal within a limited range. This improves the dynamic range of the receiver, improving performance in interference-limited environments.

3.3 RF Transmitter

3.3.1 Power Amplifier

The internal PA can deliver a maximum of 4 dBm at the RF pin into a 50 Ω load. The software can be configured to deliver lower output powers to reduce the current consumption during transmit. For more information, see *CSR102x A05 Limitations*.

3.4 Bluetooth Radio Synthesiser

The Bluetooth radio synthesiser is fully integrated onto the die with no requirement for external components and meets all lock-time requirements of the Bluetooth v4.2 specification.

3.5 Baseband

3.5.1 Physical Layer Hardware Engine

Dedicated logic performs:

- Cyclic redundancy check
- Encryption
- Data whitening
- Access code correlation

4 Clock Generation

4.1 Clock Architecture

Figure 4-1 shows CSR1021 QFN's 3 clock inputs:

- Fast Clock:
  - Bluetooth system reference clock required for TX and RX
  - Supplied by an external 16 or 32 MHz crystal
- Intermediate Clock:
  - Internal clock source that can operate at various intermediate frequencies (62.5 kHz to 8 MHz in approximate log spacing)
  - Suitable for peripherals that require a moderate clock frequency of low accuracy
  - Lower power than Fast Clock and can work in Deep Sleep
- Slow Clock:
  - Lowest power and works in Deep Sleep
  - A digital state machine uses temperature sampling to ensure clock drift for sleep timing stays within 500 ppm
  - Running at approximately 32 kHz, without trim, only calibration

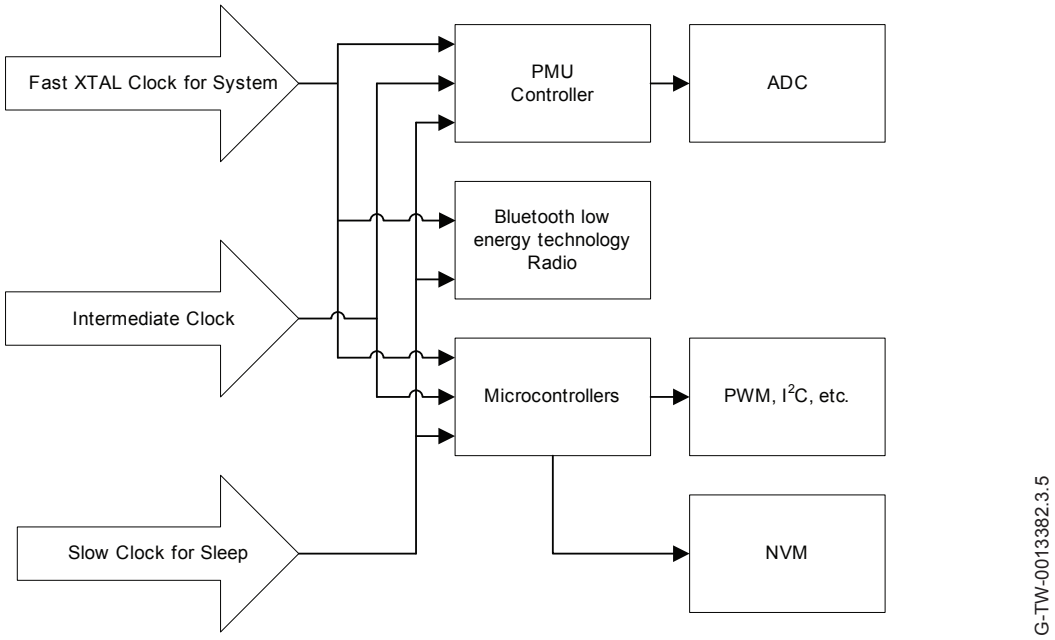


Figure 4-1 CSR1021 QFN Clock Architecture

4.2 Crystal Oscillator: XTAL_IN and XTAL_OUT

CSR1021 QFN has a crystal driver circuit. This operates with an external crystal to form a Pierce oscillator. Figure 4-2 shows how the external crystal is connected to pins XTAL_IN and XTAL_OUT.

NOTE The crystal oscillator needs no external capacitors.

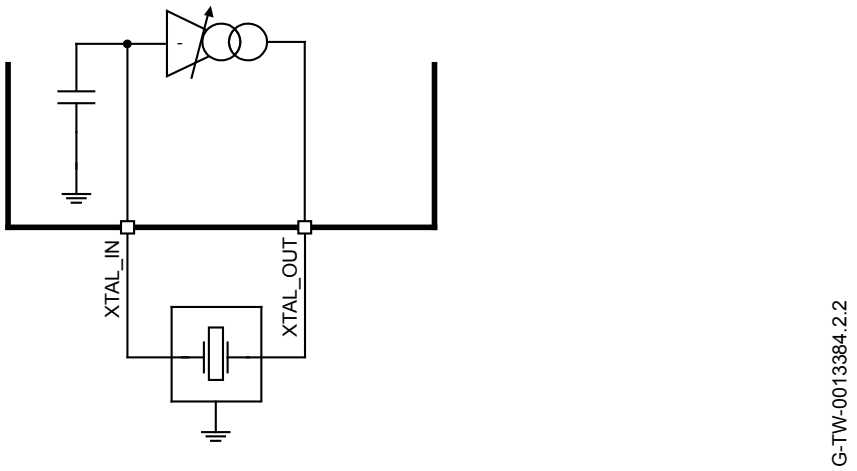


Figure 4-2 Crystal Driver Circuit

NOTE The PCB design must ensure that the total trace capacitance on XTAL_IN and XTAL_OUT are less than 2 pF each.

4.2.1 Crystal Specification

Table 4-1 lists the specification required for a CSR1021 QFN external crystal.

NOTE Crystal's with the specification in Table 4-1 are produced by a limited number of manufacturers. QTIL recommends only using crystals listed in *CSR102x Recommended Crystals Specification*.

Table 4-1 Crystal Specification

Parameter	Description	Min	Typ	Max	Unit
F_{nom}	Nominal fundamental frequency	16	16	32	MHz
T_{stg}	Storage temperature	-40	-	125	°C
$T_{op\_industrial}$	Operating Temperature range	-30	-	85	°C
C_{P_16MHz}	Package capacitance (16 MHz)	-	0.8	-	pF
C_L	Load capacitance	-	6	-	pF
F_tol_nom	Frequency Tolerance nominal at room temperature	-10	-	10	ppm
F_tol_temp_ind	Frequency stability over temperature (industrial)	-10	-	10	ppm
F_tol_aging	Frequency tolerance aging 1st year @ 25 °C	-3	-	3	ppm/yr
Sensitivity	Frequency variation v's load capacitance changes @ 25 °C	-	20	25	ppm/pF
ESR_{16MHz}	Motional Resistance (16 MHz)	-	50	80	Ω

4.3 Sleep Clock

CSR1021 QFN uses the slow clock or crystal in low-power modes rather than a dedicated sleep clock.

5 Operating Modes

CSR1021 QFN has 6 operating modes. 4 are Deep Sleep modes:

- Active
- Radio-on
- Deep Sleep: 16 KB Data RAM and 64 KB RAM Retention
- Deep Sleep: 16 KB Data RAM Retention
- Deep Sleep: No RAM Retention and External Interrupts and Timer Enabled
- Deep Sleep: No RAM Retention and External Interrupts Enabled

5.1 Active Mode

In Active mode, the processor runs:

- Code and/or performs activites with peripherals.
- With at least 1 link controller powered.

5.2 Radio-on Mode

In Radio-on mode, the Bluetooth radio is turned on.

NOTE Radio-on mode can only be entered from Active mode.

5.3 Deep Sleep: 16 KB Data RAM and 64 KB RAM Retention Mode

In Deep Sleep: 16 KB Data RAM and 64 KB RAM Retention mode:

- Normal operation uses only the slow clock or intermediate clock (running at a slow speed).
- CSR1021 QFN supports activity in peripherals to perform a particular operation (e.g. PWMs, keyboard scanner) or wake the chip on activity (e.g. UART, application SPI).
- Link controller state is maintained: this can be active (advertising, scanning or in a connection) and CSR1021 QFN can deep sleep between periods on or around radio activity.
- A PIO deep sleep timer time-out or optional temperature change or low battery can wake the chip by generating an interrupt.
- It is possible to keep the processor powered and its power controlled using power gating.

5.4 Deep Sleep: 16 KB Data RAM Retention Mode

In Deep Sleep: 16 KB Data RAM Retention mode:

- Normal operation uses only the slow clock or intermediate clock (running at a slow speed).
- CSR1021 QFN supports activity in peripherals to perform a particular operation (e.g. PWMs, keyboard scanner) or wake the chip on activity (e.g. UART, application SPI).

- Link controller state is maintained: this can be active (advertising, scanning or in a connection) and CSR1021 QFN can deep sleep between periods on or around radio activity.
- A PIO deep sleep timer time-out or optional temperature change or low battery can wake the chip by generating an interrupt.
- It is possible to keep the processor powered and its power controlled using power gating.

5.5 Deep Sleep: No RAM Retention and External Interrupts and Timer Enabled Mode

In Deep Sleep: No RAM Retention and External Interrupts and Timer Enabled mode:

- VDD_BAT must always be present.
- A PIO can wake the chip (programmably as in Deep Sleep: No RAM Retention and External Interrupts Enabled mode).
- The following can wake the chip:
  - PIO hibernate timer time-out.
  - Temperature change.
  - Low battery.

5.6 Deep Sleep: No RAM Retention and External Interrupts Enabled Mode

In Deep Sleep: No RAM Retention and External Interrupts Enabled mode:

- An attached battery can be used as a wakeup.
- No timers run, therefore CSR1021 QFN can only be woken by a PIO or a rise on VDD_BAT.
- VDD_BAT can be removed if VDD_PADS remains powered, because the pull states of pads are preserved.
- Ignore a rise on VDD_BAT until a PIO has latched an event (enabling 2 different Deep Sleep: No RAM Retention and External Interrupts Enabled modes).
- The PIOs that CSR1021 QFN is sensitive to on wakeup are programmable, i.e. it is possible to ignore events on some PIOs but not others.

6 Microcontroller, Memory and Baseband Logic

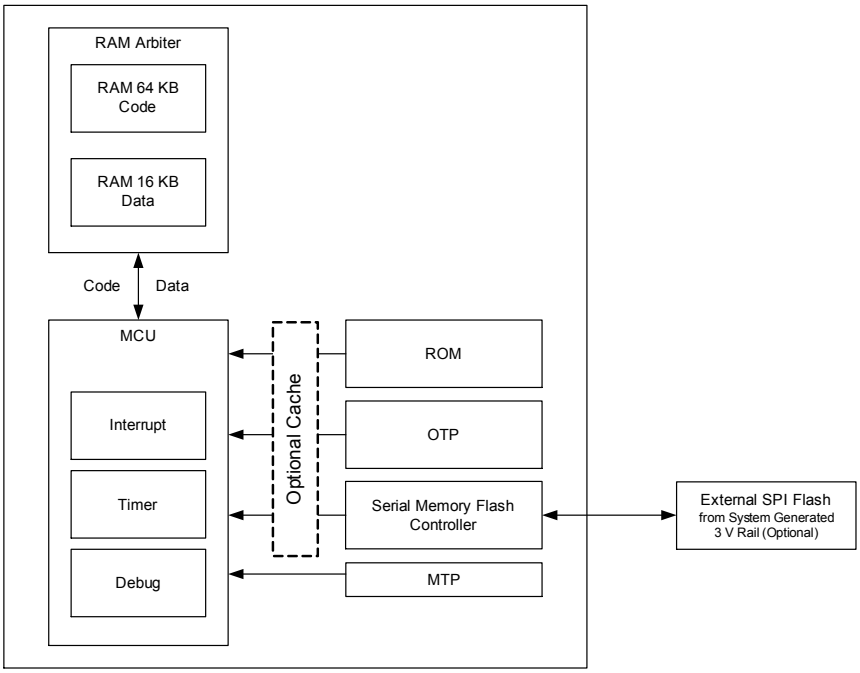


Figure 6-1 Baseband Digits Block Diagram

6.1 Microcontroller

The MCU, interrupt controller and event timer run the Bluetooth software stack and control the Bluetooth radio and external interfaces. A 16-bit RISC microcontroller is used for low power consumption and efficient use of memory.

6.2 Memory

CSR1021 QFN memory includes:

- RAM Code and Data (Internal)
- ROM (Internal)
- OTP (Internal)
- MTP (Internal)
- SPI flash from system generated 3 V rail (External) (Optional)

Memory spaces include:

- Application Store: A storage area for customer applications, located in internal OTP or internal/external SPI flash.
- Configuration Store: An area of memory used to store configuration settings (ROM, OTP, MTP, RAM, SPI flash).
- User Store: OTP (programmable once then read-only), MTP (multiple-time programmable) and SPI flash data storage available to user applications at runtime.

6.2.1 RAM Code and Data (Internal)

CSR1021 QFN has RAM for code and data.

NOTE Either RAM is available for either code or data.

Code RAM

- 64 KB
- Primary use for developing applications for eventual storage in OTP memory
- Can be used as a cache for applications stored in flash or OTP memory
- Can be used as code or data RAM if not used as a code cache
- Software provides details of the area of shared RAM to the user application
- Part or all of the code RAM is powered down to save power when not in use

Data RAM

- 16 KB
- Primary use for firmware and applications
- The use of all data RAM for executing code is possible (although there are some restrictions on when this can be done)

6.2.2 ROM (Internal)

192 KB of internal ROM is available for system firmware implementation.

NOTE Code executes from ROM and RAM.

6.2.3 OTP (Internal)

60 KB of OTP is available for storage of user applications:

- One-time programmable
- Enables reading and writing of information to the configuration store
- Enables downloading of software
- Has a storage provider driver
- PMU supplies power

6.2.4 MTP (Internal)

256 Bytes of MTP is an internal NVM where applications can store configuration data (for example, Bluetooth addresses and Link Keys):

- 10,000 erase/write cycles
- Multiple-time programmable

6.2.5 SPI Flash (External) from System Generated 2.5 to 3.3 V Rail

Up to 16 MB of dedicated flash (External) memory is available via a dedicated SPI interface:

- SPI flash rail powered from VDD_MEM at 2.5 to 3.3 V or VDD_BAT directly.
- Signalling PIOs are powered from:
  - VDD_MEM: Dedicated PIO[36:33]
  - VDD_PADS: Other PIOs

NOTE Signalling voltages must be compatible with the way that CSR1021 QFN and the flash chip are powered.

6.2.6 SPI Flash (External) (Optional)

Up to 16 MB of flash (External) memory can be made available via a serial memory flash controller interface:

- Applications can be downloaded to the external flash using OTA: An update mechanism for a remote host to download an application to the IC via a Bluetooth low energy technology link
- Flash access speed is the same as the attached crystal: 16 or 32 MHz
- A functional mode operation can fetch program code from the flash for caching
- External flash memory pads are multiplexed with PIOs and support serial, quad SPI flash and dual-IO access modes

6.2.6.1 Serial Memory Controller

CSR1021 QFN supports single-IO, dual-IO and quad-IO flash access and provides the following pins attached to a dedicated SQIF interface for external SPI flash:

- SPI_FLASH_CLK (Serial Clock Input)
- SPI_FLASH_CS# (Chip Select Input)
- SPI_FLASH_IO[0] (Data Input (Data Input/Output 0))
- SPI_FLASH_IO[1] (Data Output (Data Input/Output 1))
- SPI_FLASH_IO[2] (Write Protect Input (Data Input/Output 2))
- SPI_FLASH_IO[3] (Hold Input (Data Input/Output 3))

NOTE The SPI flash rail is powered from VDD_MEM at 2v5 to 3v3 or VDD_BAT directly.

SPI_FLASH_IO[2] and SPI_FLASH_IO[3] are mode-dependent and are not required for single-IO or dual-IO access modes.

7 Peripheral Interfaces

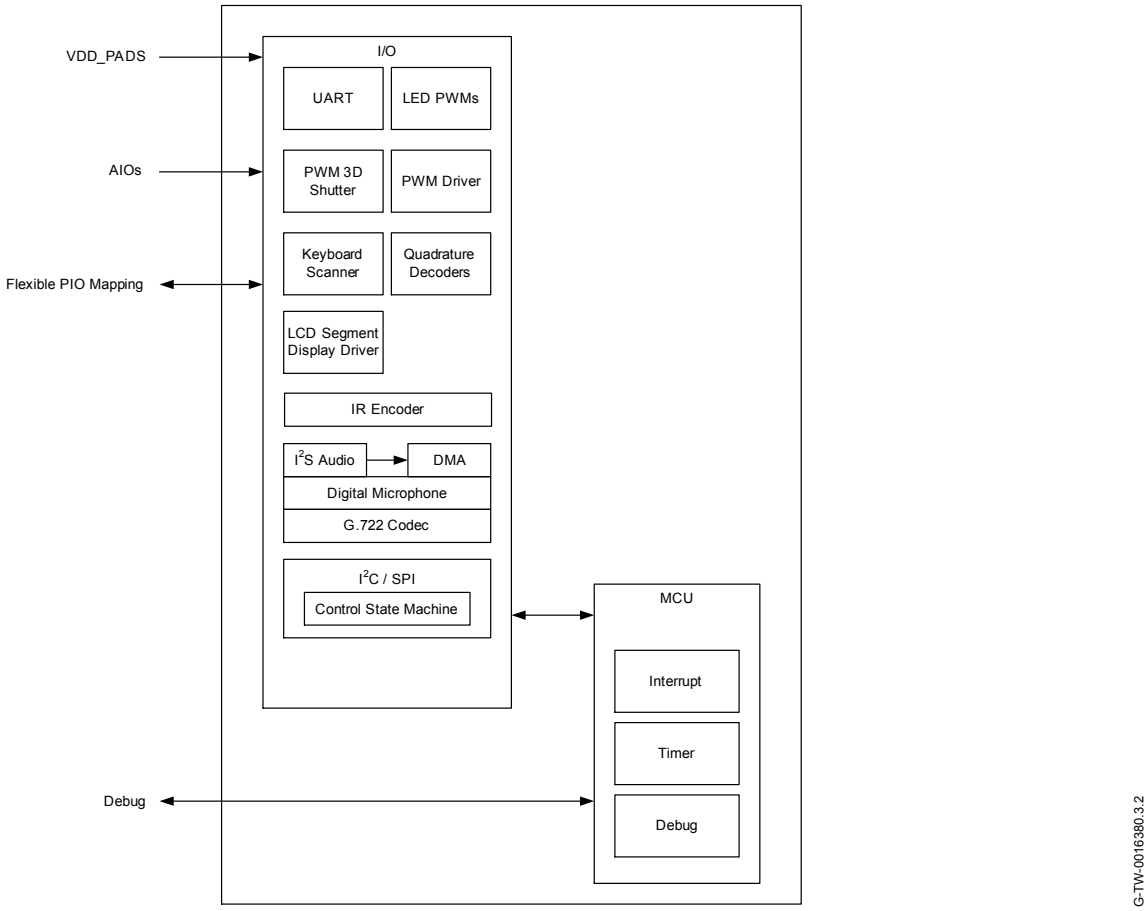


Figure 7-1 Peripheral Interfaces Block Diagram

7.1 I²C Master/Slave (General)

CSR1021 QFN has 1 I²C master/slave general interface for communication with external peripherals and sensors:

- Maximum clock speed 1 MHz
- Data transmiting/receiving of variable byte length
- 7-bit and 10-bit addressing modes
- Configurable:
  - PIO pins for SCL and SDA
  - I²C clock: 100 kHz default (software-configurable) at 1:1 duty-cycle (asymmetric if required)
  - Supports slave clock stretching
  - CSR1021 QFN is Fast Mode and Fast Mode+ compatible.

NOTE Strong pull is sufficient for I²C on all PIO pads.

7.2 SPI Master/Slave (General)

CSR1021 QFN has 1 SPI master/slave general interface for communication with other devices.

It supports:

- SPI master and slave
- All 4 modes supported
- 2 methods of transferring data to memory:
  - DMA to/from memory:
    - 8-bit or 16-bit word size
    - Big and little-endian
  - Software reads and writes to FIFOs: variable from 1 to 16 bits
- Interrupt callbacks to processor allow SPI as a slave to indicate that it requires service
- Deep sleep mode (depending on clock)

Figure 7-2 shows a simple SPI timing diagram.

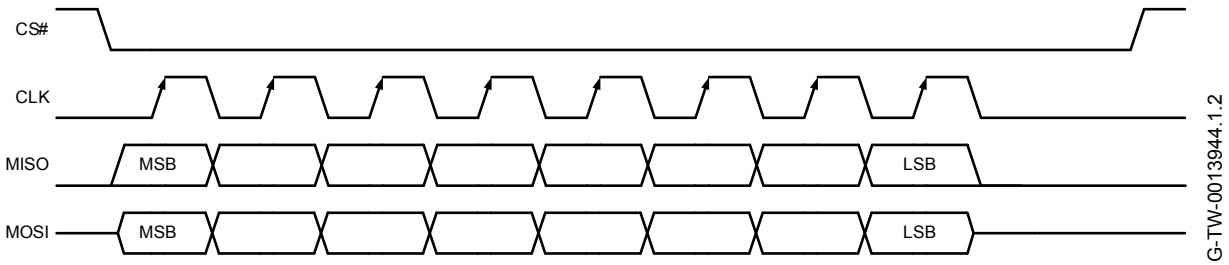


Figure 7-2 SPI Timing Diagram

7.3 SPI Debug Interface (QTIL Proprietary)

NOTE The CSR1021 QFN debug SPI interface is available in SPI slave mode to enable an external MCU to program and control the CSR1021 QFN, generally via libraries or tools supplied by QTIL. The protocol of this interface is proprietary. A 128-bit lock key secures application code. The 4 SPI debug lines directly support this function on PIO[3:0].

The SPI programs, configures and debugs the CSR1021 QFN. It is required in production. Ensure the 4 SPI signals are brought out to either test points or a header with SPI_PIO#.

Take SPI_PIO# high to enable the SPI debug feature on PIO[3:0].

CSR1021 QFN uses a 16-bit data and 16-bit address programming and debug interface. Transactions occur when the internal processor is running or is stopped.

Data is written or read one word at a time, or the auto-increment feature is available for block access.

7.3.1 Instruction Cycle

The CSR1021 QFN is the slave and receives commands on DEBUG_MOSI and outputs data on DEBUG_MISO. Table 7-1 shows the instruction cycle for an SPI transaction.

Table 7-1 Instruction Cycle for an SPI Transaction

1	Reset the SPI interface	Hold DEBUG_CS# high for 2 DEBUG_CLK cycles
2	Write the command word	Take DEBUG_CS# low and clock in the 8-bit command
3	Write the address	Clock in the 16-bit address word
4	Write or read data words	Clock in or out 16-bit data word(s)
5	Termination	Take DEBUG_CS# high

With the exception of reset, DEBUG_CS# must be held low during the transaction. Data on DEBUG_MOSI is clocked into the CSR1021 QFN on the rising edge of the clock line DEBUG_CLK. When reading,CSR1021 QFN replies to the master on DEBUG_MISO with the data changing on the falling edge of the DEBUG_CLK. The master provides the clock on DEBUG_CLK. The transaction is terminated by taking DEBUG_CS# high.

The auto increment operation on the CSR1021 QFN cuts down on the overhead of sending a command word and the address of a register for each read or write, especially when large amounts of data are to be transferred. The auto increment offers increased data transfer efficiency on the CSR1021 QFN. To invoke auto increment, DEBUG_CS# is kept low, which auto increments the address while providing an extra 16 clock cycles for each extra word written or read.

7.3.2 Multi-slave Operation

Do not connect the CSR1021 QFN in a multi-slave arrangement by simple parallel connection of slave MISO lines. When CSR1021 QFN is deselected (DEBUG_CS# = 1), the DEBUG_MISO line does not float. Instead, CSR1021 QFN outputs 0 if the processor is running or 1 if it is stopped.

7.4 UART (General)

The CSR1021 QFN UART interface provides a simple mechanism to communicate with other serial devices using the RS232 protocol.

Table 7-2 lists the 4 signals that implement the UART function in CSR1021 QFN.

Table 7-2 UART Signals

Signal	Description
UART_RX	Pin to receive UART data from another device
UART_TX	Pin to transmit UART data to another device
UART_CTS	Pin to notify another device that CSR1021 QFN is ready to receive data (active low input)
UART_RTS	Pin to notify other device that CSR1021 QFN is ready to send data (active low output)

7.4.1 UART Configuration Settings

UART configuration parameters, e.g. baud rate and data format, are set using CSR1021 QFN firmware.

NOTE To communicate with the UART at its maximum data rate using a standard PC, the PC requires an accelerated serial port adapter card.

Table 7-3 lists UART configuration settings for CSR1021 QFN.

Table 7-3 UART Configuration Settings

Parameter		Possible Values
Baud rate	Minimum	1200 baud (≤2 % Error)
		9600 baud (≤1 % Error)
	Maximum (XTAL)	1 Mbaud (≤1 % Error)
Parity		None, Odd or Even
Number of stop bits		1 or 2
Bits per byte		8

7.4.2 UART Configuration While In Deep Sleep

The maximum baud rate is 2400 baud during deep sleep.

7.5 PWMs

CSR1021 QFN has 5 independently configurable PWM instances.

A multipurpose PWM generator provides 3 modes:

- Normal PWM mode:
  - For motor control and general purpose PWM
- 3D Shutter mode:
  - For 3D shutter control
  - Cycle accurate
  - 16-bit resolution for all the configuration registers to be specified in clock cycles
  - New configuration applied on update register write or at a specific time (e.g. in response to radio traffic)
  - Variable offset after the reconfiguration can be applied
  - Configurable width of the external sync pulses
- LED mode:
  - For LED fading

7.5.1 3D Shutter Control PWM

CSR1021 QFN has a 3D shutter control PWM that is cycle accurate and can be used for driving 3D TV glasses. It has 16-bit resolution for all configuration registers to be specified in the clock cycles:

- Time On: For shutter on period
- Time Period: For shutter period
- Time Offset: Applied at a specific time (e.g. in response to radio traffic)

NOTE A new configuration is applied on the TV sync pulse or controlled on the sync register write.

7.5.2 LED Control PWM

CSR1021 QFN has 4 LED mode PWM blocks (2 x fast / 2 x slow). Each LED mode PWM has an 8-bit resolution for all configuration registers and a:

- Minimum brightness duty cycle (grouped in a 16-bit wide register)
- Maximum brightness duty cycle (grouped in a 6-bit wide register)
- Hold Minimum and Maximum time (grouped in a 16-bit wide register)
- Step (ramp) time
- Brightness configuration specified in units of typically 30 µs assuming a 32 kHz clock
- Hold times specified in units of typically 16 ms assuming a 32 kHz clock
- Step time specified in units of typically 1 ms assuming a 32 kHz clock

NOTE CSR1021 QFN supports immediate reconfiguration on the sync register write.

7.6 LCD Glass Driver

CSR1021 QFN's LCD driver has the following features:

- Drives simple static and multiplexed LCD glass with no requirement for external components.
- Capable of controlling PIO pads to support bias modes:
  - Normal: Switching between GND and VCC
  - 1/2 bias: Switching between GND, 1/2 VCC and VCC
  - 1/3 bias: Switching between GND, 1/3 VCC, 2/3 VCC and VCC
- Up to 28 segments and 4 common (backplane) driver outputs
- Configurable to support non-multiplexed (static) and 2, 3 or 4 way multiplexed LCD glass
- Supports LCD glass with up to 112 display segments (4x the number of segment driver outputs)

NOTE Unused segment outputs that can be disabled.

- LCD blanking support: Enables flashing of all segments at slow (typically 2 Hz) frequency
- LCD segment blinking support: Up to 2 segments can be configured to blink at slow frequency (typically 2 Hz)
- Flexible input clock pre-scaler to support required clock frequencies for different multiplexing modes and LCD glass characteristics.

- Ultra-low power operation to maintain LCD display with only low frequency clock input (typically 32 kHz)
- LCD clock output for pad drivers to increase output pad drivers when LCD output changes.
- Contrast control

7.7 Key Scanner

CSR1021 QFN has 1 key scanner for applications such as mouse and keyboard HID.

Figure 7-3 shows an example keyboard matrix at a size of 3 x 2 (PIO drive lines x PIO sense lines respectively).

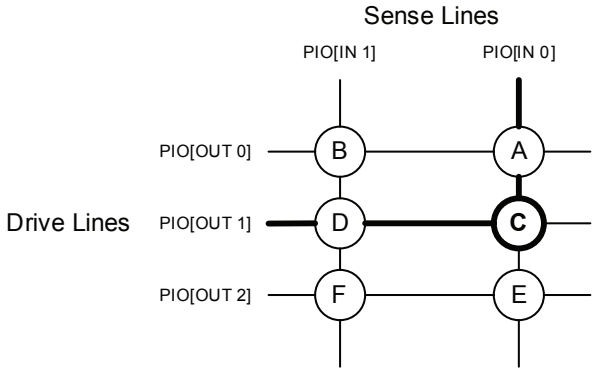


Figure 7-3 Example Keyboard Matrix 3x2 Size

Physical buttons are located on line crossings A to F. If a button is pressed both lines become connected. Assuming sense lines are pulled-up by internal logic, a key press, for example C can be detected by forcing PIO[OUT 1] low and reading 0 on PIO[IN 0].

It supports:

- Keypad matrix up to 12 PIO inputs (sense lines) and 18 PIO outputs (drive lines):
  - Drives 1 to 18 drive lines consecutively
  - 12-bit key registers updated every scan
- Press and release events reported to the host via callback
- Variable scan rate:
  - By default drives consecutive drive lines every clock cycle
  - Configurable number of clocks per drive line

NOTE The key scanner does not support ghost key removal.

The key scanner configuration and control includes:

- PIO pin numbers to be used for drive and sense lines
- Scan rate, Hz and active/idle ratio
- Hardware starting and stopping
- Callback creation to receive keyboard map data.

7.8 Quadrature Decoders

CSR1021 QFN has 4 quadrature decoders with:

- Each having a configurable simple filter on inputs (for debouncing)
- Enabling and disabling of single or multiple decoders
- Data reading functionality
- Processor interrupt generation

7.9 Infrared Output

CSR1021 QFN has 1 IR output for applications such as infrared remote control. It can run from Fast XTAL and Intermediate clocks.

7.10 Audio

Figure 7-4 shows CSR1021 QFN audio.

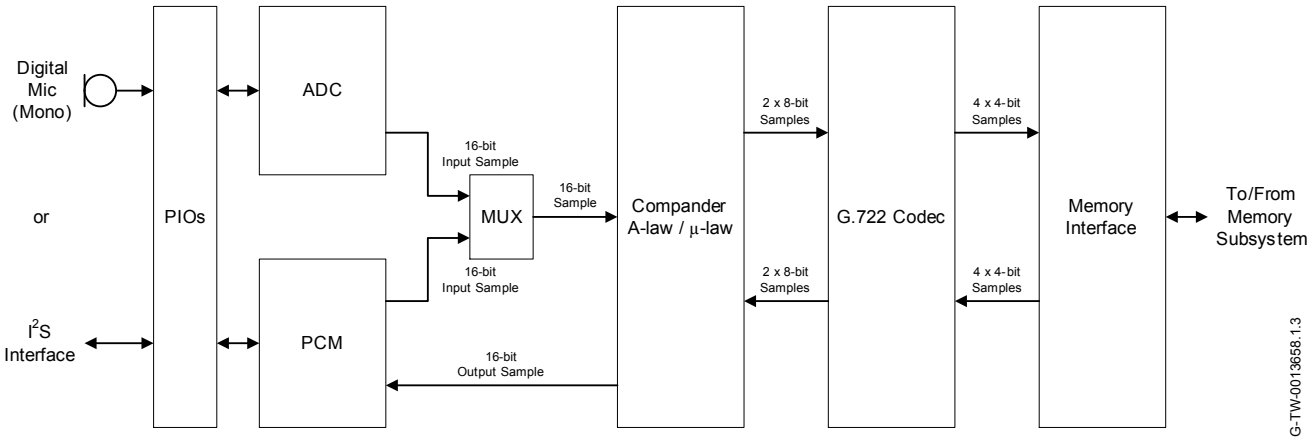


Figure 7-4 CSR1021 QFN Audio

NOTE Digital microphone and I²S input cannot be active at the same time.

G.722 codec cannot encode and decode at the same time.

7.10.1 Digital Microphone

CSR1021 QFN has 1 digital microphone input with:

- 1 or 2 Mbps sample rate
- Software selectable as left or right channel
- G.722 encoder or bypass option
- Audio routed to firmware only (not to I²S)
- Software supporting DMIC clock frequencies of 500 kHz, 1 MHz, 2 MHz, and 4 MHz

7.10.2 G.722 Codec

CSR1021 QFN has a G.722 Codec, featuring:

- Output: 48 kbps (optional 56 or 64 kbps)
- Input: 16 kHz/16-bits (optional 8 kHz/8-bits, 8 kHz/16-bits and 16 kHz/8-bits)
- Output produces 20 Byte blocks for easy GATT streaming

NOTE Analogue audio is not provided.

7.11 10-bit Aux ADC

CSR1021 QFN has 1 10-bit Aux ADC:

- A resistive SAR ADC
- Attached to 2 AIO pads
- The processor has access to its ADC result value after exit from Deep Sleep mode
- The ADC reference is VDD_AUX, see Figure 7-5.

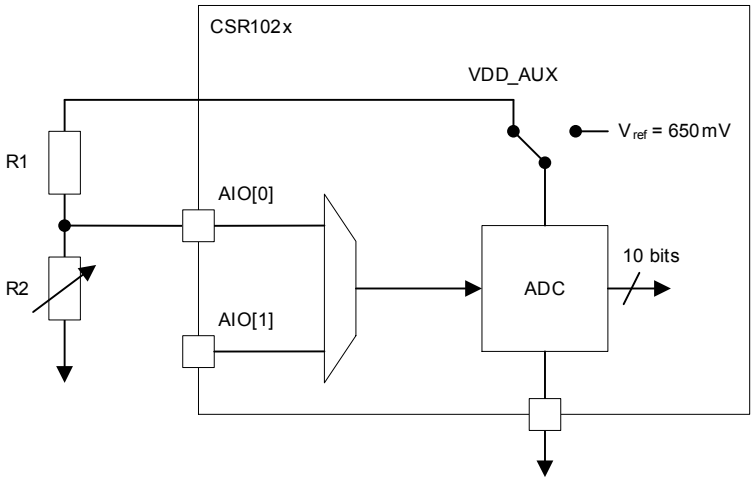


Figure 7-5 10-bit Aux ADC Reference

NOTE Figure 7-5 shows an additional internal 650 mV reference. This is for QTIL test purposes only.

The 10-bit Aux ADC is not available during XTAL startup or battery voltage and temperature monitoring. Therefore the time to perform a conversion may be longer if the hardware is already using the ADC.

8 Auxiliary Features

8.1 Battery Monitor

CSR1021 QFN contains an internal battery monitor that reports the battery voltage to the software.

8.2 Temperature Sensor

CSR1021 QFN contains a temperature sensor that measures the temperature of the die and can report the chip temperature in °C or Kelvin using a firmware API.

9 Programmable I/O Ports, PIO and AIO

This section describes CSR1021 QFN programmable I/O ports, PIO and AIO.

9.1 General PIOs

32 lines of programmable bidirectional I/O are provided:

- May be set by the application code or used as an input or to wake the chip.
- Software-configurable as weak pull-up, weak pull-down, strong pull-up or strong pull-down.
- At reset all lines are inputs with weak pull-down.
- Pull strength, direction and pad states preserved across all non-off states to support waking on any PIO (even when VDD_DIG is powered down). Configurable to wake CSR1021 QFN via an individually selectable mask for rising, falling or any edge transition from Deep Sleep modes.
- Available as interrupt request lines.
- Powered from VDD_PADS

NOTE VDD_PADS must remain powered.

QTIL cannot guarantee that the PIO assignments remain as described. Implementation of the PIO lines is firmware build-specific, for more information see the relevant software release note.

9.2 Static PIOs

5 lines of static programmable bidirectional I/O are provided PIO[36:32]:

- PIO[36:33]:
  - Attached to a dedicated SQIF interface for external SPI flash.
  - Powered from VDD_MEM.
- PIO[32]:
  - May be set by the application code or used as an input.
  - Software-configurable as weak pull-up, weak pull-down, strong pull-up or strong pull-down.
  - At reset all lines are inputs with weak pull-down.
  - Pull strength, direction and pad states preserved across all non-off states to support waking on any PIO (even when VDD_DIG is powered down). Configurable to wake CSR1021 QFN via an individually selectable mask for rising, falling or any edge transition from Deep Sleep: No RAM Retention and External Interrupts Enabled, Deep Sleep: 16 KB Data RAM Retention or Deep Sleep: 16 KB Data RAM and 64 KB RAM Retention mode.
  - Powered from VDD_PADS

NOTE VDD_PADS must remain powered.

QTIL cannot guarantee that the PIO assignments remain as described. Implementation of the PIO lines is firmware build-specific, for more information see the relevant software release note.

9.3 AIOs

CSR1021 QFN has 2 pins providing unidirectional analogue programmable input lines, AIO[1:0].

NOTE These pins do not provide an output capability.

9.4 Digital Pin States on Initial Power Up

Table 9-1 shows the pin states of CSR1021 QFN on initial power up. Pull-Up and Pull-Down default to weak values unless specified otherwise.

Table 9-1 Pin States on Initial Power Up

Pin Name / Group	On Initial Power Up
PIO[35]	Strong Pull-Up
SPI_PIO#	Strong Pull-Down
All other PIOs	Weak Pull-Down

9.5 LCD Glass Mid-rail Drive

CSR1021 QFN supports direct LCD glass driving by internally generating required voltage for one of the following modes of operation:

- ½ mode
- ⅓ and ⅔ mode

Voltage levels are generated and routed internally to the I/O pads configured for LCD glass driving.

NOTE Only a single mode of operation is available.

Hardware supports up to 4 common lines and 32 segment lines. For more information on supported modes of operation, see *CSR1021 QFN Software Release Notes*.

9.6 Analogue Properties of the PIO

Most CSR1021 QFN PIOs can route in an analogue signal that can be digitised using the 10-bit Aux ADC.

NOTE This feature may not be available in the current firmware. For information on support status, see *CSR1021 QFN Software Release Notes*.

9.7 PIO Configuration Options

PIO Pin	External Serial Flash[a]	Digital Microphone	I²S	I²C Master Only	SPI		Debug SPI	H4 UART		Quadrature Decoder Input[b]		LCD		LED/ PWM [c]	KeyScan		IR Encoder (Output)	GSIU					Radi	
					Slave Only	Inc Master		Data	Flow	A	B	Common	Segment		Drive	Sense		TX	RX	EXT TMR CTR	ANA MON CLK	EXT CLK OUT	RX EN Debug	RX ADC (SDDRC)
PIO[36]	SPI_FLASH_CLK	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
PIO[35]	SPI_FLASH_CS#	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
PIO[34]	SPI_FLASH_IO[0]	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
PIO[33]	SPI_FLASH_IO[1]	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
PIO[32]	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
PIO[31]	-	MIC_CLK_OUT	I2S_WS	SDA	CLK, CS, SDA	DATA	-	RX	CTS	Y	Y	COM3	Y	Y	Y	Y	Y	-	Y	Y	Y	Y	Y	Y
PIO[30]	SPI_FLASH_CLK	MIC_DATA_IN	I2S_CLK	SCL	CLK, CS, SDA	DATA	-	TX	RTS	Y	Y	COM2	Y	Y	Y	Y	Y	Y	-	Y	Y	Y	Y	Y
PIO[29]	SPI_FLASH_CS#	MIC_CLK_OUT	I2S_DATA	SDA	CLK, CS, SDA	DATA	-	RX	CTS	Y	Y	COM1	Y	Y	Y	Y	Y	-	Y	Y	Y	Y	Y	Y
PIO[28]	SPI_FLASH_IO[0]	MIC_DATA_IN	-	SCL	CLK, CS, SDA	DATA	-	TX	RTS	Y	Y	COM0	7	Y	Y	Y	Y	Y	-	Y	Y	Y	Y	Y
PIO[27]	SPI_FLASH_IO[1]	MIC_CLK_OUT	-	SDA	CLK, CS, SDA	DATA	-	RX	CTS	Y	Y	COM3	Y	Y	Y	Y	Y	-	Y	Y	Y	Y	Y	Y
PIO[26]	-	MIC_DATA_IN	-	SCL	CLK, CS, SDA	DATA	-	TX	RTS	Y	Y	COM2	Y	Y	Y	Y	Y	Y	-	Y	Y	Y	Y	Y
PIO[25]	-	MIC_CLK_OUT	I2S_WS	SDA	CLK, CS, SDA	DATA	-	RX	CTS	Y	Y	COM1	Y	Y	Y	Y	Y	-	Y	Y	Y	Y	Y	Y
PIO[24]	-	MIC_DATA_IN	I2S_CLK	SCL	CLK, CS, SDA	DATA	-	TX	RTS	Y	Y	COM0	6	Y	Y	Y	Y	Y	-	Y	Y	Y	Y	Y
PIO[23]	-	MIC_CLK_OUT	I2S_DATA	SDA	CLK, CS, SDA	DATA	-	RX	CTS	Y	Y	COM3	Y	Y	Y	Y	Y	-	Y	Y	Y	Y	Y	Y
PIO[22]	-	MIC_DATA_IN	-	SCL	CLK, CS, SDA	DATA	-	TX	RTS	Y	Y	COM2	Y	Y	Y	Y	Y	Y	-	Y	Y	Y	Y	Y
PIO[21]	-	MIC_CLK_OUT	-	SDA	CLK, CS, SDA	DATA	-	RX	CTS	Y	Y	COM1	Y	Y	Y	Y	Y	-	Y	Y	Y	Y	Y	Y
PIO[20]	-	MIC_DATA_IN	-	SCL	CLK, CS, SDA	DATA	-	TX	RTS	Y	Y	COM0	5	Y	Y	Y	Y	Y	-	Y	Y	Y	Y	Y
PIO[19]	-	MIC_CLK_OUT	I2S_WS	SDA	CLK, CS, SDA	DATA	-	RX	CTS	Y	Y	COM3	Y	Y	Y	Y	Y	-	Y	Y	Y	Y	Y	Y
PIO[18]	-	MIC_DATA_IN	I2S_CLK	SCL	CLK, CS, SDA	DATA	-	TX	RTS	Y	Y	COM2	Y	Y	Y	Y	Y	Y	-	Y	Y	Y	Y	Y
PIO[17]	-	MIC_CLK_OUT	I2S_DATA	SDA	CLK, CS, SDA	DATA	-	RX	CTS	Y	Y	COM1	Y	Y	Y	Y	Y	-	Y	Y	Y	Y	Y	Y
PIO[16]	SPI_FLASH_IO[3]	MIC_DATA_IN	-	SCL	CLK, CS, SDA	DATA	-	TX	RTS	Y	Y	COM0	4	Y	Y	Y	Y	Y	-	Y	Y	Y	Y	Y
PIO[15]	SPI_FLASH_IO[2]	MIC_CLK_OUT	-	SDA	CLK, CS, SDA	DATA	-	RX	CTS	Y	Y	COM3	Y	Y	Y	Y	Y	-	Y	Y	Y	Y	Y	Y
PIO[14]	-	MIC_DATA_IN	-	SCL	CLK, CS, SDA	DATA	-	TX	RTS	Y	Y	COM2	Y	Y	Y	Y	Y	Y	-	Y	Y	Y	Y	Y
PIO[13]	-	MIC_CLK_OUT	I2S_WS	SDA	CLK, CS, SDA	DATA	-	RX	CTS	Y	Y	COM1	Y	Y	Y	Y	Y	-	Y	Y	Y	Y	Y	Y
PIO[12]	-	MIC_DATA_IN	I2S_CLK	SCL	CLK, CS, SDA	DATA	-	TX	RTS	Y	Y	COM0	3	Y	Y	Y	Y	Y	-	Y	Y	Y	Y	Y
PIO[11]	-	MIC_CLK_OUT	I2S_DATA	SDA	CLK, CS, SDA	DATA	-	RX	CTS	Y	Y	COM3	Y	Y	Y	Y	Y	-	Y	Y	Y	Y	Y	Y
PIO[10]	-	MIC_DATA_IN	-	SCL	CLK, CS, SDA	DATA	-	TX	RTS	Y	Y	COM2	Y	Y	Y	Y	Y	Y	-	Y	Y	Y	Y	Y
PIO[9]	SPI_FLASH_IO[3]	MIC_CLK_OUT	-	SDA	CLK, CS, SDA	DATA	-	RX	CTS	Y	Y	COM1	Y	Y	Y	Y	Y	-	Y	Y	Y	Y	Y	Y
PIO[8]	SPI_FLASH_IO[2]	MIC_DATA_IN	-	SCL	CLK, CS, SDA	DATA	-	TX	RTS	Y	Y	COM0	2	Y	Y	Y	Y	Y	-	Y	Y	Y	Y	Y
PIO[7]	SPI_FLASH_CLK	MIC_CLK_OUT	I2S_WS	SDA	CLK, CS, SDA	DATA	-	RX	CTS	Y	Y	COM3	Y	Y	Y	Y	Y	-	Y	Y	Y	Y	Y	Y
PIO[6]	SPI_FLASH_CS#	MIC_DATA_IN	I2S_CLK	SCL	CLK, CS, SDA	DATA	-	TX	RTS	Y	Y	COM2	Y	Y	Y	Y	Y	Y	-	Y	Y	Y	Y	Y
PIO[5]	SPI_FLASH_IO[0]	MIC_CLK_OUT	I2S_DATA	SDA	CLK, CS, SDA	DATA	-	RX	CTS	Y	Y	COM1	Y	Y	Y	Y	Y	-	Y	Y	Y	Y	Y	Y
PIO[4]	SPI_FLASH_IO[1]	MIC_DATA_IN	-	SCL	CLK, CS, SDA	DATA	-	TX	RTS	Y	Y	COM0	1	Y	Y	Y	Y	Y	-	Y	Y	Y	Y	Y
PIO[3]	-	MIC_CLK_OUT	I2S_WS	SDA	CLK, CS, SDA	DATA	Y	RX	CTS	Y	Y	COM3	Y	Y	Y	Y	Y	-	Y	Y	Y	Y	Y	Y
PIO[2]	-	MIC_DATA_IN	I2S_CLK	SCL	CLK, CS, SDA	DATA	Y	TX	RTS	Y	Y	COM2	Y	Y	Y	Y	Y	Y	-	Y	Y	Y	Y	Y
PIO[1]	-	MIC_CLK_OUT	I2S_DATA	SDA	CLK, CS, SDA	DATA	Y	RX	CTS	Y	Y	COM1	Y	Y	Y	Y	Y	-	Y	Y	Y	Y	Y	Y
PIO[0]	-	-	-	SCL	CLK, CS, SDA	DATA	Y	TX	RTS	Y	Y	COM0	0	Y	Y	Y	Y	Y	-	Y	Y	Y	Y	Y

Notes:

[a] Padset groups include: 0 = PIO [36:33], 1 = PIO[9:4], 2 = PIO[30:27, 16:15]. Only one Padset group can be configured at a time. Firmware does not allow pads in different groups to be mixed.

[b] Quadrature Decoder Input A and B both require 4 PIOs to be assigned.

[c] LED/PWM require 5 PIOs to be assigned to access all functionality.

Figure 9-1 CSR1021 QFN PIO Configuration Options

10 CSR1021 QFN Software Stack

CSR1021 QFN is supplied with Bluetooth v4.2 specification compliant stack firmware. Figure 10-1 shows that the CSR1021 QFN software architecture enables the Bluetooth processing and the application program to run on the internal RISC MCU .

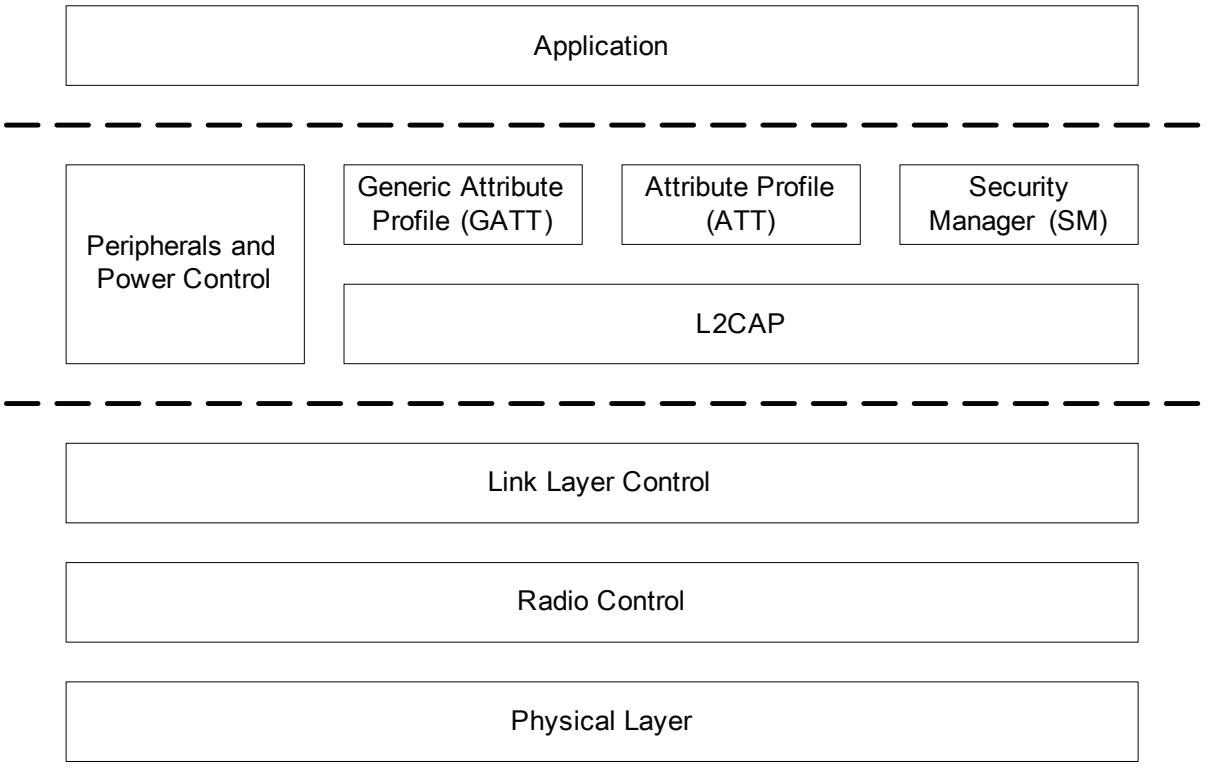


Figure 10-1 Software Architecture

11 Power Control and Regulation

CSR1021 QFN contains a switch-mode regulator that generates all the supply rails required from the battery.

11.1 Switch-mode Regulator

The switch-mode regulator generates the main rail from the battery supply, VDD_BAT.

The switch-mode regulator generates all required voltage rails for the system to operate using only a single inductor. No user intervention is required because the regulator automatically changes from buck to boost mode depending on the battery voltage and output voltage of the rail(s).

11.2 Reset

CSR1021 QFN is reset by:

- Power-on reset
- Software-configured watchdog timer

NOTE VDD_BAT input voltage must drop to 0.4 V to guarantee a rising VDD_BAT is seen by the PMU on reassertion.

VDD_BAT takes approximately 20 s to drop to 0 V when power is removed due to circuit decoupling capacitance.

To fully reset the PIO pads take all VDD_MEM and VDD_PADS pins below 0.4 V.

13 CSR1021 QFN Example Application Schematic

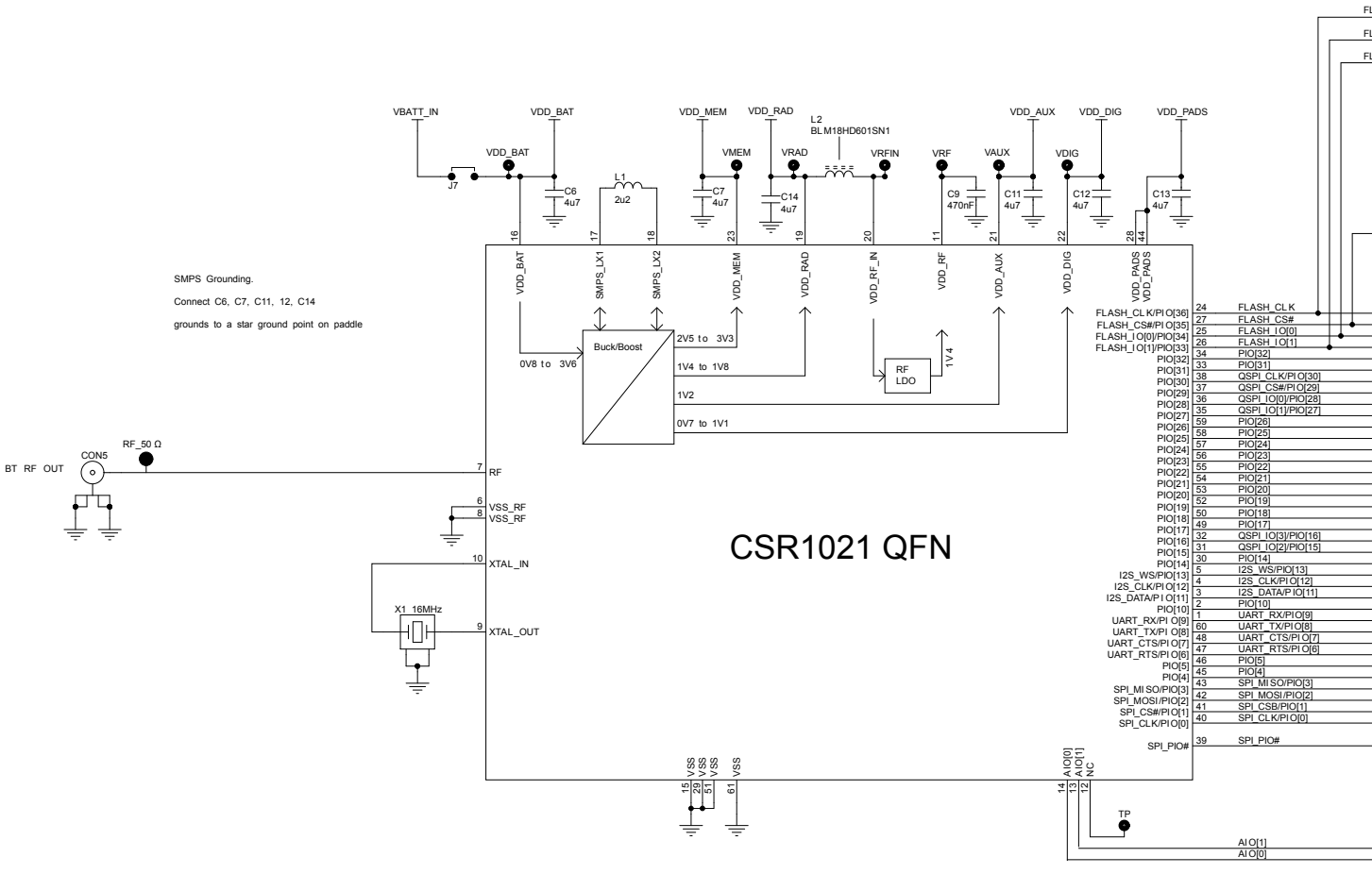


Figure 13-1 CSR1021 QFN Example Application Schematic

14 Electrical Characteristics

14.1 Absolute Maximum Ratings

NOTE Exceeding absolute maximum ratings causes permanent damage to the CSR1021 QFN.

Exposure to any absolute maximum rating for extended periods of time affects reliability.

Table 14-1 CSR1021 QFN Absolute Maximum Ratings

Rating	Min	Typ	Max	Unit
Storage temperature	-40	-	85	°C
Battery (VDD_BAT and VDD_PADS)	0	-	3.6	V
I/O supply voltage	0	-	3.6	V
VDD_AUX, VDD_DIG, AIOs	0	-	1.26	V
VDD_RAD, VDD_RF_IN, VDD_RF	0	-	2.2	V
XTAL_IN, XTAL_OUT	0	-	0.8	V

14.2 Recommended Operating Conditions

Use the CSR1021 QFN recommended operating conditions to ensure optimum performance and reliability.

Table 14-2 CSR1021 QFN Recommended Operating Conditions

Operating Condition	Min	Typ	Max	Unit
Operating temperature range	-30	20	85	°C
Battery (VDD_BAT)	0.9	3.0	3.6	V
I/O supply voltage (VDD_PADS)	1.2	3.0	3.6	V

14.3 Input/Output Terminal Characteristics

Always comply with the stated values when attaching external components to the CSR1021 QFN.

NOTE Current drawn by a pin is positive (+ve), current supplied is negative (-ve).

14.3.1 Switch-mode Regulator

Table 14-3 CSR1021 QFN Switch-mode Regulator

Switch-mode Regulator	Min	Typ	Max	Unit
Output voltage (VDD_AUX)(1)	-	1.2	-	V
Output voltage (VDD_DIG)(1)	-	1.1	-	V

Table 14-3 CSR1021 QFN Switch-mode Regulator (Continued)

Switch-mode Regulator	Min	Typ	Max	Unit
Output voltage (VDD_RAD)[1]	-	1.8	-	V
Output voltage (VDD_MEM)	-	3.3	-	V
Normal Operation				
Output current (I_{max}) (MEM)	-	-	12	mA

NOTE 1. These are internal regulators and should have no additional load connected.

14.3.2 RF Linear Regulator

Table 14-4 CSR1021 QFN RF Linear Regulator

Normal Operation	Min	Typ	Max	Unit
Input voltage (VDD_RF_IN)	1.2	-	2.2	V
Output voltage (VDD_RF)	1.0	-	2.0	V

NOTE This regulator is for QTIL internal use only of the RF rail.

14.3.3 Digital I/O Terminals

Table 14-5 CSR1021 QFN Input Voltage Levels

Input Voltage Levels	Min	Typ	Max	Unit
V_{IL} input logic level low	-	-	25% x VDD_PADS	V
V_{IH} input logic level high	75% x VDD_PADS	-	-	V

Table 14-6 CSR1021 QFN Output Voltage Levels

Output Voltage Levels	Min	Typ	Max	Unit
V_{OL} output logic level low, I_{OL} = 8.0 mA (Max Drive Strength)	-	-	20% x VDD_PADS	V
V_{OH} output logic level high, I_{OL} = -8.0 mA (Max Drive Strength)	80% x VDD_PADS	-	-	V
T_r/T_f (for 30 pF load)	-	-	2	ns

Table 14-7 CSR1021 QFN Input and Tristate

Input and Tristate	Min	Typ	Max	Unit
With strong pull-up	3.5	4.7	6.0	kΩ
With strong pull-down	3.5	4.7	6.0	kΩ
With weak pull-up(1)	8	40	50	µA
With weak pull-down(1)	10	40	50	µA
C_I input capacitance	-	5	-	pF

NOTE 1. Range applicable for VDD_PADS between 1.8 V and 3.3 V when measured as a short circuit.

14.3.4 AIO

Table 14-8 CSR1021 QFN AIO

Input/Output Voltage Levels	Min	Typ	Max	Unit
Input voltage	0	-	VDD_AUX	V

14.3.4.1 10-bit Aux ADC

Table 14-9 CSR1021 QFN 10-bit Aux ADC

10-bit Aux ADC	Min	Typ	Max	Unit
Resolution	-	-	10	Bits
Input voltage range(1)	0	-	VDD_AUX	V
Input bandwidth	-	100	-	kHz
Conversion time	1.38	1.69	4.14	µs
Sample rate(2)	-	-	700	Samples/s

NOTE 1. LSB size = VDD_AUX/1023.

2. The 10-bit Aux ADC is accessed through the firmware API. The sample rate given is achieved as part of this function.

14.4 ESD Protection

Apply ESD static handling precautions during manufacturing.

Table 14-10 shows the ESD handling maximum ratings.

Table 14-10 CSR1021 QFN ESD Handling Ratings

Condition	Class	Max Rating
Human Body Model Contact Discharge per JEDEC EIA /JS-001-2014	1C	2 kV (all pins except RF rated at 1 kV)(1)
Charged Device Model Contact Discharge per JEDEC EIA /JS002-2014	C1	500 V (all pins)(1)

NOTE 1. This value is preliminary and may be subject to change.

15 Current Consumption

Table 15-1 shows CSR1021 QFN total typical current consumption measured at the battery.

Table 15-1 Current Consumption

Mode	Description	Total Typical Current at 3 V
Deep Sleep: No RAM Retention and External Interrupts Enabled	All functions are shut down. To wake the chip, toggle a pre-configured PIO.	1.6 µA
Deep Sleep: No RAM Retention with External Interrupts and Timer Enabled	VDD_PADS = ON VDD_BAT = ON	5.5 µA
Deep Sleep: 16 KB Data RAM Retention	VDD_PADS = ON VDD_BAT = ON RAM = ON Digital Circuits = ON SMPS = ON	10.0 µA
Deep Sleep: 16 KB Data RAM and 64 KB RAM Retention	VDD_PADS = ON VDD_BAT = ON RAM = ON Digital Circuits = ON SMPS = ON	12.0 µA
Idle: Shallow Sleep	VDD_PADS = ON VDD_BAT = ON RAM = ON Digital Circuits = ON MCU = IDLE <1 µs Wake-up Time	0.75 mA
Idle: Active	VDD_PADS = ON VDD_BAT = ON RAM = ON Digital Circuits = ON MCU = IDLE <1 µs Wake-up Time	1.3 mA
TX Active	4 dBm Transmit Power	5 mA Average
RX Active	-90 dBm Sensitivity	5 mA Average

16 QTIL Green Semiconductor Products and RoHS Compliance

QTIL Green semiconductor products comply with various regulatory requirements.

QTIL confirms that QTIL Green semiconductor products comply with the following regulatory requirements:

- Restriction of Hazardous Substances directive guidelines in the EU RoHS Directive 2011/65/EU[1].
- EU REACH, Regulation (EC) No 1907/2006[1]:
  - List of substances subject to authorisation (Annex XIV)
  - Restrictions on the manufacture, placing on the market and use of certain dangerous substances, preparations and articles (Annex XVII). This Annex now includes requirements that were contained within EU Directive, 76/769/EEC. There are many substance restrictions within this Annex, including, but not limited to, the control of use of Perfluorooctane sulfonates (PFOS).
  - When requested by customers, notification of substances identified on the Candidate List as Substances of Very High Concern (SVHC)[1].
- POP regulation (EC) No 850/2004[1]
- EU Packaging and Packaging Waste, Directive 94/62/EC[1]
- Montreal Protocol on substances that deplete the ozone layer
- Conflict minerals, Section 1502, Dodd-Frank Wall Street Reform and Consumer Protection act, which affects columbite-tantalite (coltan / tantalum), cassiterite (tin), gold, wolframite (tungsten) or their derivatives. QTIL is a fabless semiconductor company: all manufacturing is performed by key suppliers. QTIL have mandated that the suppliers shall not use materials that are sourced from "conflict zone mines" but understand that this requires accurate data from the EICC programme. QTIL shall provide a complete EICC / GeSI template upon request.

QTIL has defined the "QTIL Green" standard based on current regulatory and customer requirements including free from bromine, chlorine and antimony trioxide.

Products and shipment packaging are marked and labelled with applicable environmental marking symbols in accordance with relevant regulatory requirements.

This identifies the main environmental compliance regulatory restrictions QTIL specify. For more information on the full "QTIL Green" standard, contact product.compliance@csr.com.

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[1] Including applicable amendments to EU law which are published in the EU Official Journal, or SVHC Candidate List updates published by the European Chemicals Agency (ECHA).

17 Tape and Reel Information

CSR1021 QFN ICs are supplied on tape and reels.

For tape and reel packing and labelling see *IC Packing and Labelling Specification*.

17.1 Tape Orientation

Figure 17-1 shows the CSR1021 QFN packing tape orientation.

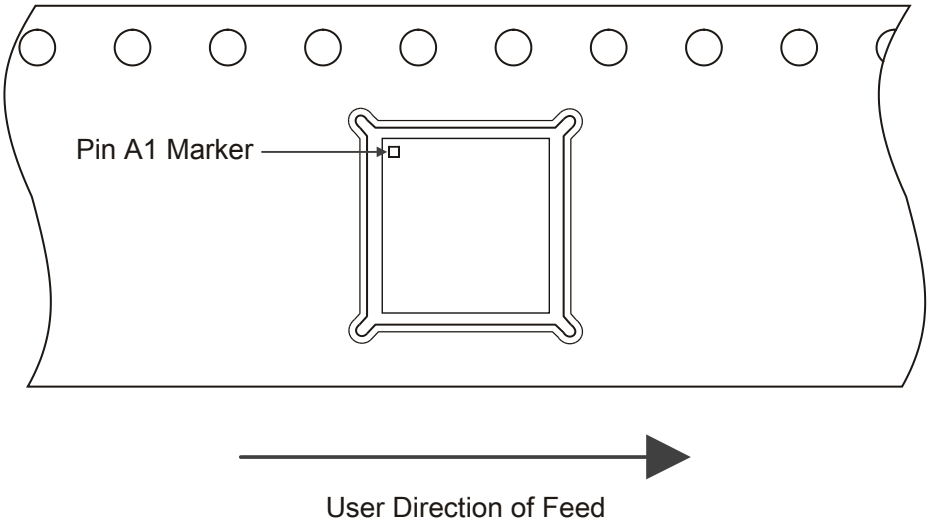

Figure 17-1 CSR1021 QFN Tape Orientation

17.2 Tape Dimensions

Figure 17-2 shows and Table 17-1 lists the dimensions of the tape for the CSR1021 QFN.

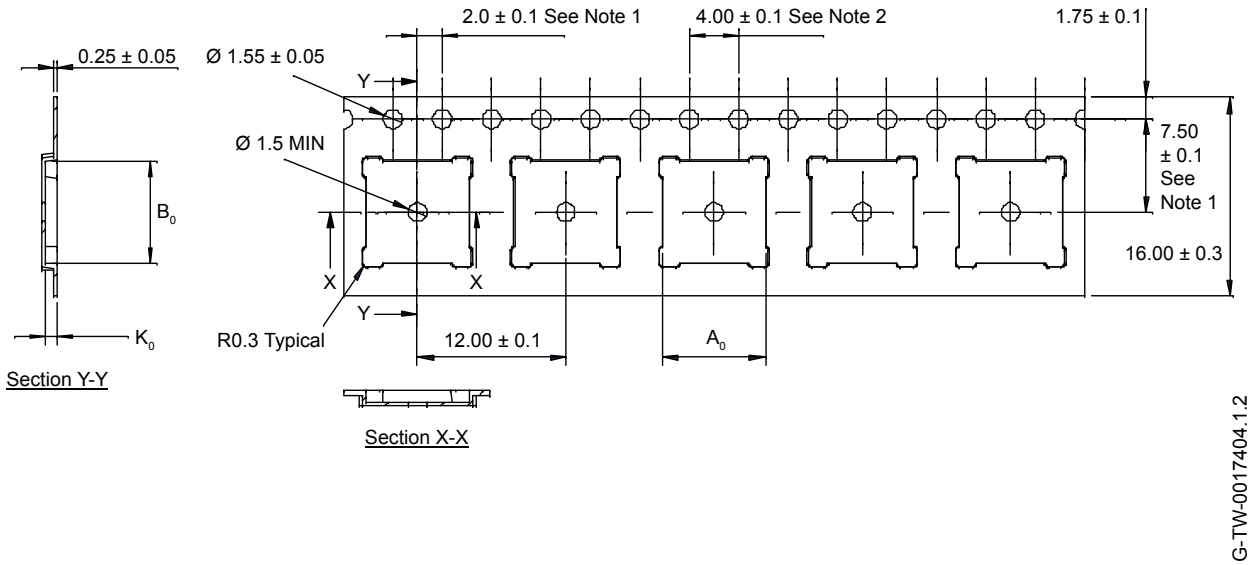

Figure 17-2 CSR1021 QFN Tape Dimensions

Table 17-1 CSR1021 QFN Tape Dimensions

A0	B0	K0	Unit	Notes
8.3	8.3	0.9	mm	1. Measured from centerline of sprocket hole to centerline of pocket. 2. 10 sprocket hole pitch cumulative tolerance ±0.2.

17.3 Reel Information

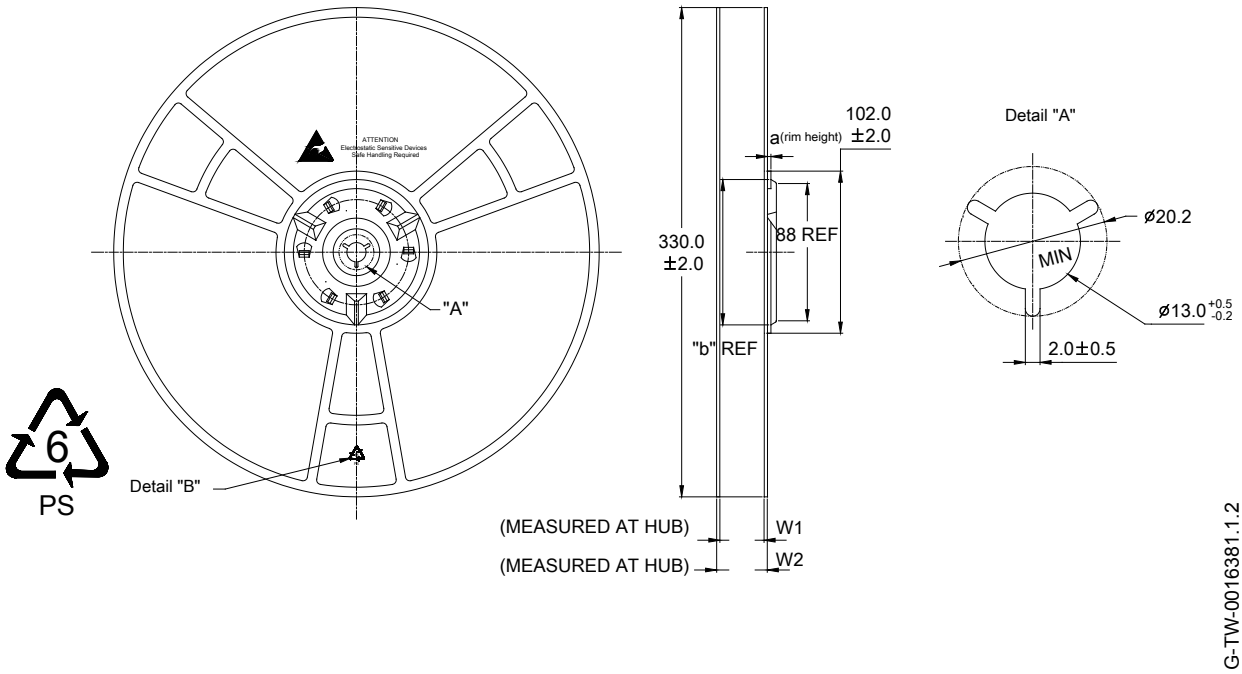

Figure 17-3 CSR1021 QFN Reel Dimensions

Table 17-2 CSR1021 QFN Reel Dimensions

Package Type	Nominal Hub Width (Tape Width)	a	b	W1	W2 Max	Units
8 x 8 x 0.65 mm QFN	16	4.5	98.0	16.8 (1.6/-0.4)	22.4	mm

17.4 Moisture Sensitivity Level

CSR1021 QFN is qualified to moisture sensitivity level MSL3 in accordance with JEDEC J-STD-020.

18 Document References

Document	Reference, Date
Core Specification of the Bluetooth System	Bluetooth Specification Version 4.2, 02 December 2014
CSR102x A05 Limitations	CS-344969-AN
CSR102x Antenna Matching Application Note	CS-344454-AN
CSR102x Recommended Crystals Specification	CS-302662-SP
CSR µEnergy SDK 3.0 Firmware Library Documentation API Description	CS-338038-SP
Environmental Compliance Statement for CSR Green Semiconductor Products	CB-001036-ST
ESDA/JEDEC Joint Standard for Electrostatic Discharge Sensitivity Testing - Charged Device Model (CDM) - Device Level	JS-002-2014, Apr 2015
ESDA/JEDEC Joint Standard for Electrostatic Discharge Sensitivity Testing - Human Body Model (HBM) - Component Level	JS-001-2014, Sep 2014
IC Packing and Labelling Specification	CS-112584-SP
Moisture / Reflow Sensitivity Classification for Nonhermitic Solid State Surface Mount Devices	IPC / JEDEC J-STD-020
Typical Solder Reflow Profile for Lead-free Devices	CS-116434-AN

19 Terms and Definitions

Term	Definition
ADC	Analogue to Digital Converter
AES	Advanced Encryption Standard
AGC	Automatic Gain Control
AIO	Analogue Input/Output
ATT	ATTribute protocol
B	Byte
Bluetooth®	Set of technologies providing audio and data transfer over short-range radio connections
Qualcomm® BlueCore™	Group term for QTIL's range of Bluetooth wireless technology ICs
codec	Coder decoder
CSR™	Cambridge Silicon Radio
dBm	Decibels relative to 1mW
EIA	Electronic Industries Alliance
ESD	Electrostatic Discharge
GAP	Generic Access Profile
GATT	Generic ATTribute protocol
GSM	Global System for Mobile communications
HID	Human Interface Device
I²C	Inter-Integrated Circuit Interface
I²S	Inter-Integrated Circuit Sound
I/O	Input/Output
IC	Integrated Circuit
IF	Intermediate Frequency
IPC	See www.ipc.org
JEDEC	Joint Electron Device Engineering Council (now the JEDEC Solid State Technology Association)
KB	Kilobyte
L2CAP	Logical Link Control and Adaptation Protocol
LCD	Liquid-Crystal Display
LDO	Low (voltage) Drop-Out
LED	Light-Emitting Diode
LNA	Low Noise Amplifier
MAC	Medium Access Control
MCU	MicroController Unit
MISO	Master In Slave Out
MOSI	Master Out Slave In
MTP	Multiple-Time Programmable

Term	Definition
NC	Not Connected or No Connection
NSMD	Non-Solder Mask Defined
NVM	Non-Volatile Memory
OTP	One-Time Programmable
PA	Power Amplifier
PC	Personal Computer
PCB	Printed Circuit Board
PCM	Pulse Code Modulation
PIO	Programmable Input/Output, also known as general purpose I/O
PMU	Power Management Unit
ppm	parts per million
PWM	Pulse Width Modulation
QFN	Quad-Flat No-lead
QTIL	Qualcomm Technologies International, Ltd.
RAM	Random Access Memory
RF	Radio Frequency
RISC	Reduced Instruction Set Computer
RoHS	Restriction of Hazardous Substances in Electrical and Electronic Equipment Directive (2002/95/EC)
ROM	Read Only Memory
RSSI	Received Signal Strength Indication
RX	Receive or Receiver
SMPS	Switch-Mode Power Supply
SPI	Serial Peripheral Interface
TX	Transmit or Transmitter
UART	Universal Asynchronous Receiver Transmitter
VCO	Voltage Controlled Oscillator
W-CDMA	Wideband Code Division Multiple Access