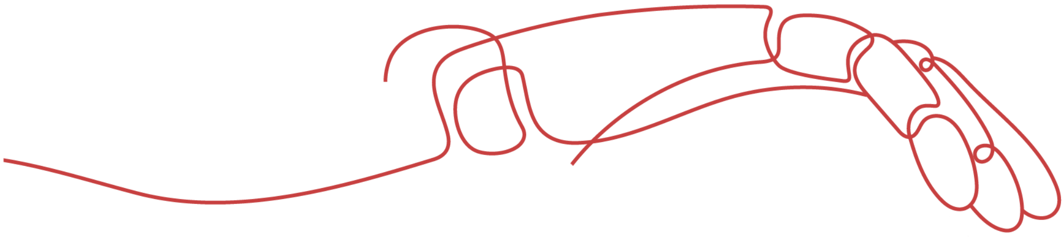
JG Techology



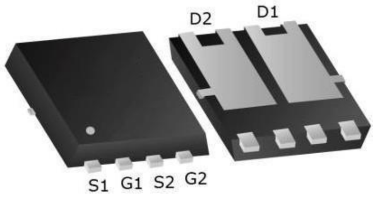
PRODUCT DATA SHEET

To learn more about JGSEMI, please visit our website at

Datasheet Resources Samples

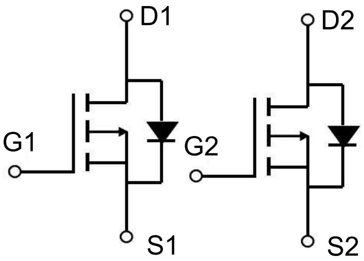
Please note: Please check the JINGAO Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.jg-semi.cn. Please email any questions regarding the system integration to JINGAO_questions@jgsemi.com.

BVDSS	RDSON	ID
-20V	12mΩ	-30A



PDFN3333-8L

- ★ Super Low Gate Charge
- ★ Green Device Available
- ★ Excellent CdV/dt effect decline
- ★ Advanced high cell density Trench technology



Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	-20	V
V_{GS}	Gate-Source Voltage	±12	V
I_D@T_C=25˚C	Continuous Drain Current, V_{GS} @ -4.5V[1]	-30	A
I_D@T_C=70˚C	Continuous Drain Current, V_{GS} @ -4.5V[1]	-18	A
I_{DM}	Pulsed Drain Current[2]	-68	A
P_D@T_C=25˚C	Total Power Dissipation[3]	18	W
P_D@T_C=70˚C	Total Power Dissipation[3]	12	W
T_{STG}	Storage Temperature Range	-55 to 150	˚C
T_J	Operating Junction Temperature Range	-55 to 150	˚C

Thermal Data

Symbol	Parameter	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-Ambient [1]	75	˚C/W
$R_{\theta JA}$	Thermal Resistance Junction-Ambient [1] (t ≤10s)	40	˚C/W
$R_{\theta JC}$	Thermal Resistance Junction-Case[1]	4.2	˚C/W

Electrical Characteristics (T_J=25 ℃, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V , I_D=-250uA	-20	---	---	V
△BV_{DSS}/△T_J	BV_{DSS} Temperature Coefficient	Reference to 25℃ , I_D=-1mA	---	-0.012	---	V/℃
$R_{DS(ON)}$	Static Drain-Source On-Resistance[2]	V_{GS}=-4.5V , I_D=-10A	---	12	15	mΩ
		V_{GS}=-2.5V , I_D=-8A	---	16	20	
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS}=V_{DS} , I_D =-250uA	-0.4	-0.7	-1.0	V
△$V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	2.94	---	mV/℃
I_{DSS}	Drain-Source Leakage Current	V_{DS}=-15V , V_{GS}=0V , T_J=25℃	---	---	1	uA
I_{GSS}	Gate-Source Leakage Current	V_{GS}=±12 V , V_{DS}=0V	---	---	±100	nA
gfs	Forward Transconductance	V_{DS}=-5V , I_D=-10A	---	43	---	S
Q_g	Total Gate Charge (-4.5V)	V_{DS}=-10V , V_{GS}=-4.5V , I_D=-10A	---	35	---	nC
Q_{gs}	Gate-Source Charge		---	5.0	---	
Q_{gd}	Gate-Drain Charge		---	10	---	
$T_{d(on)}$	Turn-On Delay Time	V_{DD}=-10V , V_{GS}=-4.5V , R_G=3.3Ω, I_D=-10A	---	12.0	---	ns
T_r	Rise Time		---	40.0	---	
$T_{d(off)}$	Turn-Off Delay Time		---	30	---	
T_f	Fall Time		---	10	---	
C_{iss}	Input Capacitance	V_{DS}=-15V , V_{GS}=0V , f=1MHz	---	2800	---	pF
C_{oss}	Output Capacitance		---	690	---	
C_{rss}	Reverse Transfer Capacitance		---	590	---	

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_S	Continuous Source Current[1,4]	V_G=V_D=0V , Force Current	---	---	-30.0	A
I_{SM}	Pulsed Source Current[2,4]		---	---	----	A
V_{SD}	Diode Forward Voltage[2]	V_{GS}=0V , I_S=-1A , T_J=25℃	---	---	-1.2	V
t_{rr}	Reverse Recovery Time	IF=-10A , dI/dt=100A/μs , T_J =25℃	---	27	---	nS
Q_{rr}	Reverse Recovery Charge		---	17.8	---	nC

Note :

1. The data tested by surface mounted on a 1 inch^2 FR-4 board with 2OZ copper.
2. The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%
3. The power dissipation is limited by 150℃ junction temperature
4. The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

Typical Characteristics

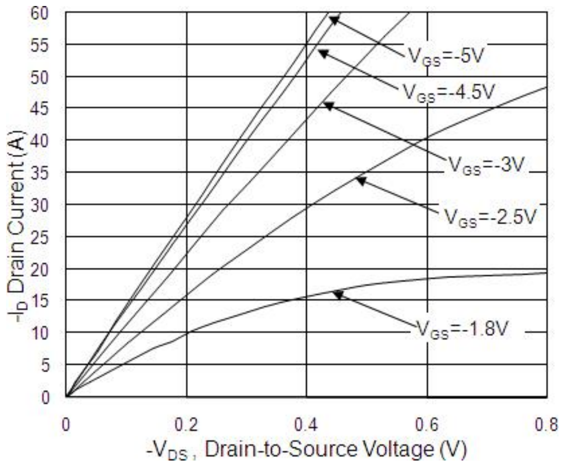


Fig.1 Typical Output Characteristics

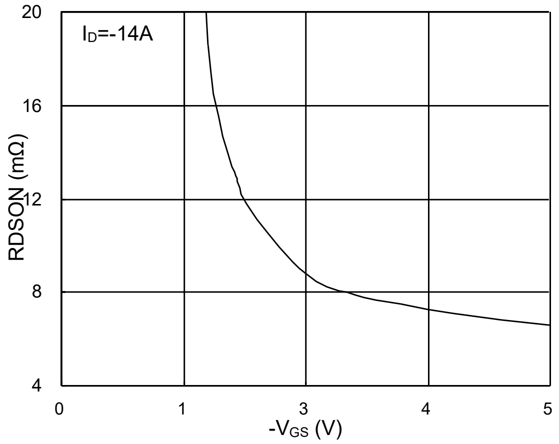


Fig.2 On-Resistance vs. G-S Voltage

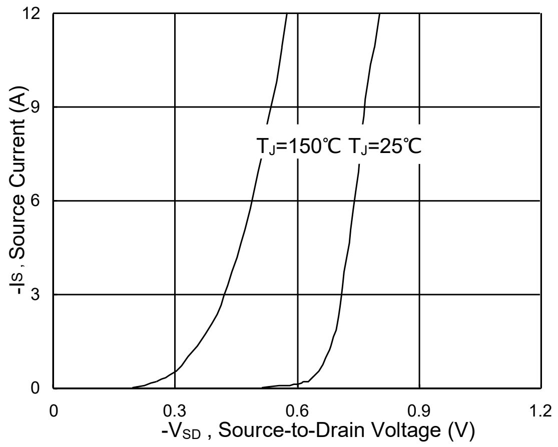


Fig.3 Forward Characteristics of Reverse

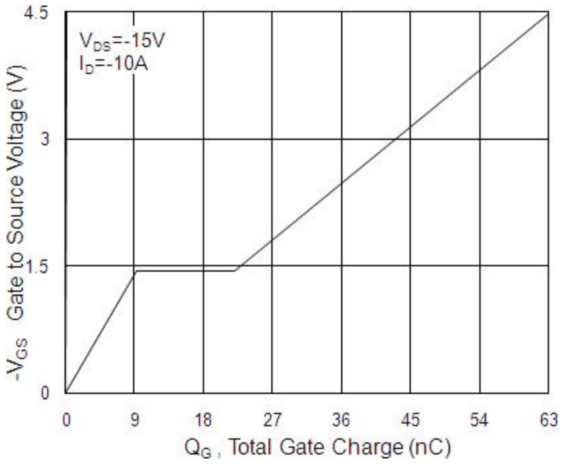


Fig.4 Gate-charge Characteristics

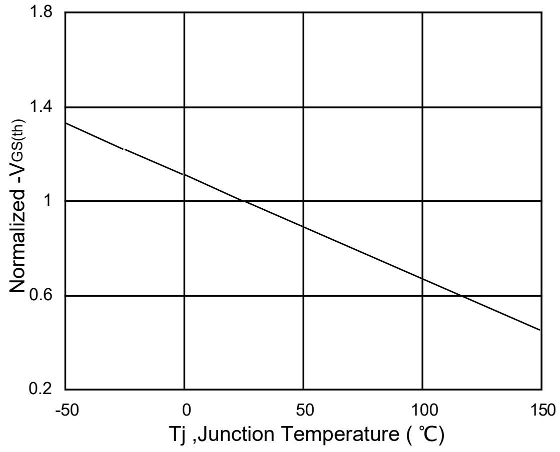


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

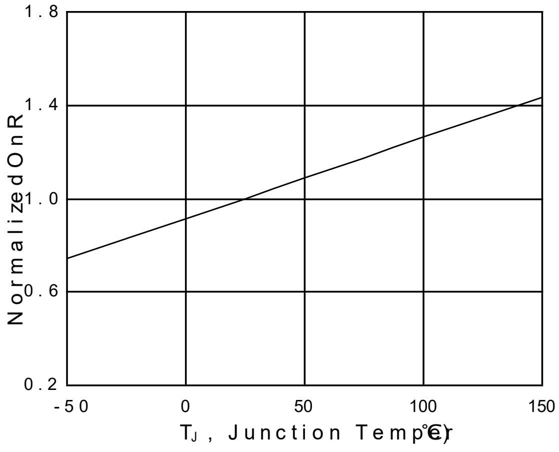


Fig.6 Normalized R_{DSON} vs. T_J

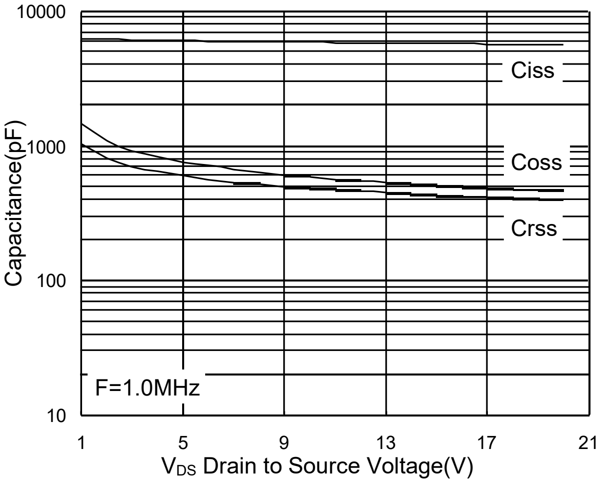


Fig.7 Capacitance

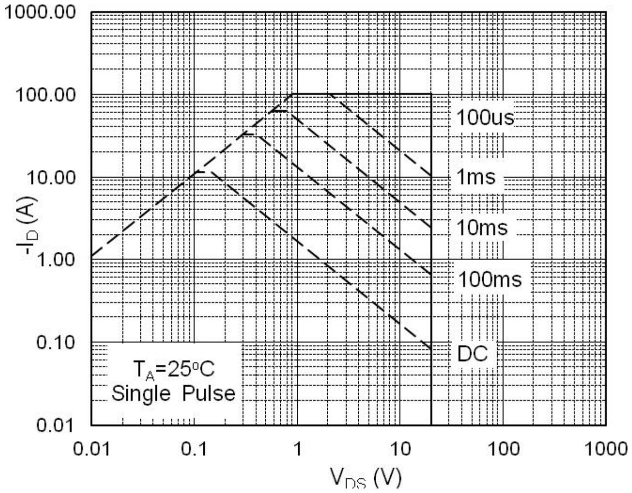


Fig.8 Safe Operating Area

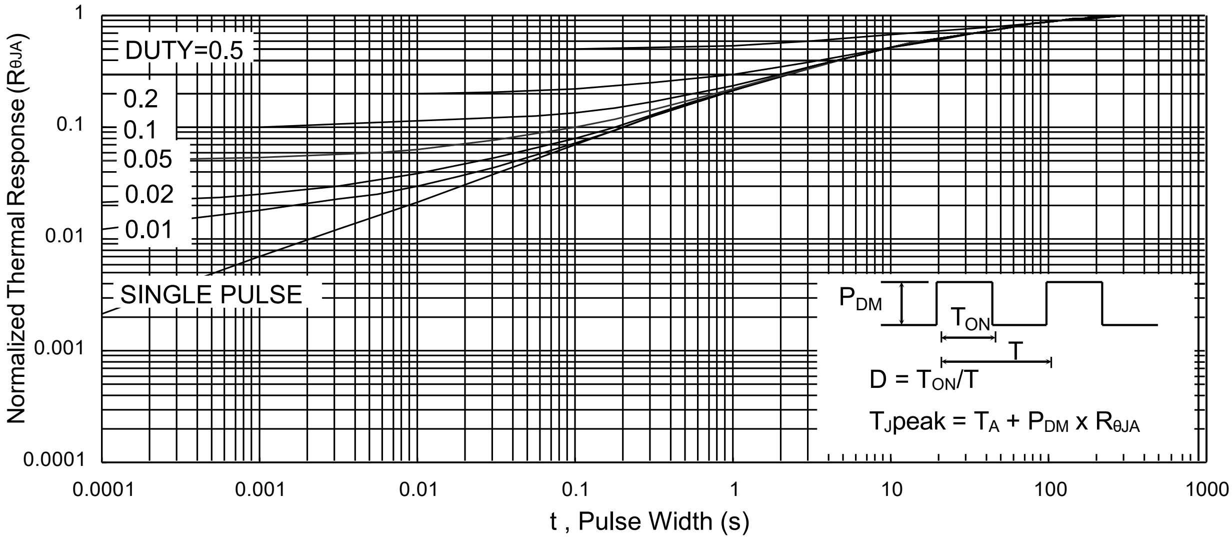


Fig.9 Normalized Maximum Transient Thermal Impedance

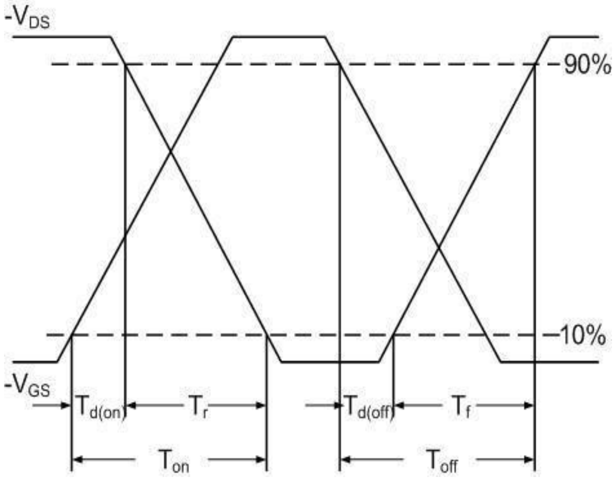


Fig.10 Switching Time Waveform

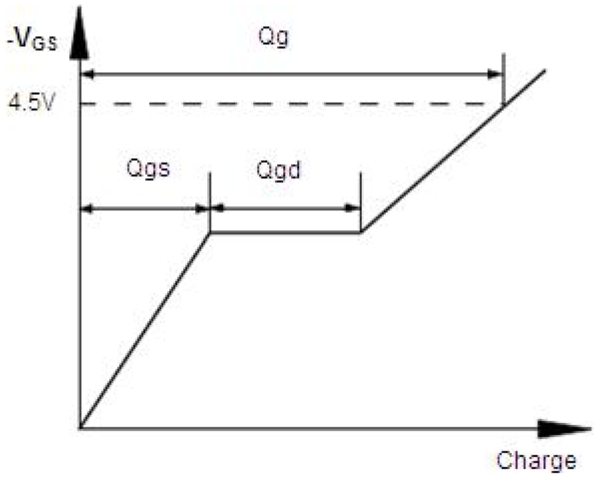
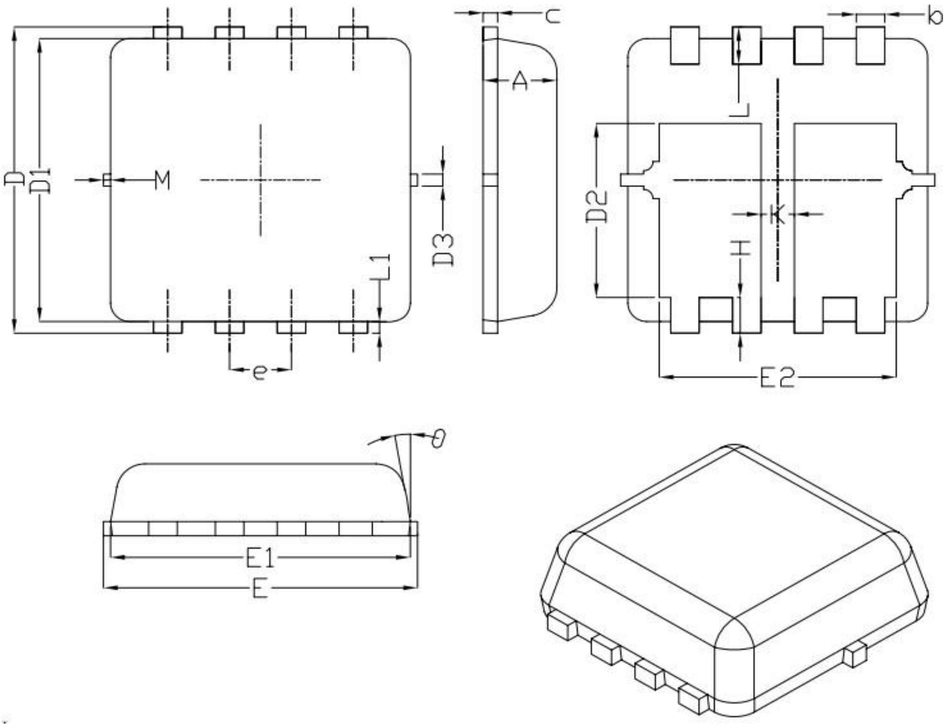


Fig.11 Gate Charge Waveform

Dual PDFN3333-8L Package Outline Data



Symbol	Dimensions (unit: mm)		
	Min	Typ	Max
A	0.70	0.75	0.80
b	0.25	0.30	0.35
c	0.10	0.15	0.25
D	3.25	3.35	3.45
D1	3.00	3.10	3.20
D2	1.78	1.88	1.98
D3	--	0.13	--
E	3.20	3.30	3.40
E1	3.00	3.15	3.20
E2	2.39	2.49	2.59
e	0.65 BSC		
H	0.30	0.39	0.50
L	0.30	0.40	0.50
L1	--	0.13	--
K	0.30	--	--
θ	--	10°	12°
M	*	*	0.15
* Not Specified			

Notes:

1. Refer to JEDEC MO-240 variation CA.
2. Dimensions "D1" and "E1" do NOT include mold flash protrusions or gate burrs.
3. Dimensions "D1" and "E1" include interterminal flash or protrusion.

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