GENERAL DESCRIPTION

OB5283 is a highly integrated current mode PWM control IC with high voltage startup, optimized for high performance, low standby power consumption and cost effective offline flyback converter applications. The controller's HV pin is used for high voltage startup, AC off detection, and X-cap Voltage discharge , this structure allows the brownout detection as well.

At full loading, the IC operates in fixed frequency (65KHz) mode. When the loading goes low, it operates in Green mode with valley switching for high power conversion efficiency. When the load is very small, the IC operates in 'Extended Burst Mode' to minimize the standby power loss. As a result, high conversion efficiency can be achieved in the whole loading range.

High voltage startup is implemented in OB5283, which features with short startup time and low standby power loss.

OB5283 offers complete protection coverage including cycle-by-cycle current limiting (OCP), over load protection (OLP), over temperature protection (OTP), output short(SCP), output and VDD over voltage protection. Excellent EMI performance is achieved with On-Bright proprietary frequency shuffling technique.

The tone energy at below 25KHz is minimized to avoid audio noise during operation.

OB5283 is offered in SOP8 package.

APPLICATIONS

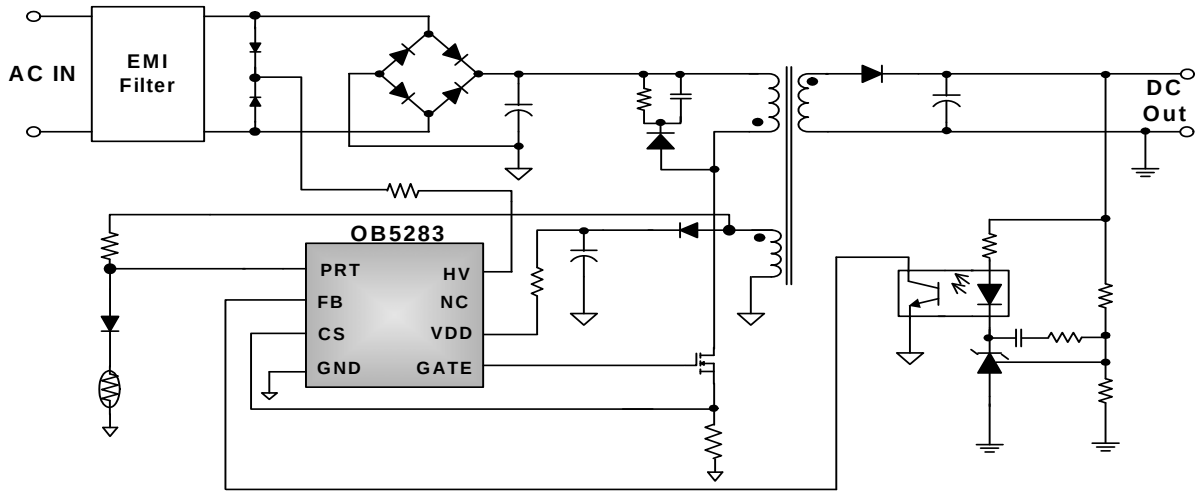
Offline AC/DC flyback converter for

- Power adaptor
- Open-frame SMPS
- PK Load Application

FEATURES

- High voltage startup
- Power on soft start reducing MOSFET Vds stress
- Frequency shuffling for EMI
- Multi-Mode Operation
  - 125KHz max frequency mode @ Peak Load
  - 65KHz fix frequency mode @ Full Load
  - Valley switching operation @ Green mode
  - Burst Mode @ Light Load & No Load
- Audio noise free operation
- Peak power delivery for peak load
- Tighten and programmable output over current protection
- Comprehensive protection coverage
  - o VDD under voltage lockout with hysteresis (UVLO)
  - o Cycle-by-cycle over current protection (OCP) with auto-recovery
  - o Overload protection (OLP) with auto-recovery
  - o Over temperature protection (OTP) with latch shut down
  - o VDD over voltage protection with latch shut down
  - o Output over voltage protection with latch shut down
  - o Output short protection (SCP) with auto-recovery
  - o Brownout protection with auto-recovery
  - o Output diode short protection with latch shut down
- Intelligent AC off detection with X-CAP discharge function

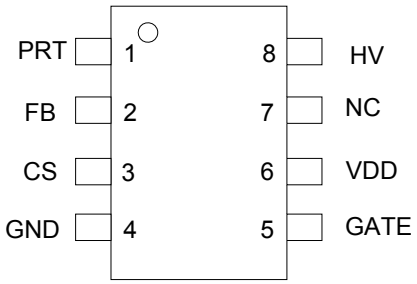
TYPICAL APPLICATION



GENERAL INFORMATION

Pin Configuration

The OB5283 is offered in SOP8 package, shown as below.



Ordering Information

Part Number	Description
OB5283CP	SOP8, Pb-free
OB5283CPA	SOP8, Pb-free in Taping

Package Dissipation Rating

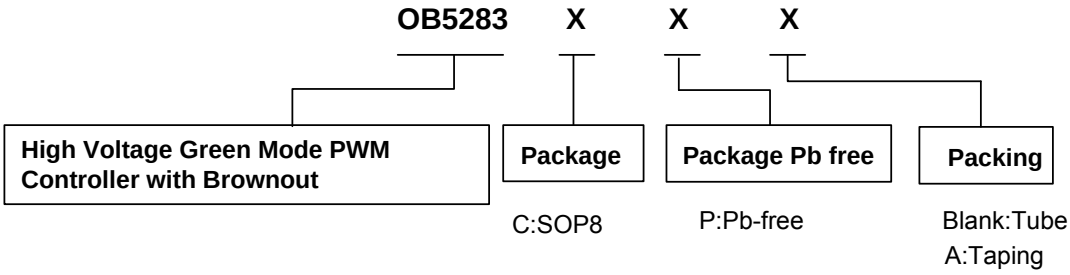
Package	RθJA(℃/W)
SOP8	90

Absolute Maximum Ratings

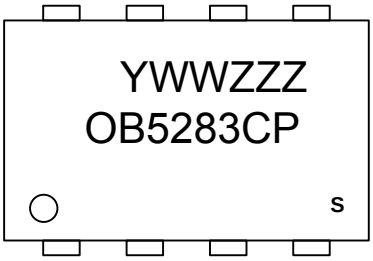
Parameter	Value
VDD DC Supply Voltage	V_{OVP}-1V
High-Voltage Pin, HV	-0.3 to 500 V
FB Input Voltage	-0.3 to 7V
CS Input Voltage	-0.3 to 7V
PRT Input Voltage	-0.3 to 7V
Min/Max Operating Junction Temperature TJ	-40 to 150 ℃
Operating Ambient Temperature T_A	-40 to 85 ℃
Min/Max Storage Temperature Tstg	-55 to 150 ℃
Lead Temperature (Soldering, 10secs)	260 ℃

Recommended Operating Condition

Symbol	Parameter	Range
VDD	VCC Supply Voltage	12 to 28V



Marking Information



Y:Year Code
WW:Week Code(01-52)
ZZZ:Lot Code
C:SOP8 Package
P:Pb-free Package
S:Internal Code(Optional)

TERMINAL ASSIGNMENTS

Pin Num.	Pin Name	I/O	Description
1	PRT	I	Multiple functions pin. Connecting a NTC resistor to ground for OTP detection. Connecting a resistor from Vaux can adjust OVP trigger voltage and detect transformer core demagnetization. If both OTP and OVP are needed, a diode should be connected between PRT pin and the NTC resistor.
2	FB	I	Feedback input pin. The PWM duty cycle is determined by voltage level into this pin and the current-sense signal at CS pin
3	CS	I	Current sense input
4	GND	P	Ground
5	Gate	O	Totem-pole gate driver output for power Mosfet
6	VDD	P	Power Supply
7	NC		
8	HV	P	Connected to the line input via resistors and diodes for startup and x-cap discharge, this PIN allows the brownout detection as well.

ELECTRICAL CHARACTERISTICS

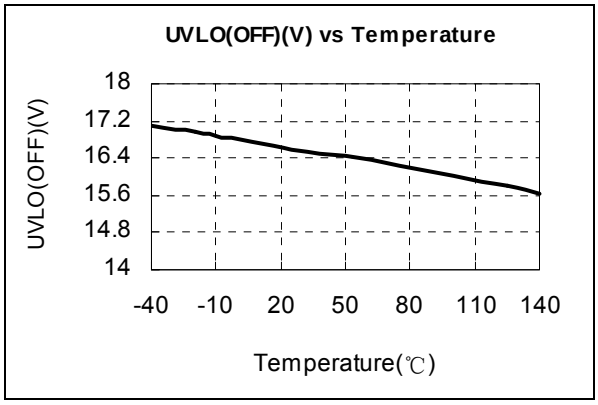
(T_A = 25℃, VDD=15V, unless otherwise noted)

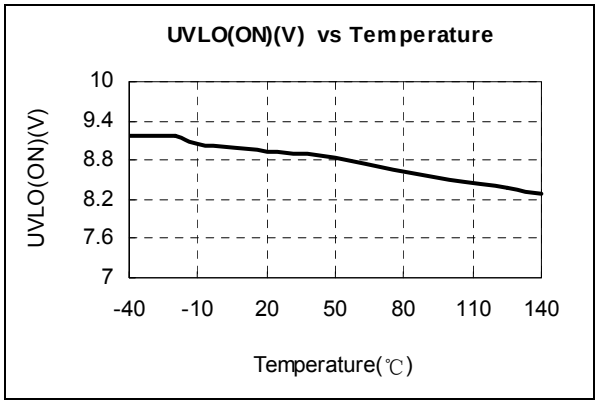
Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
IHV1	Supply current from HV pin @VDD>1V	VDD=2V, HV=100V	1	2	3.5	mA
IHV2	Supply current from HV pin @VDD<1V	VDD=0.5V,HV=100V	0.3	0.57	0.85	mA
leakage	HV pin leakage current after startup	VDD=18V, HV=500V			10	uA
Supply Voltage (VDD)						
Istartup	VDD Start up Current	VDD=UVLO(OFF)-1V, measure leakage current into VDD		5	20	uA
I_VDD_Operation	Normal Operation Current	V_{FB}=3V, CL=1nF		2.5	3	mA
I_VDD_Burst	Burst Operation Current	V_{FB}=0.5V, CL=1nF		0.7	0.8	mA
UVLO(ON)	VDD Under Voltage Lockout Enter		7.75	8.75	9.75	V
UVLO(OFF)	VDD Under Voltage Lockout Exit (Recovery)		15.75	16.75	17.75	V
Vpull-up	Pull-up PMOS active			11		V
OVP	Over voltage protection voltage	FB=3V Ramp up VDD until gate clock is off	29	30	31	V
Vth_latch	Latch release voltage			5.2		V
T_D_rst	Restart time for OCP / peak power protection occurs			9		s
Feedback Input Section(FB Pin)						
V_{FB} Open	V_{FB} Open Loop Voltage			5.1		V
Avcs	PWM input gain ΔVFB/ΔVCS			3.5		V/V
Maximum duty cycle	Max duty cycle @ VDD=14V,VFB=3V,VCS=0.3V		75	80	85	%
Vref_rising	The threshold enter rising frequency mode			3.5		V
Vref_green	The threshold enter green mode			2.10		V
Vref_burst_H	The threshold exit burst mode			1.5		V
Vref_burst_L	The threshold enter burst mode			1.4		V
I_{FB}_Short	FB pin short circuit current	Short FB pin to GND and measure current		180		uA
V_{TH}_PK	PK Power Limiting FB Threshold Voltage		4.2	4.4		V
T_D_PK	PK Power Limiting Debounce Time			3.85		s
Z_{FB}_IN	Input Impedance			22		KΩ
Current Sense Input(CS Pin)						
SST_CS	Soft start time of CS threshold			2.5		ms
T_blanking	Leading edge blanking time			250		ns
Z_{SENSE}_IN	Input Impedance			40		KΩ
T_D_OC	Over Current Detection and Control Delay	From Over Current Occurs till the gate driver output starts to turn off		90		ns

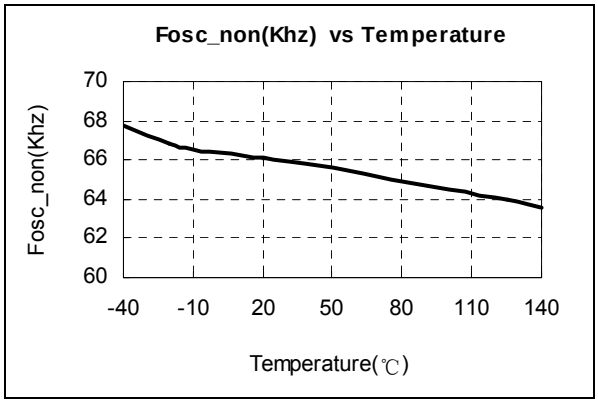
V_{TH}_PK	Internal Current Limiting Threshold Voltage with zero duty cycle		0.48	0.50	0.52	V
VPK_clamping	CS voltage clamper			0.84		V
V_{OCP}_ref	Internal OCP protection voltage threshold		0.286	0.295	0.304	V
I_{OCP}_ADJ	Output current from CS pin when PWM turns off		92	100	108	uA
T_D_OCP	OCP Debounce Time			3.85		s
Oscillator						
F_{OSC}	Normal Oscillation Frequency	VDD=15V, FB=3V,	60	65	70	KHz
Fosc_PK	Peak frequency	VDD=15V,FB=4.5V,		125		KHz
SST_freq	Soft start time of frequency			30		ms
∆f_OSC	Frequency jittering			+/-7		%
F_shuffling	Shuffling frequency			60		Hz
∆f_Temp	Frequency Temperature Stability			1		%
∆f_VDD	Frequency Voltage Stability			1		%
F_Burst	Burst Mode Switch Frequency			25		KHz
Gate driver						
VOL	Output low level @ VDD=15V, Io=20mA				1	V
VOH	Output high level @ VDD=15V, Io=20mA		8			V
V_clamping	Output clamp voltage			12		V
T_r	Output rising time 1.2V ~ 10.8V @ CL=1000pF			100		ns
T_f	Output falling time 10.8V ~ 1.2V @ CL=1000pF			50		ns
Brownout protection						
Vth_bo_L	Threshold voltage for Brownout	RHV=200 KΩ	63	70	77	VAC
Vth_bo_H	Threshold voltage for Brownout release	RHV=200 KΩ	70	77	85	VAC
Td_brownout	Brownout debounce time		27	32	37	ms
PRT pin						
Ibias	Output bias current expect during OVP detection			20		uA
IRT	Output current for external OTP detection		114	120	126	uA
VOTP	Threshold voltage for external OTP		1.14	1.2	1.26	V
Td_ex_OTP	EX OTP debounce time			30		Cycles
Ioutput_ovp	Current threshold for adjustable output OVP		170	180	190	uA
Td_output_ovp	Output OVP debounce time			5		Cycles
Iscp	SCP threshold			42		uA
Td_scp	SCP detect after startup			15		ms
On Chip OTP						
OTP Level				155		℃
OTP exit				125		℃

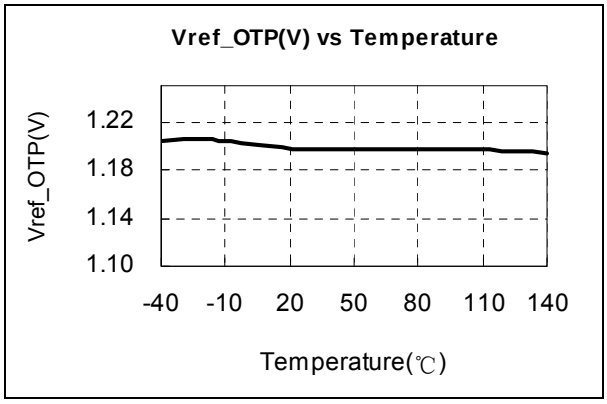
CHARACTERIZATION PLOTS

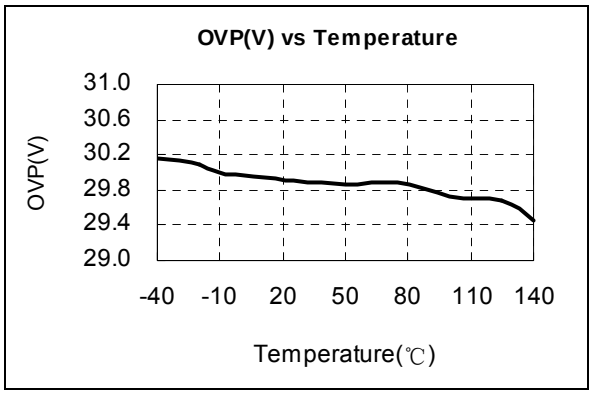
VDD = 18V, TA = 25℃ condition applies if not otherwise noted.

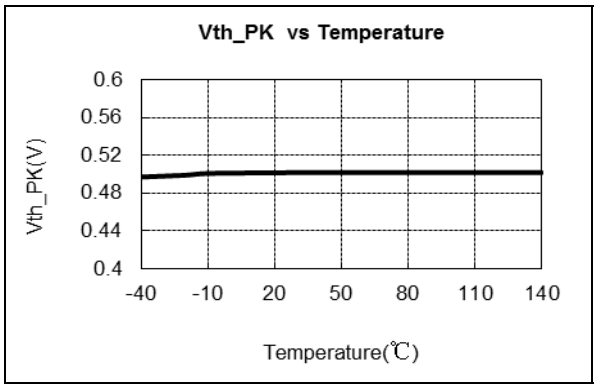


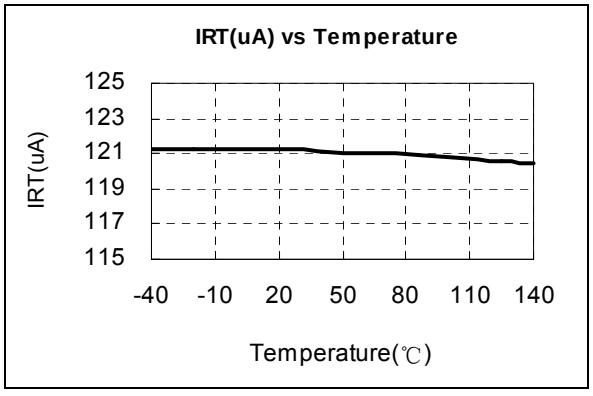


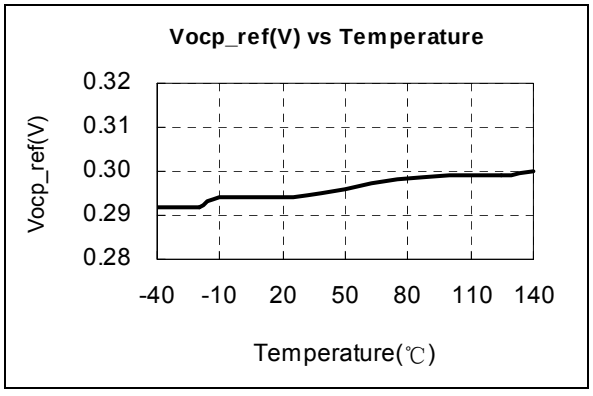












OPERATION DESCRIPTION

OB5283 is a highly integrated current mode PWM control IC optimized for high performance, low standby power consumption and cost effective offline flyback converter applications. The 'Extended burst mode' control greatly reduces the standby power consumption and helps the design easily to meet the international power conservation requirements.

Internal High Voltage Startup and Under Voltage Lockout (UVLO)

OB5283 integrates HV startup circuit, and provides about 2mA current to charge VDD pin during power on state from HV pin. When VDD voltage is higher than UVLO(OFF), the charge current is switched off. At this moment, the VDD capacitor provides current to OB5283 until the auxiliary winding of the main transformer starts to provide the operation current.

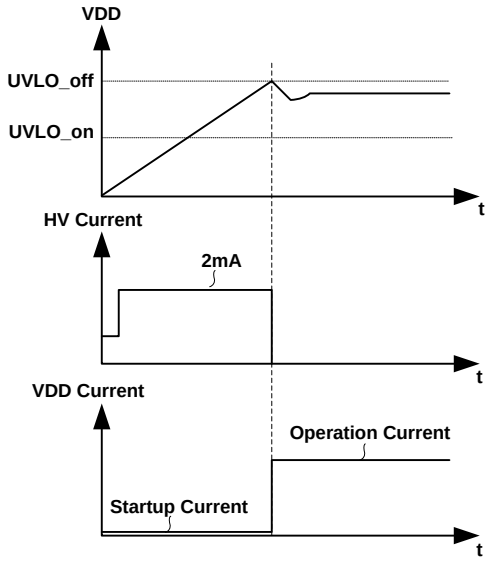


Fig1 Startup current timing

Operating Current

The typical operating current of OB5283 is 2.5mA. Good efficiency is achieved with this low operating current together with the 'Extended burst mode' control features.

Soft Start

OB5283 features an internal 2.5ms (typical) soft start to soften the electrical stress occurring in the power supply during startup. It is activated during the power on sequence. As soon as VDD reaches UVLO(OFF), the CS peak voltage is gradually increased from 0V to the maximum level. Every restart up begins with a soft start.

Frequency shuffling for EMI improvement

The frequency shuffling (switching frequency modulation) is implemented in OB5283. The oscillation frequency is modulated so that the tone energy is spread out. The spread spectrum minimizes the conduction band EMI and therefore eases the system design.

Extended Burst Mode Operation

At light load or no load condition, most of the power dissipation in a switching mode power supply is from switching loss of the MOSFET, the core loss of the transformer and the loss of the snubber circuit. The magnitude of power loss is in proportion to the switching frequency. Lower switching frequency leads to the reduction on the power loss and thus conserves the energy.

The switching frequency is internally adjusted at no load or light load condition. The switch frequency reduces at light/no load condition to improve the conversion efficiency. At light load or no load condition, the FB input drops below Vref_burst_L (the threshold enter burst mode) and device enters Burst Mode control. The Gate drive output switches when FB input rises back to Vref_burst_H (the threshold exit burst mode). Otherwise the gate drive remains at off state to minimize the switching loss and reduces the standby power consumption to the greatest extend.

Oscillator Operation

During the full load power operation, OB5283 operates at a 65KHz (typical) fixed frequency. The efficiency and system cost is controlled at an optimal level. A peak power mode is implemented based on On-Bright proprietary technology to supply a peak current output requirement. In peak power mode, frequency is increased from 65KHz (typical) to 125KHz (typical).

At light load, OB5283 enters the light load mode, where the output current is reduced. The switching losses are reduced by lowering the switching frequency.

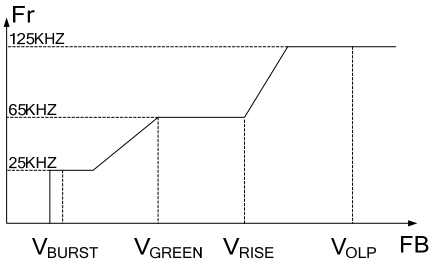


Fig2 Frequency vs Feedback voltage

Current Sensing and Leading Edge Blanking

Cycle-by-Cycle current limiting is offered in OB5283 current mode PWM control. The switch current is detected by a sense resistor into the CS pin. An internal leading edge blanking circuit chops off the sensed voltage spike at initial internal power MOSFET on state due to snubber diode reverse recovery and surge gate current of power MOSFET. The current limiting comparator is disabled and cannot turn off the internal power MOSFET during the blanking period. The PWM duty cycle is determined by the current sense input voltage and the FB input voltage.

Internal Synchronized Slope Compensation

Built-in slope compensation circuit adds voltage ramp into the current sense input voltage for PWM generation. This greatly improves the close loop stability at CCM and prevents the sub-harmonic oscillation and thus reduces the output ripple voltage.

Driver

The power MOSFET is driven by a dedicated gate driver for power switch control. Too weak the gate driver strength results in higher conduction and switch loss of MOSFET while too strong gate driver strength results the compromise of EMI.
A good tradeoff is achieved through the built-in totem pole gate design with right output strength and dead time control. The low idle loss and good EMI system design is easier to achieve with this dedicated control scheme.

Demagnetization Detection

The transformer core demagnetization is detected by monitoring the voltage activity on the auxiliary windings through PRT pin. This voltage features a flyback polarity. After the on time (determined by the CS voltage and FB voltage), the switch is off and the flyback stroke starts. After the flyback stroke, the drain voltage shows an oscillation with a frequency of approximately $1/2\pi\sqrt{L_pC_d}$, where L_p is the primary self inductance of primary winding of the transformer and C_d is the capacitance on the drain node.
The typical detection level is fixed at -50mV at the PRT pin. Demagnetization is recognized by detection of a possible “valley” when the voltage at PRT is below -50mV in falling edge.

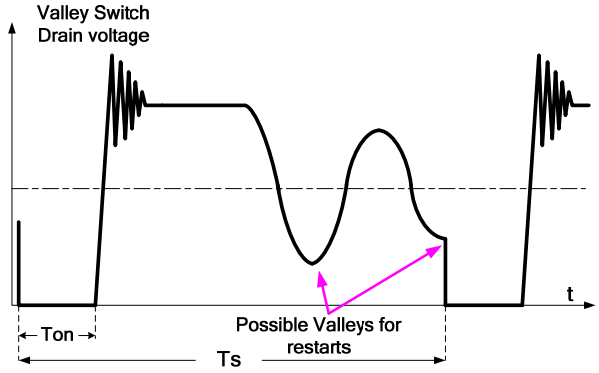


Fig3 Valley detection

Dual Function of External OTP and Output OVP

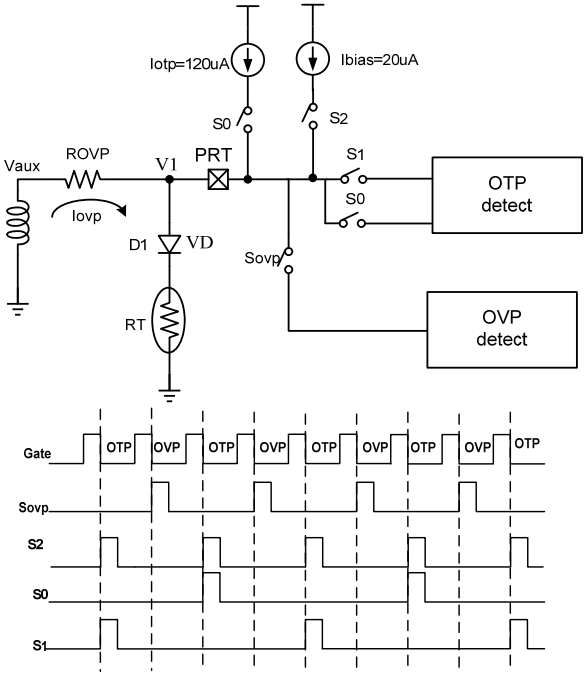


Fig4 PRT Pin protection timing

On-Bright proprietary dual function of external OTP and output OVP provides feasible and accurate detection of external OTP through NTC resistor and output OVP. The dual function is realized through time-division technology as shown in the figure 4.
There is a 20uA(typical) bias current outflow when S2=1, that’s S0= “1” or S1= “1”. For external OTP detection, when switch control signal S1= “1”, the 20uA (typical) current flows out from PRT pin. When switch control signal S0= “1”, another 120uA (typical IRT) current flows out from PRT pin in addition to 20uA.
So the PRT pin voltage V1(s0) at phase S1=“1” is:

$$V1(s1) = \frac{ROVP \cdot VD + RT \cdot Vaux + RT \cdot ROVP \cdot 20uA}{ROVP + RT}$$

The PRT pin voltage V1(s1) at phase S0="1" is

$$V1(s0) = \frac{ROVP \cdot VD + RT \cdot Vaux + RT \cdot ROVP(20uA + 120uA)}{ROVP + RT}$$

Vaux is the auxiliary winding demagnetization voltage.
VD is D1 forward voltage.
ROVP and RT are shown in fig4.
Voltage difference of ΔVotp at phase S0 and S1 phase is

$$\Delta V_{otp} = V1(s0) - V1(s1) = \frac{RT \cdot ROVP}{ROVP + RT} \cdot 120uA$$

This voltage difference cancels the effect of D1 diode forward voltage.
When ΔVotp< VOTP (1.2V typical) , external OTP latch protection is triggered after 30(typical) PWM cycles debounce.

For output OVP detection, when Sovp= "1", Iovp is equal to Vo/ROVP. If Iovp is larger than 180uA (typical Ioutput_ovp), output OVP is triggered. The output OVP is calculated as

$$V_{outovp} = \frac{180uA \cdot N_{sec} \cdot ROVP}{N_{aux}} - V_{diode}$$

Nsec is transformer secondary winding turns, Naux is transformer auxiliary winding turns, Vdiode is the secondary output diode forward voltage .
OVP latch protection is triggered after 5 Gate cycles debounce. By selecting proper Rovp resistance, output OVP level can be programmed.

Protection Controls

Good power supply system reliability is achieved with auto-recovery protection features including OCP, output short protection, Under Voltage Lockout on VDD (UVLO) and peak load protection, and latched shutdown features including Over Temperature Protection (OTP), VDD and output Over Voltage Protection (OVP).
With On-Bright proprietary technology, the OCP is line voltage compensated to achieve constant output OCP limit over the universal input voltage range and its dependency on primary inductance and frequency is removed.
At overload condition when FB input voltage exceeds power limit threshold value for more than Td_OLP, control circuit reacts to shut down the converter. It restarts when VDD voltage drops below UVLO limit. For protection with latched shut down mode, control circuit shuts down (latch) the power MOSFET when an over temperature condition or over voltage condition is detected until VDD drops below 5.2V (typical) (Latch release voltage), and the device enters power on restart-up sequence thereafter.

OCP and Peak output Current Controls

In order to meet peak current output requirement, OB5283 sets up two levels output current protection thresholds. The two thresholds correspond to the normal OCP protection and peak power protection respectively. When output current exceeds the OCP threshold for 3.85s (typical), OCP protection occurs. The OCP loop ensures the output OCP has a very tight range and is only related with turns ratio and Rsense.
At PWM off state, 100uA current flows out of CS pin to generate a voltage through R1 and Rsense. The voltage at CS pin can adjust output OCP threshold.

$$I_{OCP} = \frac{(V_{OCP\_}ref - 100uA \cdot R1) \bullet N}{Rsense}$$

N is the ratio of transformer primary winding turns to secondary winding turns. The specification for output OCP protection voltage threshold, V_{OCP_ref}, is 0.295V (typical). The specification for maximum primary winding cycle-by-cycle OCP threshold voltage (for peak load), VPK_Clamping, is 0.84V(typical).

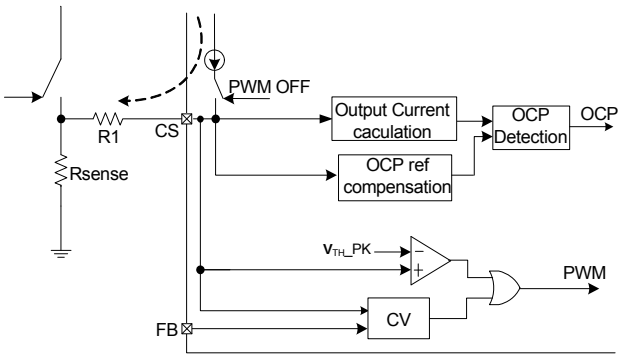


Fig5 programmable OCP and PK load protection

When primary side inductor current exceeds the peak power threshold, over peak power timer will begin counting. After 3.85s (typical), peak load protection occurs.

Two level OCP Controls

In order to meet peak current output requirement, OB5283 sets up two levels OCP protection thresholds. The two thresholds correspond to the normal OCP protection and peak power protection respectively, and these two threshold values are internally compensated. When primary side inductor current exceeds the OCP threshold, OCP timer will begin counting. After 3.85s (typical), OCP protection occurs.

When primary side inductor current exceeds the peak power threshold, over peak power timer will begin counting. After 3.85s (typical), peak load protection occurs.
OCP and peak power protection are mutually independent and do not affect each.
When OCP or peak power protection occurs, no GATE output and VDD begins discharging and charging until the duration is longer than 9s . Then VDD begins dropping until to UVLO(on) and later restarts.

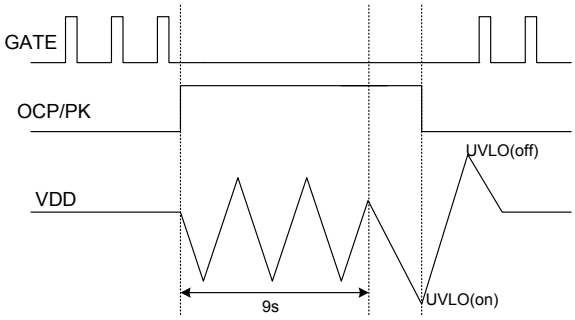


Fig6 Restart Timing when two level OCP occurs

Pin Floating and Short Protection
OB5283 provides PIN floating protection for all the pins and pin short protection for adjacent pins. In the cases when a pin is floating or two adjacent pins are shorted, Gate switching is disabled.

Intelligent AC off Detect with X-CAP discharge function
The HV pin is also used for AC off detection. When AC is off, the AC off state can be detected through HV pin. Then IC will provide a discharge path from HV pin to GND for the X-CAP discharge.

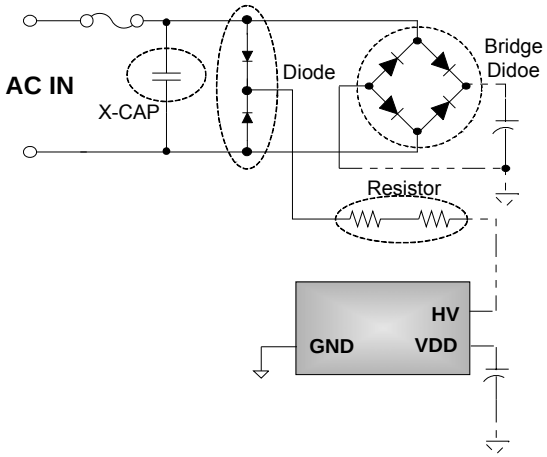


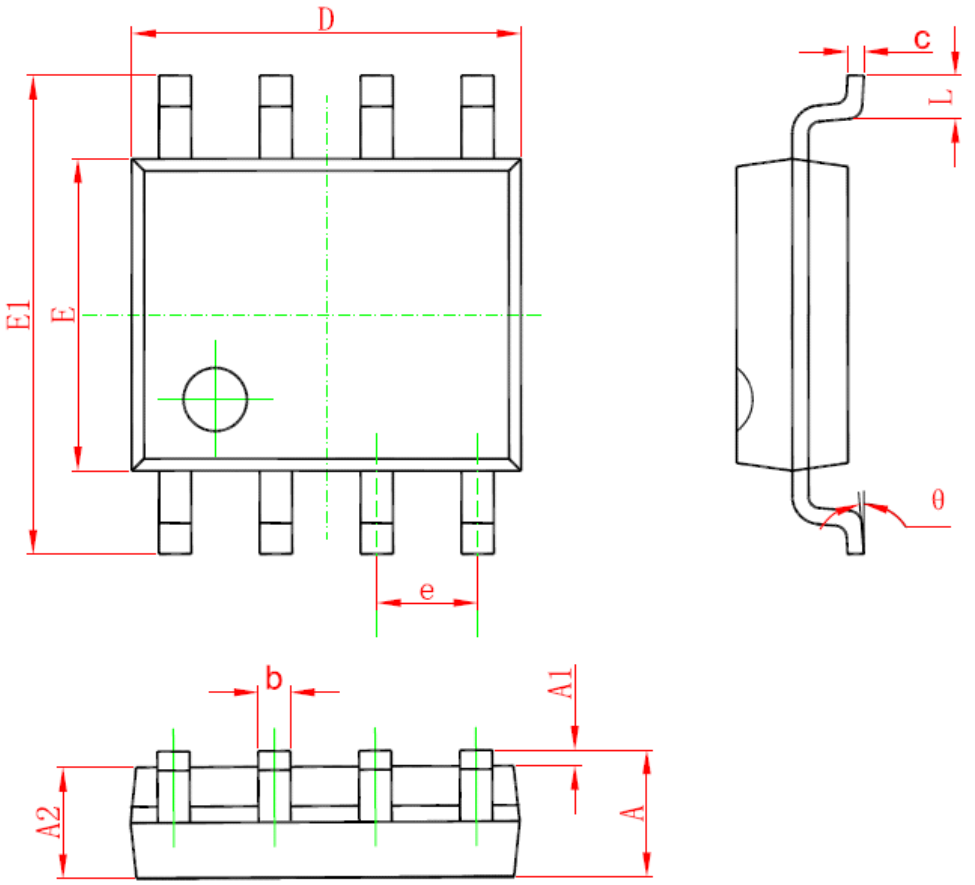
Fig7 X-CAP discharge circuit

Discharge circuit main components selection

Components	Voltage/Current Stress Range
Bridge Diode	≥600V ≥2A
Diode	≥1000V ≥1A
Resistor	R1206(1/4W)×2 Total impendence 200kΩ
X-CAP	0.1uF – 1.36uF

PACKAGE MECHANICAL DATA

SOP8 PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.050	0.250	0.002	0.010
A2	1.250	1.650	0.049	0.065
b	0.310	0.510	0.012	0.020
c	0.100	0.250	0.004	0.010
D	4.700	5.150	0.185	0.203
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

IMPORTANT NOTICE

RIGHT TO MAKE CHANGES
On-Bright Electronics Corp. reserves the right to make corrections, modifications, enhancements, improvements and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

WARRANTY INFORMATION
On-Bright Electronics Corp. warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with its standard warranty. Testing and other quality control techniques are used to the extent it deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.
On-Bright Electronics Corp. assumes no liability for application assistance or customer product design. Customers are responsible for their products and applications using On-Bright's components, data sheet and application notes. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

LIFE SUPPORT
On-Bright Electronics Corp.'s products are not designed to be used as components in devices intended to support or sustain human life. On-bright Electronics Corp. will not be held liable for any damages or claims resulting from the use of its products in medical applications.

MILITARY
On-Bright Electronics Corp.'s products are not designed for use in military applications. On-Bright Electronics Corp. will not be held liable for any damages or claims resulting from the use of its products in military applications.